An integrated linearization technique for GaAs bipolar WCDMA power amplifier

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Here we report a novel linearization and efficiency improvement technique for heterojunction bipolar transistor (HBT)-based Wireless Code Division Multiple Access (WCDMA) power amplifier. A process solution is proposed where a tantalum nitride (TaN) layer is strapped to the HBT base metal layer that resolves the current hogging issue. This is known as the strap ballasting technique. The resistance introduced by TaN improves the linear output power without trading-off its power added efficiency. At supply voltage of 4 V, the strap ballasting methodology improves the adjacent channel leakage ratio by 4.5 dB compared to the conventional base ballasting technique at output power of 28 dBm. The corresponding improvement in power added efficiency is 4%. The maximum output power delivered by power amplifier is 36 dBm. The proposed technique can be employed in the WCDMA power amplifier to minimize the fundamental trade-off issue between linear output power and efficiency.

Keywords: Heterojunction bipolar transistor, linearization, power amplifier, strap ballasting technique.

NEXT-generation radio transmission requires strict linear transmission capability due to the constraint in spectrum allocation. Therefore, the power amplifier (PA) needs to ensure that the adjacent channel leakage ratio (ACLR) criterion is met with in order for the transmitter to transmit high data rate without error[1]. Though gallium nitride (GaN)-based PA is capable of delivering high linear output power, it is found to be sensitive to input impedance which depends on its own gate periphery[2]. Therefore, GaAs power amplifiers, which have enhanced linearity performance compared to CMOS power amplifiers, are currently in demand in consumer communication due to their high-quality passives[3]. However, due to its positive temperature coefficient characteristic, GaAs-based heterojunction bipolar transistor (HBT) is susceptible to thermal runaway phenomenon due to collector current hogging in its unit cell. Thermal runaway results in current gain collapse, which eventually shuts down the unit cell due to self-heating effect[4]. This fundamental issue serves as a design constraint for higher linear output power transmission[5]. Hence, the linearity performance is usually traded-off with the efficiency of PA[6].

The aftermath of the thermal runaway effect is a higher collector current being injected by the designated unit cell. Higher collector current would eventually lead to a dependent chain of increase in the unit cell temperature. Subsequently, the base–emitter voltage of the cell will drop due to the self-heating effect, resulting in collector current hogging in the remaining active unit cell. Current hogging increases the temperature and subsequently shuts down the remaining unit cells. Eventually, it leads to collapse of the total collector current in the transistors. Figure 1 illustrates two unit cells which are connected in parallel. When device 1 is operating at a higher temperature, a drop in the base–emitter voltage increases its collector current, I_{cc1}. On the other hand, device 2, which runs at a slightly cooler temperature, compensates to maintain the total collector current, I_{cc} by regulating its base emitter voltage resulting in a lower collector correct I_{cc2}. As shown in Figure 2, when I_{cc1} increases I_{cc2} moves downhill which eventually shuts down device 2. Figure 3 illustrates the gradual degradation in the base–emitter voltage, V_{be} of device 1 as the base current increases proportionally due to the device operating temperature. Figure 2 confirms that the HBT unit cells are

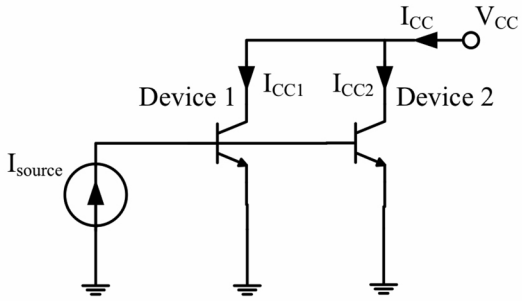

Figure 1. Class-AB biasing point in the IV curve.

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subjected to thermal runaway effect. An analytical model has been accordingly presented in predicting this phenomenon to certain accuracy[7]. While designing a PA compatible with the multi-carrier radio modulation schemes such as long term evolution (LTE) and Wireless Code Division Multiple Access (WCDMA), the HBT PA needs to be thermally efficient as the modulation scheme shows a high peak-to-average ratio, which results in increase in the junction temperature of the PA, leading to nonlinear operation[8]. Initially, emitter ballasting concept is implemented to reduce the effect of thermal runaway by suppressing the junction temperature rise threshold[9]. Further improvement is obtained through base ballasting technique as it is proven to exhibit decreasing current gain to temperature dependency characteristic[10]. Bayraktaroglu and Salib[11] proposed that the thermal isolation circuit be integrated between the current source and the power stage as a substitute for the base-ballasting concept. To improve the thermal stability, base ballast resistor was replaced by depletion field effect transistor (FET)[12]. Basically, the depletion FET is integrated to the base of the HBT, which acts as a nonlinear base ballast. On the other hand, Jin Dong *et al.*[13] proposed an optimized value of base ballast resistor based on thermal feedback network analysis to reduce the trade-off in power gain. Based on computer-aided simulation results, the HBT architecture conceptually requires a smaller base ballast resistor compared to bipolar junction transistor (BJT)[13]. Regardless of the technique, base ballast tends to degrade the power gain of the PA and contributes to the degradation of linear output power[14]. Therefore, in order to counter the aforementioned degradation, efficient linearization techniques are needed[15]. Among them, the prominent techniques include Analog pre-distortion (APD) linearization and digital pre-distortion (DPD) linearization.

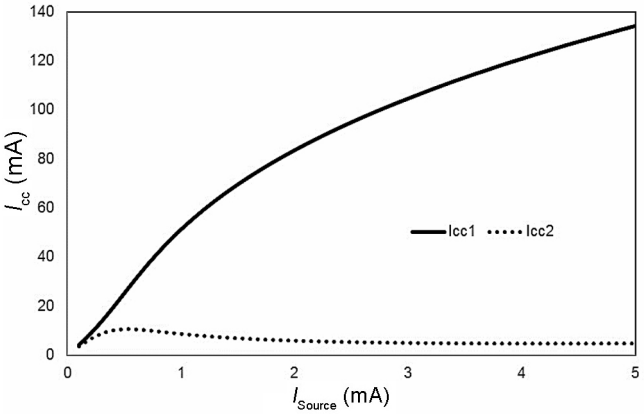

Figure 2. Current collapse phenomenon observed in device 2 represented by I_{cc2}.

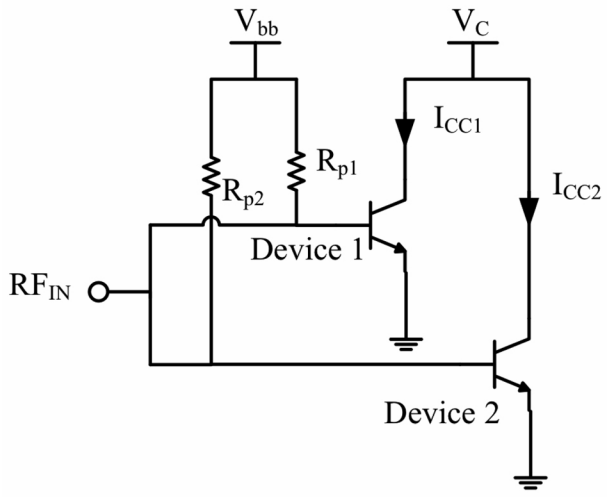

Figure 3. Strap resistors, R_{p1} and R_{p2} are implemented mitigating thermal runaway phenomenon. RF_{IN} denotes the input RF power node.

The principle operation of APD is the generation of inverse phase and magnitude response of the third (IMD3) and fifth (IMD5) order nonlinearity components to counter the components generated by the PA. For WCDMA application, an integrated cuber predistortion followed by second harmonic injection is proposed to cancel the nonlinearity effects[16]. The cuber predistortion cancels the IMD3 effect, whereas the second harmonic injection minimizes the IMD5 effect. To further improve the linear operating bandwidth, the DPD technique has been introduced. Using DPD an accurate synthesis of the IMD3 and IMD5 coefficients is achieved, thus improving the linearization dynamic range. Therefore, it can be used to linearize highly nonlinear PAs such as the class-D configuration[17]. To improve the accuracy and reduce the processing time, the memory-less DPD technique was introduced which reduces the sampling speed[18]. However, the complexity of implementation and consumption of larger board space are among the disadvantages of the DPD technique. On the other hand, complex efficiency enhancement techniques are needed to prevent the flow of excessive collector current I_{cc} that damages the transistor[19]. To reduce the trade-off between efficiency and linearity, smart power cell network design is proposed to be implemented in the GaAs HBT process[20]. However, this technique utilizes substantial amount of physical ballast resistors followed by inner matching network for each unit cell.

In the present study, a new linearization scheme is proposed for HBT power amplifier. This scheme introduces the concept of integrating strap ballasting which prevents current hogging in the HBT unit cells, thus delivering higher linear output power without trading-off the power added efficiency (PAE). The result shows that the implementation of strap ballasting in the existing HBT process not only prevents current collapse in the devices connected in parallel, but also improves the ACLR by 4 dB for WCDMA protocol. A 4% improvement in PAE is also achieved, which affirms the contribution of integrated strap ballasting.

HBT power cell optimum conduction angle

An optimum conduction angle plays an essential role in determining the linearity performance of the PA. This is because the rise of even and odd order current components is significant as the conduction angle reduces. Hence an optimum operating point is always desired. The collector current waveform is represented as

$$I_{cc} = I_{ccq} + (I_{max} - I_{ccq})\cos\theta - \alpha/2 < \theta < \alpha/2, \quad (1)$$

where

$$\cos(\alpha/2) = -\left(\frac{I_{ccq}}{I_{max} - I_{ccq}}\right). \quad (2)$$

Hence

$$I_{cc} = \frac{I_{max}}{1-\cos(\alpha/2)}(\cos\theta - \cos(\alpha/2)). \quad (3)$$

The trigonometric Fourier series (TFS) is applied to analyse eq. (3). TFS is given as

$$I_{cc\,total} = I_{dc} + \sum_{n=1}^{\infty} I_{ccn}\cos(n\theta) + \sum_{n=1}^{\infty} I_{ccn}\sin(n\theta). \quad (4)$$

Since the collector current waveform in Figure 4 is an even waveform, therefore

$$I_{cc\,total} = I_{dc} + \sum_{n=1}^{\infty} I_{ccn}\cos(n\theta). \quad (5)$$

The DC current, I_{dc} is given by

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2))\mathrm{d}\theta, \quad (6)$$

whereas the magnitude of the nth order collector current components is given by

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cdot \cos n\theta \mathrm{d}\theta. \quad (7)$$

Solving eq. (6) for the DC term and eq. (7) for the fundamental component, I_1 ($n = 1$) to fifth order I_5 ($n = 5$) results in:

$$I_{dc} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}. \quad (8)$$

$$I_1 = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)}, \quad (9)$$

$$I_2 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\sin\left(\frac{\alpha}{2}\right) - \frac{1}{3}\sin\left(\frac{3\alpha}{2}\right)\right], \quad (10)$$

$$I_3 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\frac{1}{3}\sin\alpha - \frac{1}{6}\sin 2\alpha\right], \quad (11)$$

$$I_4 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\frac{1}{6}\sin\frac{3\alpha}{2} - \frac{1}{10}\sin\frac{5\alpha}{2}\right], \quad (12)$$

$$I_5 = \frac{I_{max}}{2\pi[1-\cos(\alpha/2)]} \cdot \left[\frac{1}{10}\sin 2\alpha - \frac{1}{15}\sin 3\alpha\right]. \quad (13)$$

From eqs (8)–(13), as the conduction angle increases, the fundamental current component increases due to increase in the DC component. The second-order component, which translates to the second harmonic, has amplitude more than 0 from 0.5π to 1.5π. The peak is at 0.8π, which is close to class-B biasing. Meanwhile, the third order current component reduces as the conduction angle increases. An interesting observation is found at the conduction angle range $\pi < \alpha < 1.8\pi$. In this region, the fundamental component is at the highest and the third-order component is at the lowest. In addition, the fifth-order component is constant near the origin. Hence this plot confirms that it is possible to obtain higher fundamental output power, although the PA is not biased at class-A (conduction angle 2π) mode. The lowest third and fifth order components on the other hand, promise a linear operation to a certain extent with minimum trade-off in efficiency.

Strap resistors linearization technique

Figure 3 shows the circuit diagram for integrating the strap resistors, R_{p1} and R_{p2}. The temperature of device 2 in Figure 3 can be expressed as

$$\Delta T = \theta_{jc} P_{d2}, \quad (14)$$

where θ_{jc} is the thermal resistance and P_{d2} is the power dissipated defined as

$$P_{d2} = I_{cc2} V_c. \quad (15)$$

Substituting P_{d2} into eq. (14):

$$\Delta T = \theta_{jc} I_{cc2} V_c. \quad (16)$$

The collector and base current of device 2 are expressed as

$$I_{cc2} = \beta I_{b2}, \tag{17}$$

where I_{b2} is represented as

$$I_{b2} = \frac{v_{bb}}{R_{p1} || R_{p2}}, \tag{18}$$

resulting in

$$I_{cc2} = \beta \frac{v_{bb}}{R_{p1} \,||\, R_{p2}}. \tag{19}$$

Substituting eq. (19) into eq. (16)

$$\Delta T = \theta_{jc} \beta \frac{v_{bb}}{R_{ss}} V_c, \tag{20}$$

where $R_{ss} = R_{p1} \,||\, R_{p2}$.

Equation (20) shows that an increase in temperature relates to an inverse dependency to the total strap resistance, R_{ss}. Hence an equivalent temperature is preserved at the unit cells inheriting the highlighted relation in eq. (20), which results in uniform current flow among the unit cells (Figure 4). As these strap resistors are not placed in series to the RF input power path of the HBT unit cells, the input power is not subject to distortion. Hence it serves as a significant contribution to the linearity performance of the PA. This can be proved using the following equations. Referring to the power series:

$$I_{out} = a_0 + a_1 I_{tot} + a_2 I_{tot}^2 + a_3 I_{tot}^3, \tag{21}$$

where

$$I_{tot} = I_{cc1} + I_{cc2}. \tag{22}$$

Since $I_{cc1} = I_{cc2}$ as shown in Figure 4, therefore $I_{tot} = 2I_{cc2}$. With this, eq. (21) becomes

$$I_{out} = a_0 + 2a_1 I_{cc2} + 4a_2 I_{cc2}^2 + 8a_3 I_{cc2}^3. \tag{23}$$

Inserting eq. (19) into eq. (23)

$$I_{out} = a_0 + 2a_1 \left[\frac{\beta V_{bb}}{R_{p1} \,||\, R_{p2}} \right] + 4a_2 \left[\frac{\beta V_{bb}}{R_{p1} \,||\, R_{p2}} \right]^2 + 8a_3 \left[\frac{\beta V_{bb}}{R_{p1} \,||\, R_{p2}} \right]^3. \tag{24}$$

From eq. (24), it can be observed that the magnitude of the third order component, which has a negative impact on the linearity performance of the PA, is greatly reduced with the integration of the strap ballasting technique.

HBT model development and results

Figure 5 illustrates the proposed stack-up for the linear HBT. The strap ballasting resistors are made of tantalum nitride (TaN) layer that is integrated with the base metal layer of the transistor, thus distinguishing it from the typical HBT process. The existing contact and metal 1 (MET1) layers are used as contact points for the integrated strap resistor. Figure 3 depicts the corresponding schematic of these unit cells.

The proposed linear HBT model with built-in strap resistance is deployed in a class-AB PA. The performance

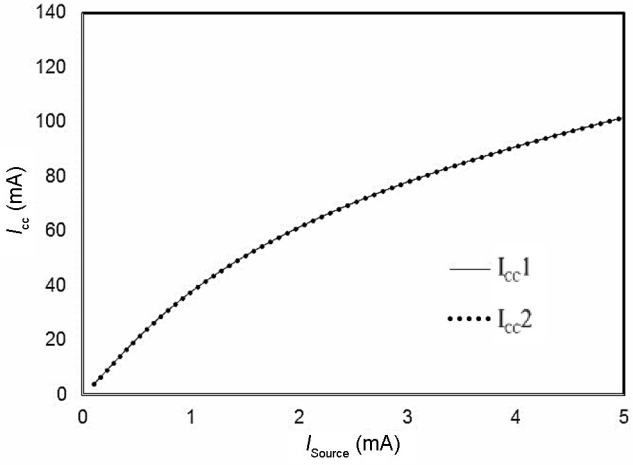

Figure 4. Collector current in device 1, I_{cc1} and device 2, I_{cc2} do not collapse after integration of strap resistors. Therefore, $I_{cc1} = I_{cc2}$.

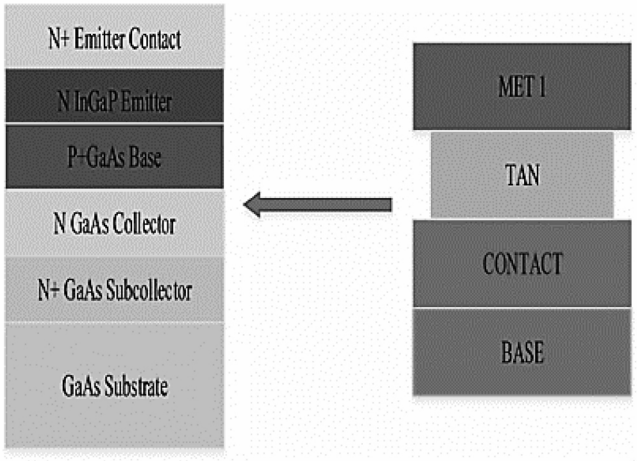

Figure 5. The proposed stack up of the HBT PA.

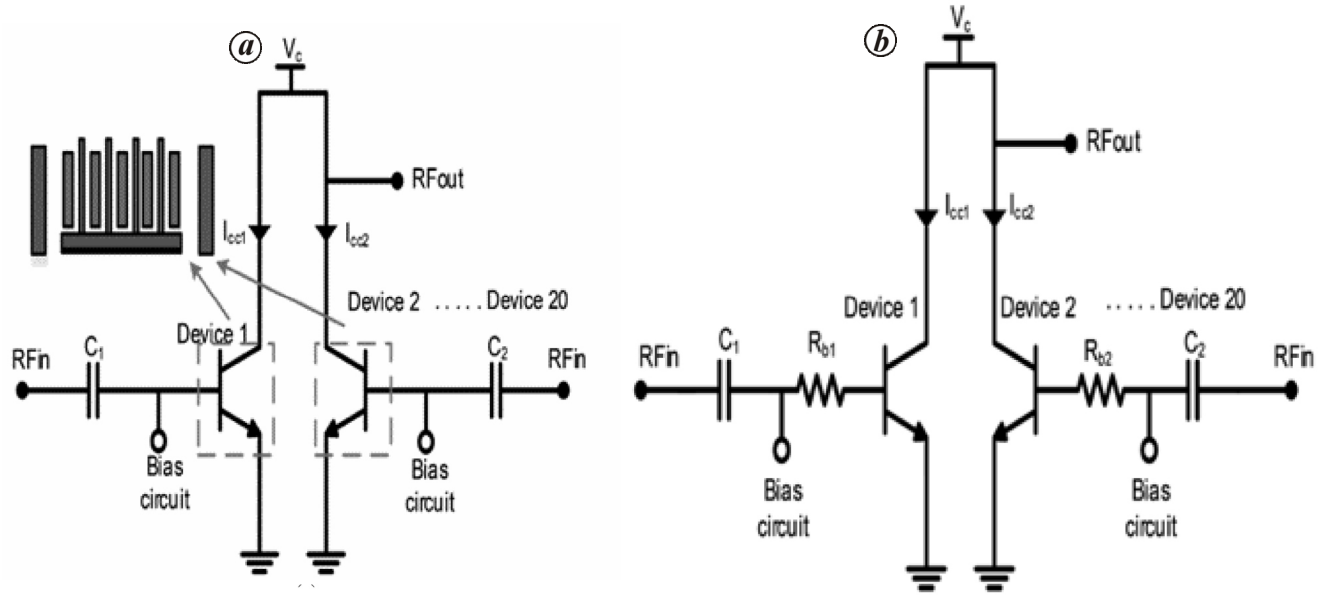

Figure 6. The schematic for both PA: ***a***, Class AB PA with the proposed strap ballasting model; ***b***, Class-AB PA with the conventional base ballasting (R_b) technique.

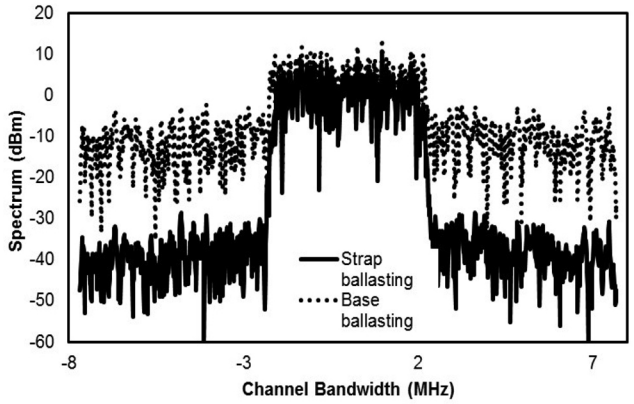

Figure 7. Power spectrum plot of the PA for both techniques at maximum linear output power of 28 dBm.

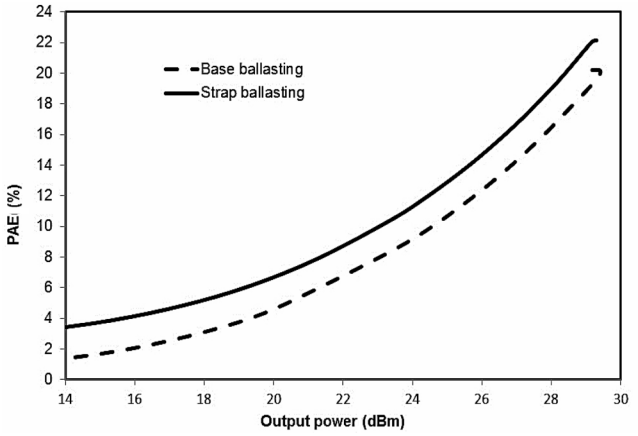

Figure 8. The PAE plot across output power for both techniques.

Table 1. Performance summary of the power amplifier

Parameters	Results
Technology	2 μm InGaP/GaAs HBT
Supply voltage	4 V
Frequency	1.98 GHz
Mode	WCDMA
Maximum output power	36 dBm
Maximum linear output power	28 dBm (ACLR – 48 dBc)
Power added efficiency @ 28 dBm	20%

is then compared with the conventional base ballasting technique. To ensure fair comparison, both PAs are biased at the optimum conduction angle of 1.3π that has been calculated in the earlier section. The linear HBT model is designed and simulated with 3D EM simulation software. Figure 6 depicts the schematic of both PAs. Twenty devices are integrated in parallel.

The proposed linear HBT model has been verified for linear transmission capability by simulating the ACLR and power spectrum. Figure 7 compares the power spectrum of the two techniques, which obviously shows that strap ballasting has a lower adjacent power. Figure 7 concludes the strap ballasting concept delivers better linear output power compared to the base ballasting technique.

Figure 8 shows the PAE plot for both ballasting techniques. Due to thermally stable and lower current consumption, the strap ballasting technique has better PAE. For the base ballast technique, the PAE failed to show continuous improvement compared to strap ballasting at higher output power. Table 1 provides the performance

summary of the designed strap ballasting power amplifier.

Conclusion

In this work, a new linearization and thermal compensation technique for GaAs HBT PA is presented. The strap ballasting resistors play a vital role in improving the linearity of the PA without degrading the PAE. The fundamental issue of thermal runaway and its relation to linearity has been addressed, and a solution proposed. This has been proven using mathematical and simulation analysis. The fully integrated solution enables the design of a miniature PA confining to less than 1 mm^2 area. Results show that the PA built using strap ballasting technique is able to deliver a maximum output power of 36 dBm, without severe gain compression or expansion. Compared to the conventional base ballasting concept, this technique also helps deliver higher linear output power and PAE for a WCDMA signal profile. Hence, the proposed methodology is an effective, low-cost and a reliable solution for eliminating the bottleneck in designing a linear and efficient PA for mobile phone communication.

1. Ramiah, H., Eswaran, U. and Kanesan, J., A high gain and high linearity class-AB power amplifier for WCDMA applications. *Microelectron. Int.*, 2013, **31**(1), 1–7.
2. Qin Ge, Liu, X., Chen, X., Luo, W. and Liu, G., Ku-band high power internally matched GaN HEMTS with 1.5 GHz bandwidth. *Microelectron. Int.*, 2013, **90**, 19–23.
3. Drakaki, M., Siskos, S. and Hatzopoulos, A., A 0.5–20 GHz bandwidth enhanced distributed amplifier. *Microelectron. Eng.*, 2012, **90**, 26–28.
4. Liu, W., Nelson, S., Hill, D. G. and Khatibzadeh, A., Current gain collapse in microwave multi-finger heterojunction bipolar transistors operated at very high power densities. *IEEE Trans. Electron Devices*, 1993, **40**, 1917–1927.
5. Sweet, A., *Designing Bipolar Transistor Radio Frequency Integrated Circuits*, Artech House, London, 2008.
6. Jagadheswaran, U. R., Ramiah, H., Mak, P. I. and Martins, R. P., A 2-μm InGaP/GaAs class-J power amplifier for multi-band LTE achieving 35.8-dB gain, 40.5% to 55.8% PAE and 28-dBm linear output power. *IEEE Trans. Microwave Theory Technol.*, 2016, **64**, 200–209.
7. Liou, J. J., Liou, L. L. and Huang, C. I., Analytical model for the AlGaAs/GaAs multi-emitter finger HBT including self-heating and thermal coupling effects. *IET J. Circuits, Devices Syst.*, 1994, **141**, 469–475.
8. Thein, T. T., Law C. L. and Fu, K., Frequency domain dynamic thermal analysis in GaAs HBT for power amplifier applications. *Prog. Electromagn. Res.*, 2011, **118**, 71–87.
9. Liou, L. L., Jenkins, T. and Huang, C. I., Effect of base potential distribution on thermal runaway and the power limitation of the heterojunction bipolar transistor with circular dot geometry. In IEEE, Electron Devices Meeting, Hong Kong, 1996, pp. 49–52.
10. Liu, W. *et al.*, The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors. *IEEE Trans. Electron. Devices*, 1996, **43**, 245–251.
11. Bayraktaroglu, B. and Salib, M., Unconditionally thermally stable cascade GaAs HBTs for microwave applications. *IEEE Microwave Guided Wave Lett.*, 1997, **7**, 187–189.
12. Jang, J., Kan, E. C., Arnborg, T. Johansson, T. and Dutton, R. W., Characterization of RF power BJT and improvement of thermal stability with nonlinear base ballasting. *IEEE J. Solid-State Circuits*, 1998, **33**, 1428–1432.
13. Jin Dong, Y. *et al.*, A simple method to optimize the ballasting resistor of RF power HBT. In Proceedings of the 7th International Symposium on Antenna Propagation and EM Theory, Guilin, China, 2006, pp. 1–4.
14. Maas, S., Ballasting HBTs for wireless power amplifier operation. In Proceedings of the IEEE International Workshop on Integrated Nonlinear Microwave and Millimeter-Wave Circuits, Portugal, 30 January 2006, pp. 2–5.
15. Eswaran, U., Ramiah, H. and Kanesan, J., Class-E power amplifier with novel pre-distortion linearization technique for 4G mobile wireless communications. *Elektron. IR Elektrotech.*, 2014, **20**, 53–56.
16. Matsubara, H., Ishihara, K., Miyadai, N. and Nojima, T., A novel 3rd and 5th order predistortion circuit for 2 GHz band WCDMA amplifier. In Proceedings of Asia-Pacific Conference, APMC 2007, Bangkok, Thailand, 2008, pp. 1–4.
17. Landin, P. N., Fritzin, J., Moer, W. V., Isaksson, M. and Alvanpour, A., Modeling and digital predistortion of class D outphasing RF power amplifiers. *IEEE Trans. Microwave Theory Tech.*, 2012, **60**, 1907–1915.
18. Hammi, O., Kwan, A., Bensmida, S. and Morris, K. A., A digital predistortion system with extended correction bandwidth with application to LTE-A nonlinear power amplifiers. *IEEE Trans. Circuits Syst.*, 2014, **61**, 3487–3495.
19. Young, S. J., Jukyung, C. and Sangwook, N., High-efficiency power amplifier using novel dynamic bias switching. *IEEE Trans. Microwave Theory Techn.*, 2007, **55**, 690–696.
20. Xiaohong, S., Huai, G. and Weifeng, S., Peripheral adaption power cell network for high efficiency and high linearity power amplifier. *IEEE Microwave Wireless Components Lett.*, 2014, **24**, 799–801.

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