

Composition of magnetic tunnel junction-based magnetoresistive random access memory for Field-Programmable Gate Array

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In this study, the schematics for Magnetic Tunnel Junction-Magnetoresistive Random Access Memory (MTJ-MRAM) are designed and simulations are carried out in 45 and 90 nm Complementary Metal-Oxide Semiconductor (CMOS) Very Large Scale Integration (VLSI) technology using analog design environment. Other memory circuits like volatile Static Random Access Memory (SRAM) and non-volatile flash memory are designed and behavioural waveforms verified. The output behavioural characteristics of MTJ-MRAM are compared with that of SRAM and flash memory. The attributes like power and delay are calculated and compared with SRAM and flash memory circuits. The study was carried out in order to integrate the non-volatile memory with field-programmable gate array (FPGA) architecture and design a non-volatile memory-based FPGA. MTJ-MRAM shows better performance than volatile SRAM and non-volatile flash memory in terms of power and delay parameters.

Keywords: Behavioural waveforms, field-programmable gate array, magnetic tunnel junction, memory circuits.

In the era of growing technology and fast computation there is constant demand for computing systems that performs various computations in which memory place a dominant role. Memory devices are basically classified as volatile and non-volatile memories. In volatile memory devices, data are stored only till the power is on, and they lose data when powered off. While non-volatile memory devices, store the data even when the system is powered off.

SRAM is a class of memory which is volatile in nature, as it loses data when powered off^{1,2}. Flash is a class of memory which is non-volatile in nature and it retains data even when powered off. FPGAs are classified based on memory technology. SRAM-based FPGAs are of volatile type, while flash-based and anti-fuse-based FPGAs are of non-volatile type. Anti-fuse-based FPGAs are only one-time configurable and are used only once for some specific applications. Consequently flash-based FPGAs are increasingly beneficial among the non-volatile memory

types, but still is not more preferred than SRAM based FPGA as SRAM offers more advantages than all non-volatile FPGA types. The sole limitation of SRAM based FPGA is volatility. This creates demand for new non-volatile memory types to be integrated with FPGA for better performance³. Magnetoresistive random access memory (MRAM) is a class of memory which gives the advantage of non-volatility. There are many variations in the construction of MRAM types.

Charge and spin are the two important inherent properties of the electrons. Magnetism can be ascribed to the electron spin. Amalgamation of data storage and data handling within a single material is seen through the fresh perspective of spin in semiconductors. These devices are referred to as spintronic or spin electronic devices, and are part of the study involving both their electronic charge and magnetic moment^{1,4}.

A magnetic tunnel junction (MTJ) or tunnelling magnetoresistance (TMR) is the consequence of a quantum mechanical effect called tunnelling. This nanoscale effect occurs in the MJT, which comprises a thin insulating layer between a couple of ferromagnets or magnetic metals. When a certain potential is applied across it, the electrons would be able to pass from one ferromagnet to the other through the slim insulator creating a load resistance.

Magnetoresistance is the inherent characteristic of a material when magnetic field is applied externally, and brings about a variation in the material's electrical resistance. This property of magnetoresistance can be extended to sensors, hard disks and electric current as it functions in the absence of any physical connection⁵⁻⁸. The MRAM is mainly comprised of MTJ which is responsible for the switching occurring in the former. This device that is based on spin and functions on the principle of magnetoresistance, exhibits non-volatile characteristics. Layers of ferromagnets separated by an ultra-thin film of dielectric forms the covering layer of the MTJ. These layers are in nanoscale and all together leads the junctions to thin vertical nanostructure called MTJ. Figure 1 shows the cross-section of a MTJ. The upper layer is called free layer, whose magnetic orientation can be changed freely. While the lower layer is called pinned or reference layer; the spin orientation is fixed in this layer when the device is manufactured. The barrier between the pinned and free layers is thin enough, so that electrons

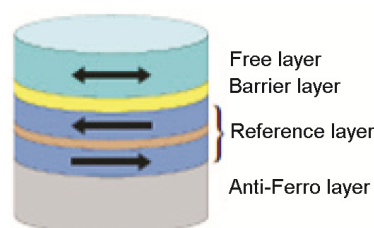


Figure 1. Magnetic tunnel junction (MTJ).

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can tunnel through and offer some resistance even if the layers are insulating. The pinned layer is found to be denser in comparison to the free layer. Since the pinned layer has a fixed magnetic orientation with reference to the free layer, large external bias energies and high blocking temperatures are desired. The pinned layer consisting of two sub-layers separated by the Ruthenium (Ru) film separates the two sub-layers of the pinned layer in order to establish an antiferromagnets structure and aids in eliminating the free layer of the magneto-static field^{2,9,10}.

One of the first-generation MTJs was the field-induced magnetic switching (FIMS) type, which used synthetic anti-ferromagnetic layers¹¹. The next generation MTJ was thermally assisted switching (TAS) type junction, which used an additional antiferromagnetic layer along with ferromagnetic layer^{12,13}. In thermally assisted switching MRAM (TAS-MRAM), on heating the cell, the current changes across the ferromagnetic and anti-ferromagnetic layers. TAS offered advantages like lower power, higher density and lower switching disturbance compared to FIMS. Yet TAS-MRAM had bottleneck of switching speed that was limited due to the thermal switching nature of TAS-MTAM. Another type of implementation of MTJ was STT, in which the spin of the carriers in MTJ can be changed by applying spin-polarized current¹⁴⁻¹⁶. The next generation MTJ was a combination of TAS and STT, in which an additional antiferromagnetic layer was required to heat up the MTJ¹⁷. The next generation MTJ was implemented using spin Hall effect (SHE) and spin-transfer torque (STT)^{18,19}. Here, the MTJ device was constructed using STT in which MTJ was deposited on a heavy metal resulting in a three-terminal device.

FPGA performance is constrained by its volatile memory technology. Data configuration of SRAM FPGA is volatile and can be reconfigured in-circuit. In anti-fuse based FPGA, the configuration is set by 'burning' internal fuses and is non-volatile, but cannot be changed, i.e. it is only one-time programmable. However flash-based configuration is non-volatile and is configured off-board, but has increased internal leakage power. Due to the volatile nature of FPGA, data need to be loaded each time on the device, and the configuration time of data on the device increases due to iterations. The efficiency of the FPGA device is thus affected and the device demands non-volatility with increased configuration speed. Novel non-volatile memory (NVM)-based FPGAs need to be designed in order to improve the overall performance of the device. This is achieved by reducing configuration time and the power required to configure the data on the device by making the memory of the device non-volatile. Here we describe the construction of a non-volatile MTJ-based MRAM for FPGA architecture. Starting from the modelling of a basic MTJ cell, a non-volatile memory circuit is demonstrated and compared with existing volatile and non-volatile FPGA memories. Also, the power

dissipation and access time of the designed MRAM circuit are compared with existing FPGA memories.

The MTJ is basically the fundamental part of the MRAM memory circuit and switching of the memory circuit is dependent on the MTJ integrated with the memory circuit. The MTJ changes its resistance depending upon change in magnetic orientation of 'free' and 'fixed' layers. In order to realize this resistance and make a memory circuit, a switching element is required. CMOS transistors are used for switching purpose. The programming of the element is done mainly by current sink. The current pulse through the switching element and bit line provide magnetic field to the MTJ and change the resistance across the junction. The pulse is more than enough to flip the orientation of MTJ layers and store bits. Depending on the supply voltage the pulse is generated and the resistance that MTJ offers changes accordingly^{5,9}.

The MTJ acting as memory element of MRAM can be modelled as a resistive element. Depending on the orientation of electrons in free and fixed layers, resistance is created in the MTJ memory element. Figure 2 shows the orientation and development of variable resistance. The MTJ hence can be modelled as a variable resistance, and to change the orientation of the electrons in free and fixed layers MTJ-based MRAM can be modelled using two fields acting on the MTJ memory element.

One of the key functionality of memory is characterized as its capacity to save data and through this ability, memory can be categorized as volatile and non-volatile type. One such non-volatile characteristic is obtained by MTJ. The orientation of layers in MTJ offers two states, namely parallel and antiparallel. As the carriers in the layers orient, they result in parallel and anti-parallel states. Each state offers some resistance and hence the MTJ can be modelled as a resistive element offering high and low resistance depending on the state that the MTJ is offering. Various methods are employed to model MTJ. The proposed method uses a current source to generate current pulse, which forces to change the orientation of charges in MTJ and hence the alignment of layers in the MTJ structure.

Basically an MTJ changes its resistance depending upon change in magnetic orientation of the free layer with respect to the fixed layer or reference layer. In order to exploit this variation in resistance and build a memory cell, we can use reliable read and write operation with the help of switching elements. Generally, CMOS transistors, semiconductor diodes or bipolar junction transistors are



Figure 2. Resistive element from MTJ.

various choices available for this purpose in order to read the MTJ state (resistance). These switching elements also isolate the MTJ device from the word line when that particular device is not addressed. These cells are programmed by sending a pulsed current through the word line and bit line. The whole memory has to be designed in such a way that the field from a single pulse on either line is not adequate to flip the orientation of the MTJ free layer, but a combination of fields generated by these two lines is large enough for switching to occur. The MTJ can be modelled as shown in Figure 3; the circuit is designed using Cadence tool in 45 nm and also 90 nm technology.

The MTJ-MRAM can be modelled as shown in Figure 3, in which the memory element of MRAM is designed using two fields acting on the memory element. By modelling the MTJ using two acting fields, the memory element is considered to behave as a resistive element that holds the data. One of the fields is produced due to current source and the other field is generated by the data line.

In order to provide a field for the memory element, specially for free layers of the MTJ, a current source is used. The current source is created and implemented in a specific manner. A current source can be implemented by a transistor so the circuit is connected to a transistor. The transistor is biased such that the current flows through it. The current through the transistor may be controlled using biasing voltage. It is assumed that current flow through the transistor reaches the free layer of the MTJ through the access transistor. A magnetic field is created due to the current flow and hence the electrons change their orientation continuously. The current flowing through the access transistor is controlled by control signal of the memory. The other field is the data provided to the memory element through bit line of the memory.

The proposed model of the MTJ shown in Figure 3 can be considered as memory model for MTJ-MRAM, which

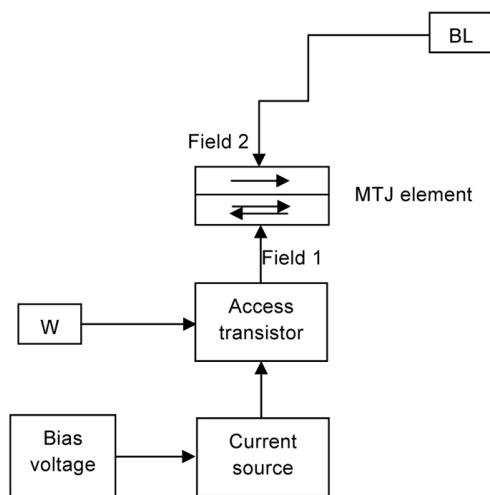


Figure 3. Proposed model of MTJ-based magnetoresistive random access memory (MRAM).

can be used as a potential non-volatile memory design. The proposed design provides the basic memory element and access control to the memory element. Figure 4 shows the design implementation of MTJ-MRAM using CMOS technology. The current source is implemented using transistor M1 controlled by the bias gate voltage of M1. The current flowing across the transistor is controlled by the bias voltage applied to M1. The current flows through the transistor M2 that is controlled by the control signal of the memory known as word line (WL). The current flows to the MTJ element that is modelled as resistance R1 in Figure 4. The other field to the MTJ element is through bit line of the memory that is given directly to the fixed layer of MTJ.

MTJ-MRAM is modelled as a device that is controlled by two fields, one of the fields is fixed and the other is variable. The variable field is the one that is given directly to the device through the bit line, which is the data fed to the device. While the fixed field is the one that is given to the MTJ through current source. The supply is given to current source transistor, so that the circuit outputs a fixed amount of field. The voltage at the gate of transistor M1 is biased such that the current flowing through the transistor can be controlled. This current flowing through the access transistor produces a fixed voltage and hence produces a fixed field to the other layer of the MTJ. In this way the MTJ is offered with fixed and variable fields in order to exhibit variable resistance. The access transistor M2 with the MTJ structure attached to it acts like a MRAM memory, and the data can be stored or retrieved from the MRAM memory circuit.

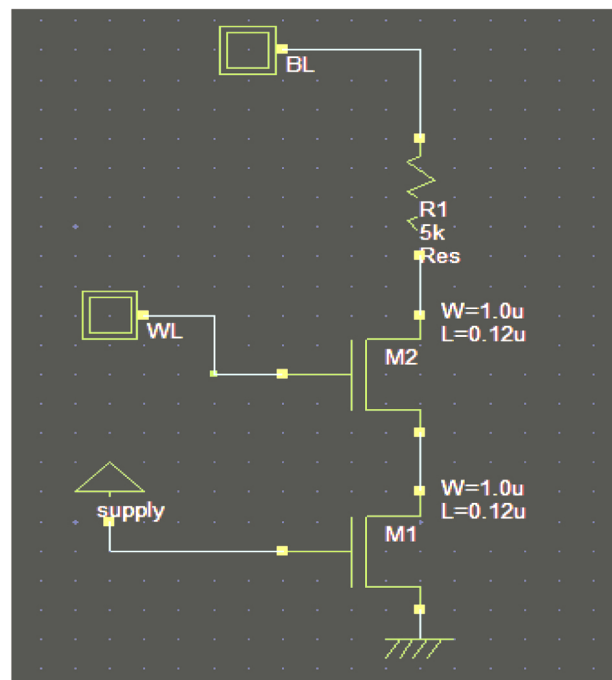


Figure 4. Schematic of MTJ-MRAM.

Table 1. Estimation of magnetoresistive random access memory (MRAM), FLASH and SRAM attributes

Memory	Delay	Power (nW)	Feature
SRAM (90 nm technology)	64.11×10^{-9} s	151.3	Volatile
NOR-flash (90 nm technology)	4.568×10^{-12} s	5.4	Non-volatile
MTJ-MRAM			
90 nm technology	15.14×10^{-15} s	19.97	Non-volatile
45 nm technology	70.85×10^{-15} s	11.73	Non-volatile

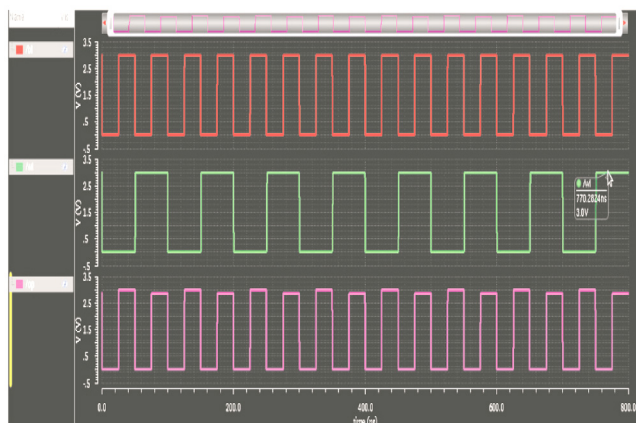


Figure 5. Behavioural waveforms of MTJ-MRAM.

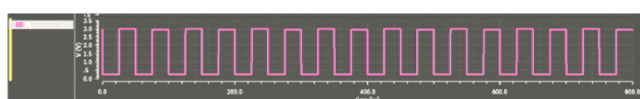


Figure 6. Behavioural waveforms of flash memory.

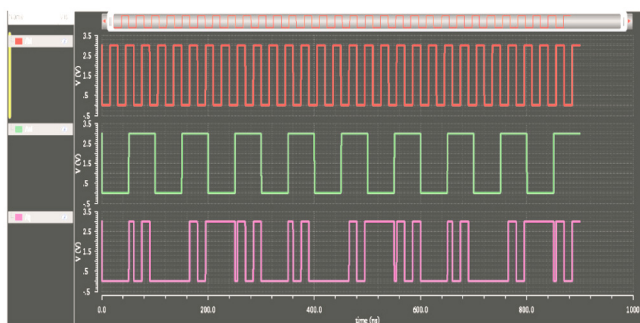


Figure 7. Behavioural waveforms of SRAM.

When the current pulse is given to the MTJ through the access transistor, it varies the charge orientation depending on the strength of the current pulse produced. The current pulse generated from the current source M1 is given to the MTJ through cell select transistor M2. When word line is high and the other pulse is produced by the bit line, i.e. when the word line and bit line are equal to 1, then the free layer of the MTJ is oriented in a direction which is opposite to that of the fixed layer. Both layers of the MTJ are aligned in opposite directions and they are in anti-parallel state offering high resistance. Therefore,

when that word line and bit line are equal to 1, the MTJ stores logic 1 in the memory cell.

Consider the case when the current pulse is given to the MTJ through a cell select transistor controlled by the word line and the second pulse is applied through the bit line. The current pulse through the bit line given to the MTJ changes the orientation of charge carriers in the ‘free layer’. Due to the alignment of charges in the two layers, they are now in parallel state offering low resistance. Hence when the word line is high 1 and bit line is low 0, the MTJ stores logic 0 in its memory cell.

A schematic of MTJ-MRAM has been designed using Cadence electronic design automation (EDA) tool to obtain behavioural characteristics and performance parameters like power dissipation and delay. Also, circuit design for flash memory and SRAM was carried out in order to compare the present memory technologies both volatile and non-volatile types, with the designed MTJ-MRAM circuit. The behavioural characteristic waveforms for non-volatile MTJ-MRAM is presented in Figure 5. Also the characteristic waveforms for non-volatile NOR flash memory and volatile SRAM are also shown in Figures 6 and 7. The waveforms in Figure 5 are compared with that of Figure 6 and 7 in order to check non-volatility of MTJ-MRAM circuit. It can be seen from these figures that MTJ-MRAM shows similar behaviour as that of the non-volatile memory. The data are stored even when the word line is low.

The circuits were designed in 90 nm technology, and power and delay were estimated. For the designed MTJ-MRAM circuit in 90 and 45 nm technology, the power and delay were also estimated. The power consumption was found to be ~19.97 nW and time delay was found to be ~15.14 fs for 90 nm. While the power consumption was found to be ~11.73 nW and time delay ~71.85 fs for 45 nm. Table 1 shows the power consumption, circuit delay time and prominent features in comparison to existing volatile and non-volatile memory circuits.

The table clearly shows that MTJ-MRAM exhibits strong features of low power dissipation compared to SRAM and flash. The delay time of MTJ-MRAM shows a lower value compared to SRAM and flash memory. However, the power dissipation shows results comparable to flash, but lower power dissipation compared to SRAM. Further, it is seen that the attributes for 45 and 90 nm technology MTJ MRAM memory do not show significant difference, indicating that the MTJ process is independent of channel length.

From the behavioural analysis of circuits and the timing analysis of the simulations carried out in the study the following conclusions can be made:

(1) The design parameters of MTJ–MRAM show better performance in terms of delay, showing in femtoseconds exhibiting three time delay reduction in both 45 and 90 nm designs when compared to flash memory circuit.

(2) The design exhibits significant power reduction of about six times compared to SRAM memory circuit in both 45 and 90 nm technology. While the MTJ–MRAM design in 45 nm technology experiences a bottleneck in terms of power dissipation.

(3) The behavioural characteristics of MTJ–MRAM show non-volatility feature. Designing the memory circuit for FPGA architecture, the configuration time of FPGA decreases and speeds up the overall FPGA process with the added advantage of minimized power consumption compared to SRAM-based FPGA.

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Sterically hindered amine functionalized zeolites prepared from fly ash for effective carbon dioxide adsorption

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Highly crystalline zeolite Na-X also known as Linde X, is synthesized in pure form using fly ash waste from coal-fired power plants. Functionalization of as-synthesized adsorbent was carried out using 2-amino-2-methyl-1-propanol in order to apply it in post-combustion carbon dioxide capture. Zeolite Na-X was thoroughly characterized through XRD, FTIR, SEM and TEM analysis. The synthesized zeolite was found to have high surface area and octahedral morphology. Zeolite X and functionalized zeolite X were evaluated in a dynamic adsorption assembly for the uptake of carbon dioxide. Functionalized zeolite was found to have better adsorption capacity at 55°C. It also showed good performance in the presence of moisture. Regeneration studies, however, showed a drop after the second cycle in case of functionalized adsorbent.

Keywords: Amine functionalization, adsorbent, carbon dioxide, fly ash, zeolites.

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