INCREASING THE TRANSISTOR COUNT BY CONSTRUCTING A TWO-LAYER CRYSTAL SQUARE ON A SINGLE CHIP

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ABSTRACT

According to the Moore's law, the number of transistor should be doubled every 18 to 24 months. The main factors of increasing the number of transistor are: a density and a die size. Each of them has a serious physical limitation; the first one "density" may be reached "Zero" after few years, which causes limitation in performance and speed of a microprocessor, the second one "die size" cannot be increased every 2 years, it must be fixed for several years, otherwise it will affect the economical side. This article aims to increase the number of transistors, which increase the performance and the speed of the microprocessor without or with a little bit increasing the die size, by constructing a two-layer crystal square for transistors, which allows increasing the number of transistors two additional times. By applying the new approach the number of transistors in a single chip will be approximately doubled every 24 months according to Moore's Law without changing rapidly the size of a chip (length and width), only the height of a chip must be changed for putting the two layers.

KEYWORDS

Moore's Law, Crystal square, Density, Die size, Number of transistors, Feature size, Design complexity.

1. INTRODUCTION

All manufacturers of a central processing unit (CPU), is also known as a microprocessor, such as Intel, IBM, Sun, Motorola and others design and construct their products to perform the same thing in approximately the same way [1]. Examples of these products are: i80x86, Pentium, Itanium (Intel), PowerPC (IBM), SPARC (Sun), R2000, R12000 (MIPS), etc.

According to the Moore's Law the number of transistors on a chip would be doubled every 18 to 24 months [2, 3]. Raising the transistor count in a CPU automatically increases its speed and performance; more transistors, more clock cycles [4, 5]. Therefore the designers and architects of the CPUs are interested to increase the number of transistors with each new CPU-generation by applying the Moore's law, which doubles the number of transistors according to the design rule by reducing the feature size (size of a transistor), in this case more transistors can be fitted on a chip without changing rapidly the die size (size of a chip).

2. PHYSICAL LIMITATION OF INCREASING THE TRANSISTOR COUNT AND DIE SIZE

Increasing the size of a CPU and the number of transistors will be limited due to the following limitation [6, 7, 8, 9]:

2.1. DENSITY, DESIGN RULE AND DESIGN COMPLEXITY [10,11,12,13]

The transistors and wires are drawn photographically on the chips, therefore the size of the transistors and the width of the wires are determined by the pixel size of the imaging process. The feature size determines the number of transistors that can be fitted on a given chip size. The number of transistors can be raised in case the size of a transistor on a chip goes down, which means the smaller the transistors, the more transistors can be fitted on the chip. Feature sizes have decreased from 10 micron in 1971 to 0.022 micron in 2015; the semiconductor manufacturing processes have decreased from 10 µm in 1971 to 22 nm in 2015 [4, 13, 14] (see Table 1).

Since the surface area of a transistor determines the transistor count per square millimeter of silicon, the transistors density increases quadratically with a linear decrease in feature size. The increase in transistor performance however, is more complex. Devices shrink quadratically in the horizontal and vertical dimensions since the feature sizes shrink. The shrink in the vertical dimension needs a reduction in operating voltage to maintain correct operation and reliability of the transistors. This combination of scaling factors leads to a complex interrelationship between transistor performance and process feature size; transistor performance improves linearly with decreasing feature size [1].

The design complexity of a CPU will be increased, because of the shrinking of the pixel size and the increasing of the density. If the pixel size shrinks double and the density increases double every two years according to Moore's Law, the physical limitation will definitely appear in few years, which means that it will be very difficult to apply Moore's Law in future. Some studies have shown that the physical limitations could be reached by 2018 [6] or 2020-2022 [15, 16, 17, 18].

2.2. TRANSISTOR COUNT AND DIE SIZE [5, 11, 19, 20]

The size of a chip is known as a die size; the chip size depends on the chip manufacturing processes. As mentioned above, the smaller size of a transistor, the larger number of transistors can be fitted on a chip; this allows increasing the size of a chip slowly over time. The die size should be increased due to increasing of the number of transistors.

The die size of the processor refers to its physical surface area size on the wafer. The measure of the die size is a square millimeters (mm^2). The three most important contributing factors to die size are the process technology used, the circuit size in microns, and the design of the processor itself (newer processors are in general larger because they do a lot more).

There are two methods for estimating die size:

Method 1:
Die size (mm^2) = Known or functionality−informed CPU transistor count (M transistors)/
Expected transistor density: based on process technology (M trans./mm^2)

Method 2:
Die size (mm^2) = CPU transistor count:estimate based on Moore's Law (M transistors) /
Expected transistor density: based on process technology (M trans./mm^2)

Expected transistor density for each process technology is reported and updated each year through the International Technology Roadmap for Semiconductors (ITRS).

The number of transistors of Intel microprocessors has increased from 2300 in 1971 to 5,56 billion in 2014 (2.42 million times during 43 years) and the die size has increased from 12 mm^2 in

1971 to 661 mm^2 in 2014 (55.08 times during 43 years). The number of transistors of MIPS microprocessors has increased from 110,000 (R2000) in 1986 to 7.2 million (R14000) in 2001 (65.45 times during 15 years) and the die size has increased from 80 mm^2 in 1986 to 204 mm^2 in 2001 (2.55 times during 15 years). The number of transistors of IBM microprocessors has increased from 1.5 million (Power3) in 1998 to 7.1 billion (IBM z13 Storage Controller) in 2015 (4733.3 times during 17 years) and the die size has increased from 270 mm^2 in 1998 to 678 mm^2 in 2015 (2.51 times during 17 years) (see Table 1).

2.3. PIXEL SIZE AND POWER CONSUMPTION [1,21, 22, 23]

The pixel size determines the transistor's switching speed, the smaller transistors switch faster, so they require less power to be switched. In general, the smaller the chip, the faster it can run. This is due in part to reduced power consumption and heat generation; heat is generated when transistors switch from a zero to a one or vice-versa, and the faster the chip runs, the more switching in a given unit of time, so the more heat that is produced. A chip that overheats locks up or causes computation errors. Designers usually try to move chips to smaller circuit sizes to keep heat down.

Small pixel size allows the battery life of portable devices to be saved for a long time. The energy consumption required for switching transistors is known as dynamic power consumption, which can be increased due to charging and discharging the capacitive output load. Increasing the amount of power requires more hot generation, which can cause an interference of transistors with each other.

Table 1. Evolution of Microprocessors: 1971 to 2015

Manufacturer	Processor	Date of introduction	Number of transistors	Process	Area [mm^2]
Intel	Intel4004	1971	2,300	10 µm	12
	Intel8008	1972	3,500	10 µm	14
	Intel8080	1974	4,400	6 µm	20
	Intel8085	1976	6,500	3 µm	20
	Intel8086	1978	29,000	3 µm	33
	Intel80286	1982	134,000	1.5 µm	44
	Intel80386	1985	275,000	1.5 µm	104
	Intel80486	1989	1,180,235	1 µm	173
	Pentium	1993	3,100,000	0.8 µm	294
	Pentium Pro	1995	5,500,000	0.5 µm	307
	Pentium II	1997	7,500,000	0.35 µm	195
	Pentium III	1999	9,500,000	0.25 µm	128
	Pentium 4	2000	42,00,000	180 nm	217
	Itanium 2 McKinely	2002	220,000,000	180 nm	421
	Core 2 Duo	2006	291,000,000	65 nm	143
	Core i7 (Quad)	2008	731,000,000	45 nm	263

	Six-Core Core i7	2010	1,170,000,000	32 nm	240
	Six-Core Core i7/8-Core Xeon E5	2011	2,270,000,000	32 nm	434
	8-Core Itanium Poulson	2012	3.100,000,000	32 nm	544
	Six-core Core i7 Ivy Bridge E	2013	1,860,000,000	22 nm	256
	15-core Xeon Ivy Bridge-EX	2014	4,310,000,000	22 nm	541
	18-core Xeon Haswell-E5	2014	5,560,000,000	22 nm	661
MIPS	R2000	1986	110,000	2.0 µm	80
	R3000	1988	150,000	1.2 µm	56
	R4000	1991	1,200,000	0.8 µm	213
	R10000	1994	2,600,000	0.5 µm	299
	R10000	1996	6,800,000	0.35 µm	299
	R12000	1998	7,150,000	0.25 µm	229
	R14000	2001	7,200,000	130 nm	204
IBM	POWER3	1998	15,000,000	0.35 µm	270
	POWER4	2001	174,000,000	180 nm	412
	POWER4+	2002	184,000,000	130 nm	267
	POWER5	2004	276,000,000	130 nm	389
	POWER5+	2005	276,000,000	90 nm	243
	POWER6+	2009	790,000,000	65 nm	341
	POWER7	2010	1.200,000,000	45 nm	567
	POWER7+	2012	2.100,000,000	32 nm	567
	Six-core zEC12	2012	2,750,000,000	32 nm	597
	POWER8	2013	4.200,000,000	22 nm	650
	IBM z13 Storage Controller	2015	7.100,000,000	22 nm	678

3. TWO-LAYER CRYSTAL SQUARE

This article proposes constructing a two-layer crystal square for the transistors in a single chip as a new approach for avoiding the physical limitations mentioned above and for applying the

Moore's Law for more years. The new approach of constructing a crystal square for transistors on a chip suggests increasing the number of transistors without changing rapidly the size of the chip. Assume a microprocessor (let's say X) has the following specifications: date of introduction – 2015, one-layer crystal square of transistors, transistor count (number of transistors) – 5 billion, pixel size (feature size) – 0.022 micron, die size (area) – 600 mm^2 (see Figure 1).

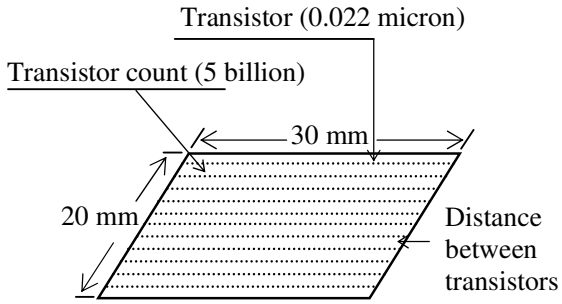

Figure 1. Crystal Square of Transistors

A crystal square of transistors can be constructed using two layers that are equal in size and transistor count, this allows to increase the number of transistors twice (Moore's Law) without touching the feature size and die size (see Figure 2).

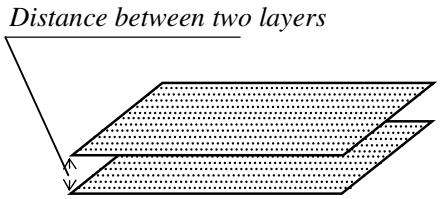

Figure 2. Two-Layer Crystal Square of Transistors

The two-layer crystal square of transistors shown in Figure 2 contains double transistor count without changing feature size and die size. Double number of transistors allows increasing a microprocessor's speed approximately twice. In this case the voltage of transistors must be decreased in order to reduce the dynamic power and energy. Of course it must an isolator between the two layers.

As an example the second generation of the microprocessor (let's say X1) has the following specifications: date of introduction – 2017, Two-layer crystal square, and each layer with the following characteristics: number of transistors – 5 billion (10 billion both), pixel size – 0.022 micron, die size – 600 mm^2 (see Figure 3).

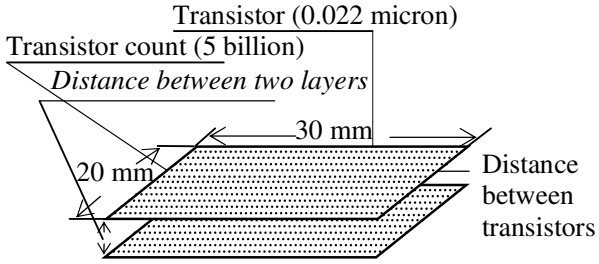

Figure 3. Second Generation

Applying this approach would double transistor count and speed of the microprocessors every two years with slowly increasing the density and area, and decreasing feature size and voltage, so the physical limitations will be reduced and Moore's Law will be continued for many years (may be till 2037 or more).

Assume the third generation of the microprocessor (let's say X2) has the following specifications: date of introduction – 2019, Two-layer crystal square, and each layer with the following characteristics: transistor count – 10 billion (20 billion both), pixel size – 0.019 micron, die size – 688 mm2 (see Figure 4).

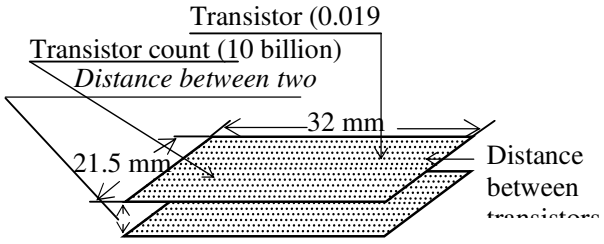

Figure 4. Third Generation

The third generation doubles the transistor count with small decreasing of the feature size (from 0.022 micron to 0.019 micron) and small increasing of the area (from 600 mm^2 to 688 mm^2), of course, with more density, which allows to fit more transistors in small area.

All the assuming characteristics of the microprocessors (X, X1, X2) and others (XN-1 and XN) are shown in Table 2. This table shows some of the assuming microprocessors from 2015 till the year 2037. The number of transistors will have doubled every two years. The feature size will have increased 3 nm (from 22 to 12) every two years (from the year 2019 – after applying a two-layer crystal technology in the year 2017), which means that the feature size would be reached 0.8 nm by the year 2037, which increases the design complexity and causes reaching the physical limitation. The area will also have increased about 12-15% every two years (from the year 2019); the small increasing of area can be applied if and only if the density of transistors increases with each generation. The increasing of the density would also be reached the physical limitation by the year 2037, as more density needs more power, which requires more hot generation.

Table 2. Assuming Evolution of Microprocessors: 2015 to 2037

Processor	**Date of introduction**	**Number of transistors (billion)**	**Feature size (nm)**	**Area [mm^2]**
X	2015	5	22	600
X1 (Two-layer crystal)	2017	10	19	600 (each layer)
X2 (Two-layer crystal)	2019	20	17	688 (each layer)
X3 (Two-layer crystal)	2021	40	15	770 (each layer)
X4 (Two-layer crystal)	2023	80	13	882 (each layer)
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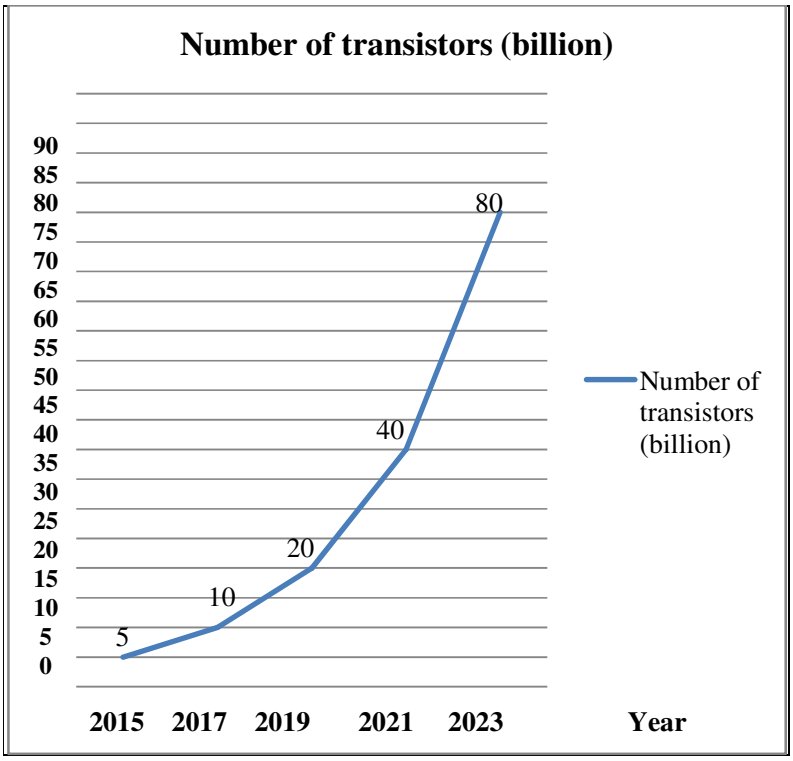
XN-1 (Two-layer crystal)	2035	4000	1	---
XN (Two-layer crystal)	2037	8000	0.8	---

As shown in the table below, several measures of microprocessors technology, such as transistor count, is improving at exponential rate based on Moore's Law (see Figure 5).



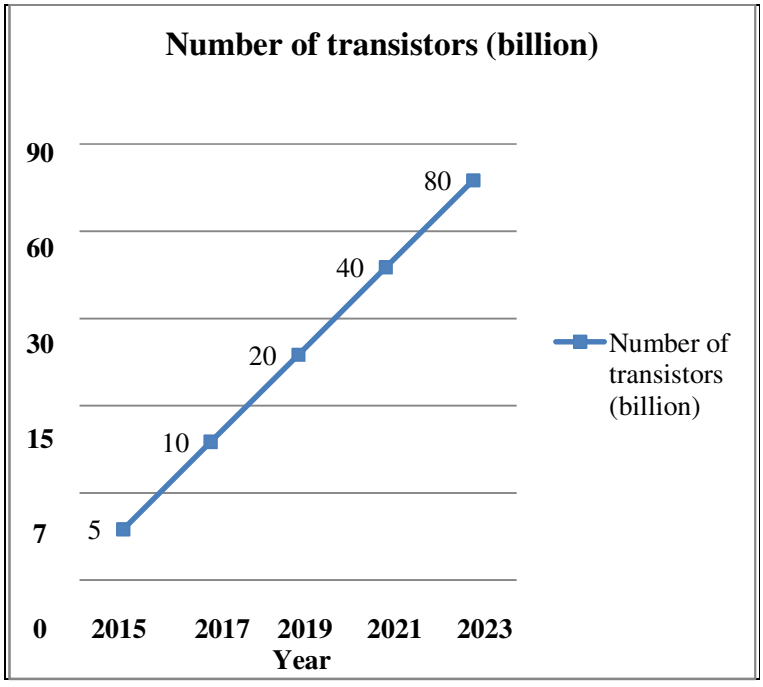


Figure 5. Number of transistors related to Moore's Law

4. CONCLUSION

The Moore's Law states that the number of transistors on a chip would double every two years. As mentioned above some physical limitations affect applying Moore's Law for many years. The problem of applying Moore's law in microprocessor technology as much as possible is still topical research field although it has been studied by the research community for many decades. The main objective of this article is to introduce a new approach as solution for avoiding physical limitation in manufacturing of microprocessors technology and applying Moore's Law for a long time.

The physical limitation will be delayed for few more years by applying the new approach in microprocessor technology, because it consists of two layers, each of which contains the same number of transistors, in this case the transistor count may be doubled every two years based on Moore's Law, which approximately double the microprocessor's performance and speed, with small decreasing of the feature size and small increasing of the die size.

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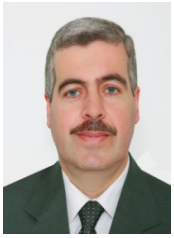

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