STRUCTURAL AND HARDWARE COMPLEXITIES OF MICROPROCESSOR DESIGN ACCORDING TO MOORE'S LAW

Haissam El-Aawar

Associate Professor, Computer Science/Information Technology Departments
Lebanese International University – LIU, Bekaa – Lebanon

ABSTRACT

The most important factors of the microprocessors' development are improvement in the performance and increasing the speed of a microprocessor. Increasing the performance and the speed of a microprocessor majorly depends on the increasing of the number of transistors on a chip, which causes rapidly growing of microprocessor design complexity. The number of transistors should be doubled every 18-24 months related to Moore's Law. The doubling of transistor count affects increasing of the microprocessor design complexities (such as structural, hardware), raising power dissipation, and cost of design effort.

This article presents a proposal to discuss the matter of scaling structural and hardware complexities of a microprocessor design related to Moore's Law. The structural and hardware complexities measurements are presented based on the discussion.

KEYWORDS

Structural Complexity, Hardware Complexity, Microprocessor Design, Transistor Count, Die Size, Density.

1. INTRODUCTION

One of the significant measurements of complexity, which is appearing along the recent past, is the complexity of the algorithms. Although, the algorithmic devices are developed rapidly, they involve a computer system as one of their examples; the structural and hardware complexities are still occupying an important role in computer design, if it is thought to be oriented towards the software/hardware view [1, 2].

The development of the microprocessor's design and integrated circuit (IC) technology has been characterized by Moore's Law during the past five decades. Moore's Law indicates that the number of transistors on a chip would double every 18-24 months [3, 4]; applying Moore's law in the design of the microprocessors makes it more complicated and more expensive. In order to fit more transistors on a chip, the die size must be increasing and/or the density of the transistors must be decreasing. As the feature size on the chip goes down, the number of transistors rises and the design complexity increases.

The development of a microprocessor design takes into consideration the following characteristics: design complexity, feature size, die area, performance, speed, design time and others. These characteristics are generally interdependent. Increasing the number of transistors on a chip increases the size of the chip, the performance and the speed of a microprocessor; more transistors, more clock cycles. Decreasing the feature size increases the number of transistors, the power dissipation and the design complexity [5, 6].

2. HARDWARE AND STRUCTURAL COMPLEXITY MEASUREMENTS

2.1. Hardware complexity measurement

The measurement of the hardware complexity is used to scale the number of components, which are compounded, along any selected level of hardware processing. Any selected level, includes all the involved structures of hardware appearing beyond a specific apparatus. The hardware complexity measurement is defined as [2]:

$$A = | E |\ldots\ldots\ldots (1)$$

where, E is the multitude of the elements emerging in a hierarchal structural diagram.
In order to illustrate, when a processor level is selected (Figure.1), the apparatus complexity measure (ACM) would be defined by the amount of the beyond registers, ALU and the Control Unit.

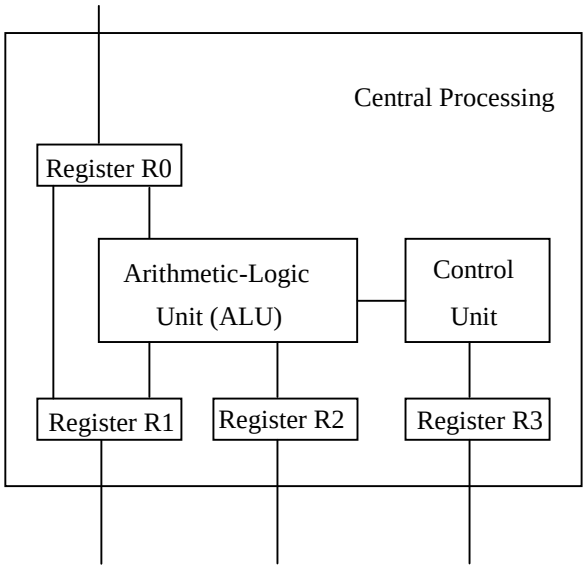

Figure.1.View of a CPU complexity Level, [7].

For the given example of Figure.1: ACM = | E | = 6.
So, the increasing of the number of elements at any processor level increases the hardware complexity of that level.

2.2. Structural complexity measurement

The structural complexity measure scales the data path among the different elementary constituents. This measure needs a process of reformatting the logical diagrams into state transition-based organization. In this organization a convenient abstraction is embodied. Then, the structural complexity of the algorithmic device is the entropy of the incidence matrix. Entropy is used in different areas; in thermodynamics, in software engineering fields, entropy is applied, to design a mathematical model for evaluating software quality, to define complexity measures, etc [1, 2, 8, 9, 10, 11, 12].

The structural complexity can be defined as [2]:

$$S = -U_n \log_2 \frac{U_n}{\alpha.\beta} \text{..... (2)}$$

where, S – is the structure complexity measure.

$$U_n = \sum_L u_l$$

u_l - the quantity or the intercircuit connections of the l-th fragment of the incidence matrix scheme;

α - is the number of elements appearing in the scheme of petri-net diagram.

β - is the number of interconnection among the elements of the state transition scheme.

α x β - matrix size.

The structural complexity measure determines the dimension of the combinations of interconnection paths. It is usually determined in three steps:

1. Current Model scheme is transformed into directed graph.
2. Directed graph is coded as an incidence matrix.
3. The incidence matrix entropy is calculated.

To evaluate the structural complexity measurement, the architecture of a CPU complexity Level shown in Figure 2 should be turned in a directed graph (incidence graph) (see Figure 2), and the incidence graph should be coded as an incidence matrix (see Table 1).

Figure 2 shows the graph incidence obtained from the Figure1. Each component in Figure 1 is assigned by α, such as register R0 is assigned by α1, and the interconnection between this register and register R1 is assigned by β2, etc.

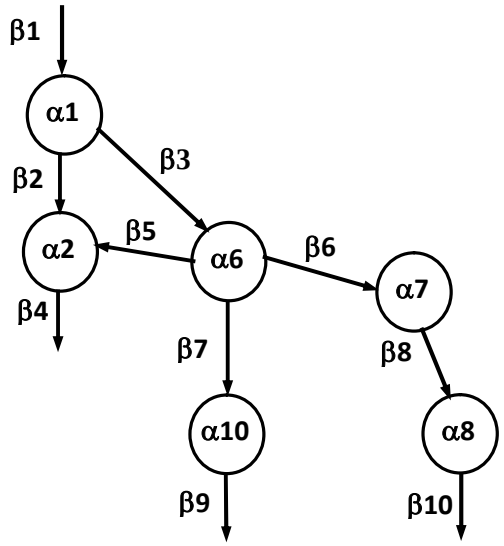

Figure 2. Incidence Graph of the architecture of a CPU complexity Level

Table 1 shows the matrix incidence of the graph incidence shown in Figure 2.

Table 1. Matrix incidence of the incidence graph shown in Figure 2

#	β1	β2	β3	β4	β5	β6	β7	β8	β9	β10
α1	**-1**	**1**	**1**	0	0	0	0	0	0	0
α2	0	**-1**	0	**1**	**-1**	0	0	0	0	0
α3	0	0	**-1**	0	**1**	**1**	**1**	0	0	0
α4	0	0	0	0	0	**-1**	0	**1**	0	0
α5	0	0	0	0	0	0	**-1**	0	**1**	0
α6	0	0	0	0	0	0	0	**-1**	0	**1**

From Figure 2 and Table 1 the following values are founded: Un = 16, α = 6, β = 10
Using equation (2) the structural complexity measurement of this architecture is:

$S \approx 30.5102$ BU (BU – stands for binary unit).

3. PHYSICAL LIMITATION OF INCREASING THE NUMBER OF THRANSISTORS

Raising the number of transistors will be limited due to several limitations, such as increasing the density, the die size, decreasing the feature size, the voltage [13, 14, 15].

Since the surface area of a transistor determines the transistor count per square millimeter of silicon, the transistors density increases quadratically with a linear decrease in feature size [16]. The increase in transistor performance is more complicated. As the feature sizes shrink, devices

shrink quadratically in the horizontal and vertical dimensions. A reduction in operating voltage to maintain correct operation and reliability of the transistor is required in the vertical dimension shrink. This combination of scaling factors leads to a complex interrelationship between the transistor performance and the process feature size.

The hardware complexity rises due to the shrinking of the pixel size and the increasing of the density. If the pixel size shrinks double and the density increases double every two years according to Moore's Law, the physical limitation will definitely appear in few years, which means that it will be very difficult to apply Moore's Law in the future. Some studies have shown that physical limitations could be reached by 2018 [17] or 2020-2022[18, 19, 20, 21].

Applying the Moore's Law by doubling the number of transistors every two years increases the speed and performance of the processor and causes increasing the processor's hardware complexity (see Table 2) and structural complexity, which will be limited after a few years [22, 23, 24, 25].

Table 2. Complexity of microchip and Moore's Law

Year	**Microchip Complexly Transistors**	**Moore's Law: Complexity: Transistors**
1959	1	$2^0 = 1$
1964	32	$2^5 = 32$
1965	64	$2^6 = 64$
1975	64,000	$2^{16} = 64{,}000$

Table 3 shows the apparatus complexity measurement of different microprocessors from 1971 till 2012. As shown in this table the number of transistors increases with every new type of processor, which causes increasing the structural complexity.

Table 3. Evolution of Microprocessors and Apparatus Complexity Measurement: 1971 to 2012

Manufacturer	**Processor**	**Date of introduction**	**Number of transistors (Apparatus Complexity)**	**Area [mm^2]**
Intel	Intel4004	1971	2,300	12
	Intel8008	1972	3,500	14
	Intel8080	1974	4,400	20
	Intel8085	1976	6,500	20
	Intel8086	1978	29,000	33
	Intel80286	1982	134,000	44
	Intel80386	1985	275,000	104
	Intel80486	1989	1,180,235	173

	Pentium	1993	3,100,000	294
	Pentium Pro	1995	5,500,000	307
	Pentium II	1997	7,500,000	195
	Pentium III	1999	9,500,000	128
	Pentium 4	2000	42,000,000	217
	Itanium 2 McKinely	2002	220,000,000	421
	Core 2 Duo	2006	291,000,000	143
	Core i7 (Quad)	2008	731,000,000	263
	Six-Core Core i7	2010	1,170,000,000	240
	Six-Core Core i7/8-Core Xeon E5	2011	2,270,000,000	434
	8-Core Itanium Poulson	2012	3,100,000,000	544
MIPS	R2000	1986	110,000	80
	R3000	1988	150,000	56
	R4000	1991	1,200,000	213
	R10000	1994	2,600,000	299
	R10000	1996	6,800,000	299
	R12000	1998	7,1500,000	229
IBM	POWER3	1998	15,000,000	270
	POWER4	2001	174,000,000	412
	POWER4+	2002	184,000,000	267
	POWER5	2004	276,000,000	389
	POWER5+	2005	276,000,000	243
	POWER6+	2009	790,000,000	341
	POWER7	2010	1,200,000,000	567
	POWER7+	2012	2,100,000,000	567

4. INCREASING THE DIE SIZE

In order to avoid the physical limitations mentioned above this article suggests, as a solution, a new approach of constructing a chip with die size, which contains free spaces for allowing to apply the Moore's Law for a few years by doubling the number of transistors on a chip without

touching the voltage, the feature size and the density, in this case only the hardware and structural complexities will be raised.

Let us assume a microprocessor (let's say X) has the following specifications: date of introduction – 2015, one-layer crystal square of transistors, transistor count (number of transistors) – 3 billion, pixel size (feature size) – 0.038 micron, die size (area) – 2400 mm2: for transistors – 600 mm2 and free space – 1800 mm2 (see Figure. 3).

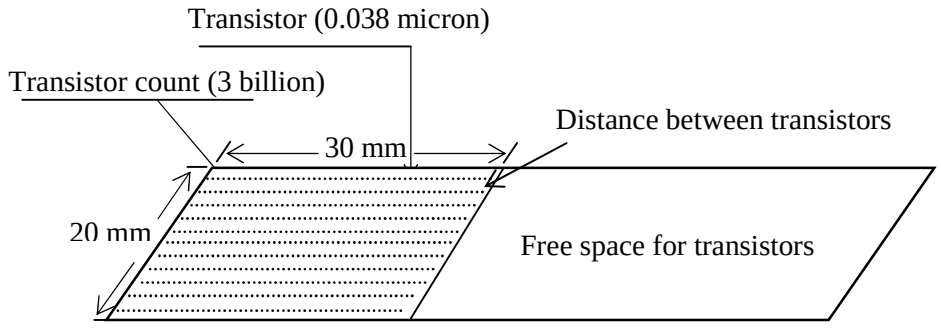

Figure 3. Crystal Square of Transistors

By applying this approach the number of transistors will be doubled after two year (2017) without touching the feature size, die size, voltage and density. In 2017 year a new microprocessor (let's say X1) will have the following specifications: date of introduction – 2017, one-layer crystal square of transistors, transistor count (number of transistors) – 6 billion, pixel size (feature size) – 0.038 micron, die size (area) – 2400 mm^2: for transistors – 1200 mm^2 and free space – 1200 mm^2 and so on. The hardware and structural complexities of the microprocessors will be increased related to the number of transistors. When the number of transistors would occupied all the free space, the architects can decrease the feature size and increase the density without touching the die size (see Table 4).

Table 4. Assuming Evolution of Microprocessors: 2015 to 2021

Microprocessor	**Date of introduction**	**Number of transistors (billion)**	**Feature size (nm)**	**Area [mm^2]**	
				For Transistors	**Free space**
X	2015	3	38	2400	
				600	1800
X1	2017	6	38	1200	
				1200	1200
X2	2019	12	38	2400	
				2400	
X3	2021	24	28	2400	

As shown in the table above, several measures of microprocessors technology, such as hardware complexity can be changed (increased) during few years; of course the structural complexity will be increased due to the raising of the interconnection between the components of the microprocessors, while the others can be fixed.

5. CONCLUSION

Applying Moore's law in microprocessor technology as much as possible is still a topical research field although it has been studied by the research community for many decades.

The aim of this article is to find a suitable solution for avoiding physical limitation in manufacturing of microprocessors technology and applying Moore's Law for a long time.

As it is mentioned in the previous sections, the physical limitations could be reached by 2018 or 2022. Applying the new approach in microprocessor technology will delay the physical limitation for few more years, because it doubles the number of transistors every two years based on Moore's Law, with increasing the die size, the hardware complexity at the transistor level and the structural complexity at the processor level, without decreasing of the feature size and increasing of the density.

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REFERENCES

[1] Cherkaskyy M.V. and Haissam El-Aawar, "Optimization of Complexity of Software/Hardware of Microprocessor Level", Proceedings of CAD essentials, implementation and Applications Symposium", Vol: 2, p: 200-201, 1997, Ukraine.

[2] Haissam El-Aawar; "Theory of Complexity of Algorithmic Devices", Proceedings of the 14th International Conference on Computer Theory and Applications ICCTA' 2004. Alexandria, Egypt, 2004.

[3] Gorden E. Moore, "cramming more Components onto Integrated Circuits", Electronics, Vol. 38, No. 8, April 19, 1965.

[4] Jane Laudon, Kenneth Laudon, "Essentials of Management Information Systems", Chapter 4: IT Infrastructure: Hardware and Software, 10th ed., 2012.

[5] Steve Gilheany, "Evolution of Intel Microprocessors: 1971 to 2007". http://www.iro.umontreal.ca/~aboulham/F2880/EvolutionMicroprocessor1971a2007.

[6] Wolfgang Arden, "Future roadblocks and solutions in silicon technology as outlined by the ITRS roadmap" in Mterials Science in Semiconductor Processing, vol.5 issue 4-5 August – October, 2002, pp. 313-319.

[7] John P. Hayes, " Digital System Design and Microprocessors", McGraw-Hill press. 1987, USA.

[8] Meyers R.A. (ed.). Encyclopedia of Physical Science & Technology. 3rd edition. Academic Press. New York 2001.

[9] Von Foester H. The Cybernetics of Cybernetics. 2nd edition. Future System Inc., Minneapoli, 1995.

[10] Ya. A. Kogan, A.A. Korshunov, and I.B. Muchnik, "Algorithm for Structural Analysis of The Measurement Path of Computer System Performance Parameters", Automatica and Telemekhanika, No. 3, pp. 161-167, March, 1984.
[11] David Feldman, "A Brief Introduction to: Information Theory, Excess Entropy and Computational Mechanics", April, 1998.
[12] Matthias Dehmer, "Information processing in complex networks: Graph entropy and information functional", Applied Mathematics and Computation 201, pp. 82-94, 2008.
[13] Hasan S., Humaria, Asghar M.,"Limitation of Silicon Based Computation abd Future Prospects" in Proceedings of Second International Conference on Communication Software and Networks, 2010. ICCSN'10, pp. 599-561.
[14] Robert W. Keyes, "Physical limits of silicon transistors and circuits", September 2005.
[15] F. Morals, L. Torres, M. Robert, D. Auvergne, "Estimation of layout densities for CMOS digital circuits", Proceeding International Workshop on Power and Timing Modeling Optimization Simulation (PATMOS'98), pp. 61-70, November 1998, Lyngby, Danemark.
[16] John L. Hennessy and David A. Patterson, "Computer Architecture, A Quantitative Approach", 5th ed., pp. 17-26, 2011.
[17] Jan M. Rabaey, "Design at the end of Silicon Roadmap", Keynotes Address III, University of California, Berkelev, IEEE, ASP-DAC 2005.
[18] Ahmad, Khaled; Schuegraf, Klaus, "Transistor Wars: Rival architecture face off in a bid to keep Moore's Law alive", IEEE Spectrum: 50, November 2011.
[19] Brooke Crothers, "End of Moore's Law: it's not just about physics", August 28, 2013.
[20] Robert Colwell, "The Chip Design Game at the End of Moore's Law", Hot Chips, August 2013. http://news.cnet.com/8301-1001_3-57600373-92/end-of-moores-law-its-not-just-about-physics/
[21] Joel Hruska, "Intel's former chief architect: Moore's law will be dead within a decade", August 30, 2013. http://www.extremetech.com/computing/165331-intels-former-chief-architect-moores-law-will-be-dead-within-a-decade.
[22] Mike Stojcev, Teufic Tokic and Ivan Milentijevic, "The Limits of Semiconductor Technology and Oncoming Challenges in computer Micrarchitectures and Architectures", Ser.: Elec.Energ. vol. 17, December 2004, pp. 285-312.
[23] Suleiman Abu Kharmeh, Kerstin Eder, and David May. Complexity of Hardware Design and Model-Checking: An Asymptotic Analysis of State-Machine Metrics. Technical report, University of Bristol, March 2012.
[24] Cyrus Bazeghi, Francisco J. Mesa-martinez, Brian Greskamp , Josep Torrellas, Jose Renau, "µComplexity: Estimating Processor Design Effort", International Symposium on Microarchitecture, 2005.
[25] Pradip Bose David H. Albonesi Diana Marculescu, "Complexity-Effective Design", Proceeding International Workshop on Complexity-Effective Design, Madison, Wisconsin, June 5, 2005.

AUTHOR

Haissam El-Aawar is an Associate Professor in the Department of Computer Science and Information Technology at the Lebanese International University where he has been a faculty member since 2009. Haissam completed his Ph.D. and M.Sc. degrees at the State University "Lviv Polytechnic" in Ukraine. His research interests lie in the area of Artificial Intelligence, theory of complexity, microprocessors evaluation, CISC- and RISC-architectures, robotics control, mobility control and wireless communication.