

Design and FPGA Implementation of DDR3 SDRAM Controller for High Performance

Shabana Aqueel* and Kavita Khare**

* Dept. of Electronics and Communication , M.A.N.I.T, Bhopal, India

** Dept. of Electronics and Communication , M.A.N.I.T, Bhopal, India

Abstract—*The demand for faster and cheaper memories has been increasing by the day. Hence, these memory devices are rapidly developing to give high density and high memory bandwidths. However, with the increase in technology, complexity of instructions to control the memory devices also increases. In this paper, a specific purpose DDR3 Controller is described. This paper presents the overall architecture of the DDR3 Controller. Also the advantages of DDR3 over DDR2 and DDR are discussed.*

Keywords—*DDR3; VHDL; Xilinx; FPGA*

I. INTRODUCTION

The DDR3 SDRAM is a high speed synchronous dynamic random access memory with eight banks [1]. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. According to JEDEC standards DDR3 runs at a frequency between 800 MHz to 1666 MHz , which is double that of frequency of DDR2. The associated interface techniques used by DDR3 SDRAM is not directly compatible with any earlier type of random access memory (RAM) due to different signaling voltages, timings, and other factors. The primary benefit of DDR3 SDRAM over its immediate predecessor, DDR2 SDRAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth [11] or peak data rates [6]. With two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed in megabytes per second (MB/s). In addition, the DDR3 standard permits chip capacities of up to 8 gigabits.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in capture at the DDR3 SDRAM input receiver. DQS is centre-aligned with data for WRITES. The read data is transmitted by the DDR3 SDRAM and is edge-aligned to the data strobe [7]. The DDR3 SDRAM operates from a differential clock (CK and CK#).

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of ACTIVATE command which is followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The architecture of DDR3 SDRAM allows pipelining along with self- refresh mode, power saving and power down mode.

This module has been implemented in RTL using VHDL [5]. The focus of this work is to implement a behavioural model for DDR3 SDRAM and also implement it on the Xilinx [3] Spartan series FPGA.

II. TOP MODULE

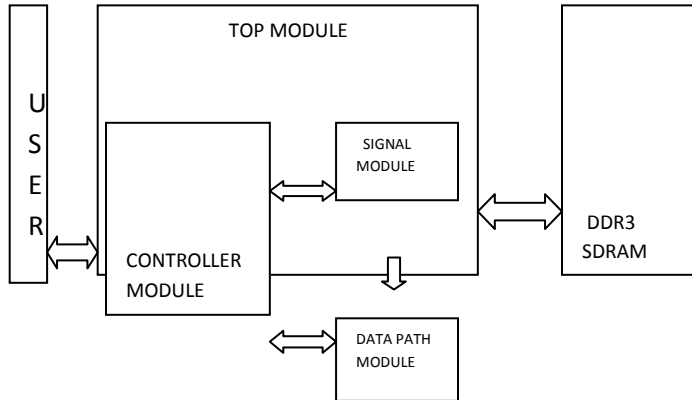


Figure 1. Top Module

The top module of the DDR3 SDRAM Controller is shown in Figure 1. It consists of 3 modules, the main controller module, the signal module and the data path module.

The user sends the data to be written onto or read from the DDR3 SDRAM along with the memory location (address). The main controller module has two state machines and a refresh counter. The signal generation module generates the address and command signals required for DDR3. The data path module performs the data latching and dispatching of the data between the processor and DDR3.

III. FUNCTIONAL DESCRIPTION

A. Initialization

DDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified would result in undefined operation.

After the power supply has been applied the RESET# should be LOW, so as to ensure the outputs are disabled(High-Z). After the power is stable, RESET# should still be maintained low for 200us to begin the initialization process. After the specified delay CKE must be LOW 10ns prior to RESET# transitioning HIGH. After RESET# transitions HIGH, 500us of time should elapse with CKE LOW. After the CKE LOW time, CKE is brought synchronously HIGH while only NOP or DES commands are to be issued. Stable clocks have to be present and should be valid for atleast 10ns and then ODT must be driven LOW or HIGH atleast tIS prior to CKE being registered HIGH. Once CKE is registered HIGH, it must be continuously registered HIGH until full initialization process is complete. A certain tXPR has to be satisfied before issuing MSR(LOAD MODE) command to MR2. Then an MRS command is issued to MR3 and then to MR1(including enabled DLL and configured ODT). Later an MRS command to MR0 is issued including DLL REST command. Finally calibration of Rtt and Ron is to be

done, by issuing ZQCL command. Prior to normal operation, tZQinit and tDLLK must be satisfied [7][10].

B. Register Definition

There are basically four mode registers in DDR3 SDRAM namely MR0, MR1, MR2 and MR3. Figure 2. shows

MR0 definition where it defines the burst length by MR0[1:0]. The eighth bit is used to change the value of DLL RESET. The PD (Precharge) bit is applied only when precharge power-down mode is used. CAS Latency is the delay in clock, cycles, between internal READ command and the availability of the first bit of output data.

The definition for MR1 is described in Figure 3. This mode register controls additional functions and features such as Q OFF (OUTPUT DISALBE), TQDS (Termination data strobe), WRITE LEVELING (which is used during initialization to deskew the DQS for better integrity).

MR2 further controls functions like CAS WRITE Latency (It is the delay in clock cycles from the releasing of the internal write to the latching of the first data in), AUTO SELF REFRESH (ASR), SELF- REFRESH TEMPERATURE (SRT). This is shown in Figure 4.

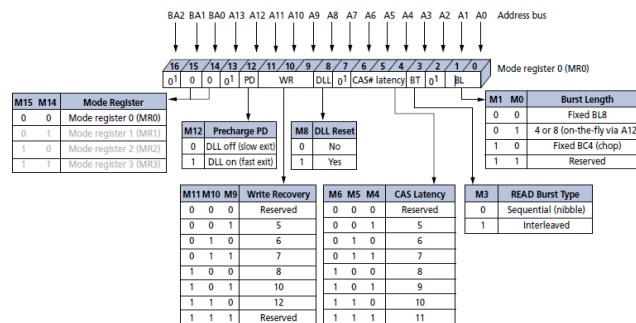


Figure 2. MR0 Definition

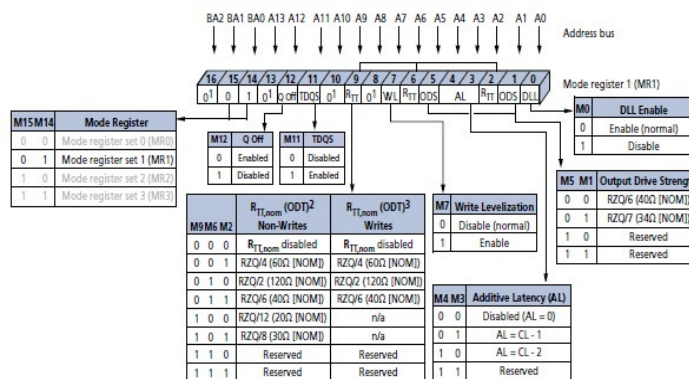


Figure 3. MR1 Definition

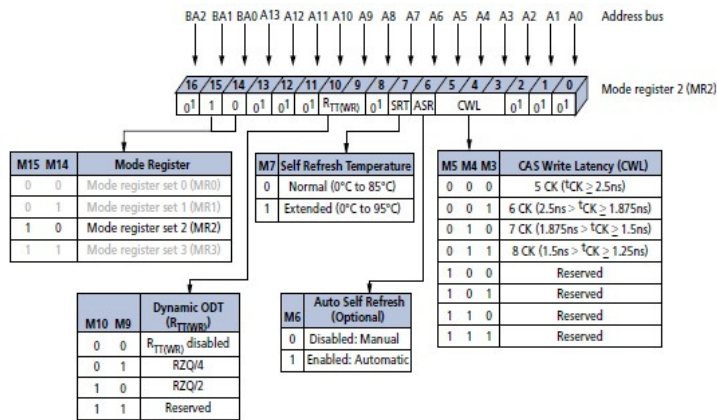


Figure 4. MR2 Definition

The MR3 is current defined as the MULTIPURPOSE REGISTER. Its function is to output a predefined system timing calibration bit sequence. This definition is illustrated in Figure 5.

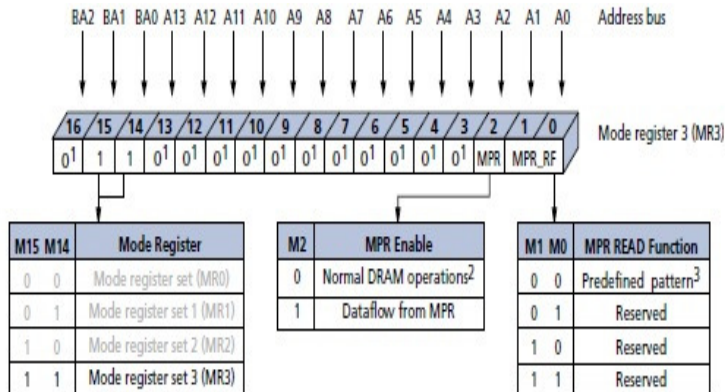


Figure 5. MR3 Definition

C. DDR3 Commands

Table 1. illustrates the various commands issued by the controller. The commands are defined by the states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.

Table 1.DDR3 Commands

Function	Symbol	Prev. Cycle	Next Cycle	CS#	RAS#	CAS#	WE#	BA [2:0]	An	A12	A10	A[11, 9:0]	
MODE REGISTER SET	MRS	H	H	L	L	L	L	BA	OP code				
REFRESH	REF	H	H	L	L	L	H	V	V	V	V	V	
Self refresh entry	SRE	H	L	L	L	L	H	V	V	V	V	V	
Self refresh exit	SRX	L	H	H	V	V	V	V	V	V	V	V	
Single-bank PRECHARGE	PRE	H	H	L	L	H	L	BA	V	V	L	V	
PRECHARGE all banks	PREA	H	H	L	L	H	L	V		V	H	V	
Bank ACTIVATE	ACT	H	H	L	L	H	H	BA	Row address (RA)				
WRITE	BL8MRS, BC4MRS	WR	H	H	L	H	L	L	BA	RFU	V	L	CA
	BC4OTF	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA
	BL8OTF	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA
WRITE with auto precharge	BL8MRS, BC4MRS	WRAP	H	H	L	H	L	L	BA	RFU	V	H	CA
	BC4OTF	WRAP54	H	H	L	H	L	L	BA	RFU	L	H	CA
	BL8OTF	WRAP58	H	H	L	H	L	L	BA	RFU	H	H	CA
READ	BL8MRS, BC4MRS	RD	H	H	L	H	L	H	BA	RFU	V	L	CA
	BC4OTF	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA
	BL8OTF	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA
READ with auto precharge	BL8MRS, BC4MRS	RDAP	H	H	L	H	L	H	BA	RFU	V	H	CA
	BC4OTF	RDAP54	H	H	L	H	L	H	BA	RFU	L	H	CA
	BL8OTF	RDAP58	H	H	L	H	L	H	BA	RFU	H	H	CA
NO OPERATION	NOP	H	H		H	H	H	V	V	V	V	V	
Device DESELECTED	DES	H	H	H	X	X	X	X	X	X	X	X	
Power-down entry	PDE	H	L	L	H	H	H	V	V	V	V	V	
Power-down exit	PDX	L	H	L	H	H	H	V	V	V	V	V	
				H	V	V	V						
ZQ CALIBRATION LONG	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ CALIBRATION SHORT	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

IV. DDR3 SDRAM CONTROLLER BLOCK

Before normal memory access can be performed DDR3 SDRAM should be initialized first. So, the controller block consists of two FSMs (Finite state machines), one is the initialization FSM and the other is the command FSM. The initialization involves the predefined steps described in section III.A. of this article. The command FSM handles the read, write and refresh of DDR3. The initialization FSM consists of all the possible states to be encountered during initialization. Once the initialization is done the DDR3 SDRAM is ready for either writing data into or reading data from its store. The command FSM mainly contains two states READ and WRITE state, besides, continuous REFRESH state (as it's a dynamic RAM). When either of the states are met a sequence of internal signals are generated corresponding to that state.

All the rows are in the “closed” status after the DDR3 initialization. The rows need to be “opened” before they can be accessed. The Command decode logic block shown in Figure 6. accepts the user commands from the local interface and the Command application logic block decodes them to generate a sequence of internal memory commands depending on the current command and the status of banks and rows[2]. The intelligent bank management built in the controller tracks the open/close status of every bank and stores the row address of every opened bank. The controller designed implements a command pipeline to improve throughput. With pipelining capability, the next command in the queue is decoded while the current command is present at the memory interface.

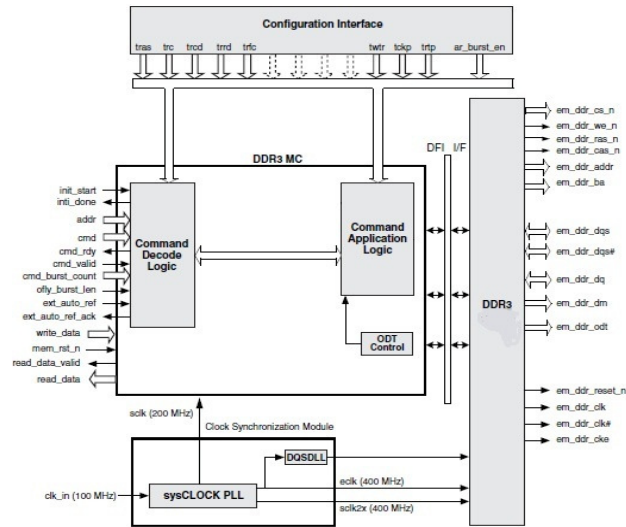


Figure 6. DDR3 SDRAM Controller Block Diagram

V. TIMING DIAGRAMS

Figure 7. and 8. are the read cycle and write cycle timing diagrams.

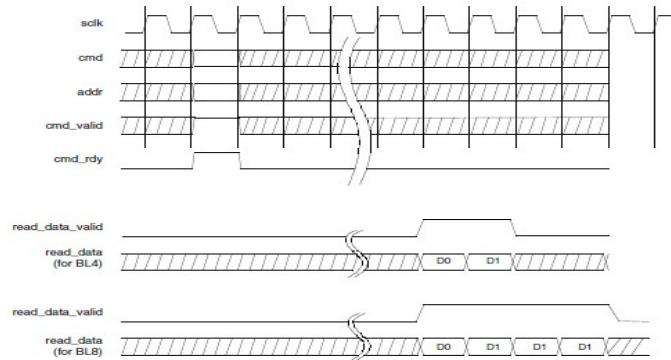


Figure 7. Read timing diagram for burst length 4 and 8



Figure 8. Write timing diagram for a one clock and two clock write data delay

When the read command is accepted, the DDR3 SDRAM Controller access the memory to read the addressed data and brings the data back to the local user interface. Once the read data is available on the local user interface, the memory controller asserts the read_data valid signal to indicate that the valid read is on the read_data bus. The write command is accepted along with cm_valid signal and the address. Then the controller asserts the datain_rdy signal when it is ready to receive the write data from the user to write into the memory. Once datain_rdy is asserted, the core expects the valid data on the write_data bus after one or two clock cycles after the datain_rdy signal is asserted. The write data delay is programmable.

VI. DDR3 FEATURES COMPARISON

DDR3 is the next-generation, high-performance solution for CPU systems it pushes the envelope in key areas like power consumption, signaling speeds, and bandwidth, bringing new levels of performance to desktop, notebook, and server computing. DDR3 offers a substantial performance improvement over the previous DDR2 and DDR memory systems. One of the main DDR3 features include improved signal integrity so as to have higher performance without an undue burden on the system designer. Table 2. compares some differences between DDR3 and the previous two [9].

Table 2. DDR3 Feature Comparison

Feature	DDR	DDR2	DDR3
Data Rate	200-400 Mbps	400-800 Mbps	800-1600 Mbps
Burst Length	BL=2,4,8	BL=4,8	BL=4,8
No. of Bank	4 banks	512Mb : 4 Banks 1 Gb : 8 Banks	512Mb/1 Gb : 8 Banks
Prefetch	2 bits	4 bits	8 bits
CL/tRCD/tRP	15/15/15 ns	15/15/15 ns	12/12/12 ns
Source sync.	Bi-directional DQS (single ended Default)	Bi-directional DQS (Single/Diff. Default)	Bi-directional DQS (Differential Default)
Vdd/Vddq	2.5+/- 0.2 V	1.8+/- 0.1 V	1.5+/- 0.075 V
Reset	No	No	Yes
ODT	No	Yes	Yes

VII. SIMULATION RESULTS

In this work we have designed a high speed DDR3 SDRAM Controller using Micron's DDR3 memory model (MT41J128M8) [8]. The controller is written in VHDL [5] language. The tool used to synthesize it and verify is Xilinx[4]. A complete task file including all operations was set up. Then, all mode registers were initialized. Finally, test bench with several testcases were set up to verify the expected results. The Figure 9. shows the RTL schematic of the top module and the controller respectively.

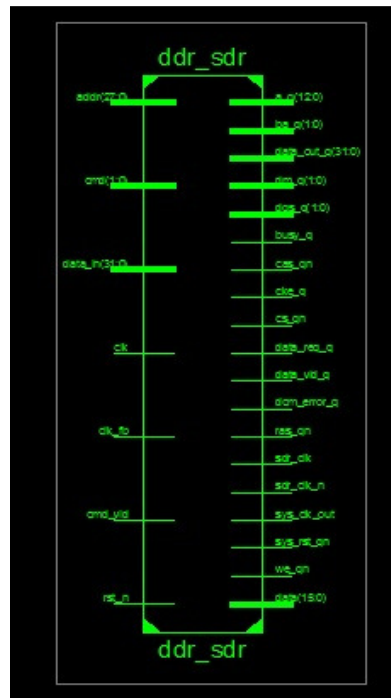


Figure 9. RTL Schematic of the top module

Figure 10. shows the result of our designed controller.

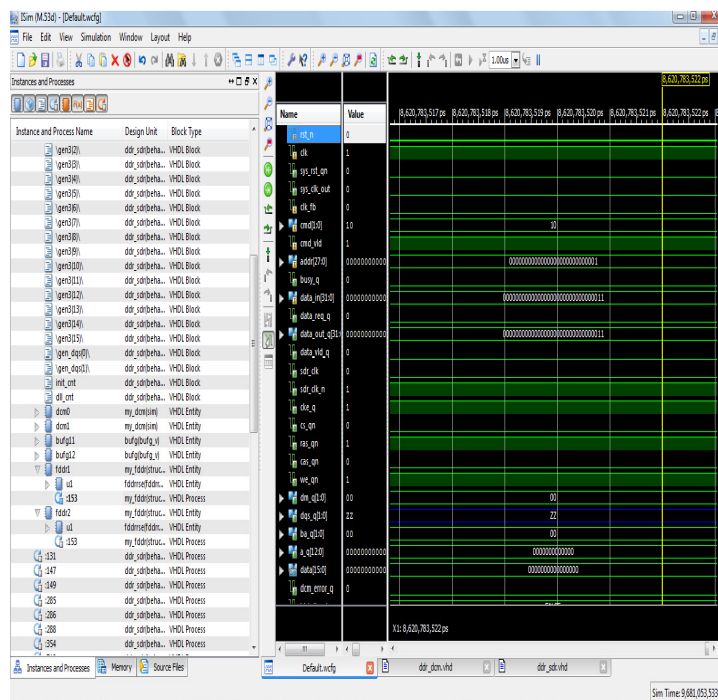


Figure 10. Result of our simulation

HDL Synthesis Report of the core designed is as follows

Macro Statistics:

Adders/Subtractors : 2
2-bit subtractor : 1
5-bit subtractor : 1
Counters : 4
14-bit down counter : 1
3-bit down counter : 1
4-bit down counter : 1
8-bit down counter : 1
Registers : 66
1-bit register : 46
13-bit register : 5
16-bit register : 3
2-bit register : 4
3-bit register : 3
32-bit register : 3
5-bit register : 1
6-bit register : 1
Comparators : 3
3-bit comparator greater : 1
4-bit comparator greater : 1
8-bit comparator greater : 1
Tristates : 18
1-bit tristate buffer : 18
Registers : 249
Flip-Flops : 249
Shift Registers : 35
2-bit shift register : 32
3-bit shift register : 2
5-bit shift register : 1

Device utilization summary:

Selected Device : 3s50pq208-5
Number of Slices : 210 out of 768 27%
Number of Slice Flip Flops : 304 out of 1536 19%
Number of 4 input LUTs : 263 out of 1536 17% Number used as logic : 228
Number used as Shift registers : 35
Number of IOs : 146
Number of GCLKs : 3 out of 8 37%
Number of DCMs : 2 out of 2 100%

The above experimental results clearly validate the expected performance of the proposed custom purpose DDR3 controller architecture.

VIII. CONCLUSIONS

The design study shows that high-performance and large lookup table circuits can be implemented using low-cost state-of-the-art FPGA and DDR3 technology. The proposed DDR3 SDRAM Controller design has been verified by the exhaustive functional verification. We examined the performance of the design by generating several testcases and noting down the time taken by the designed DDR3 Controller in finishing them. In most of the scenario the throughput of the design was close to the theoretical maximum.

REFERENCES

- [1]. DDR3 SDRAM Specification (JESD79-3A), *JEDEC Standard, JEDEC Solid State Technology Association*, Sept. 2007.
- [2]. “Double Data Rate (DDR3) IP Core User’s Guide”, *Lattice Semiconductors Corporation*, Dec. 2010.
- [3]. <http://www.xilinx.com>
- [4]. “High-Performance DDR3 SDRAM Interface in Virtex-5 Devices”, *Xilinx, XAPP867 (v1.0)*, Sept 24, 2007.
- [5]. J. Bhasker “A VHDL Primer”, *3rd Edition*, *Pearson Education*
- [6]. www.altera.com/literature/ug/ug_altmemphy.pdf, External DDR Memory PHY Interface Megafunction User Guide (ALTMEMPHY), accessed on 23 Feb. 2009
- [7]. Micron 1GB DDR3 SDRAM , *Micron Technology Inc.* , 2006.
- [8]. <http://www.micron.com>
- [9]. Vikky Lakhmani, Nusrat Ali, Dr. Vijay Shankar Tripathi, “AXI Compliant DDR3 Controller”, *Second International Conference on Computer Modeling and Simulation*, 2010, pp 391-395.
- [10]. DDR3 Power-up, Initialization, and Reset, Technical Note, TN-41-07, Micron.
- [11]. Xin Yang, Sakir Sezer, John McCanny, Dwanyne Burns, “DDR3 Based Look-up circuit for High Performance network Processing”, *IEEE* 2009, pp 351-354.