

LEVEL SHIFTER DESIGN FOR LOW POWER APPLICATIONS

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ABSTRACT

With scaling of V_t sub-threshold leakage power is increasing and expected to become significant part of total power consumption. In present work three new configurations of level shifters for low power application in $0.35\mu\text{m}$ technology have been presented. The proposed circuits utilize the merits of stacking technique with smaller leakage current and reduction in leakage power. Conventional level shifter has been improved by addition of three NMOS transistors, which shows total power consumption of 402.2264pW as compared to 0.49833nW with existing circuit. Single supply level shifter has been modified with addition of two NMOS transistors that gives total power consumption of 108.641pW as compared to 31.06nW . Another circuit, contention mitigated level shifter (CMLS) with three additional transistors shows total power consumption of 396.75pW as compared to 0.4937354nW . Three proposed circuit's shows better performance in terms of power consumption with a little conciliation in delay. Output level of 3.3V has been obtained with input pulse of 1.6V for all proposed circuits.

KEYWORDS

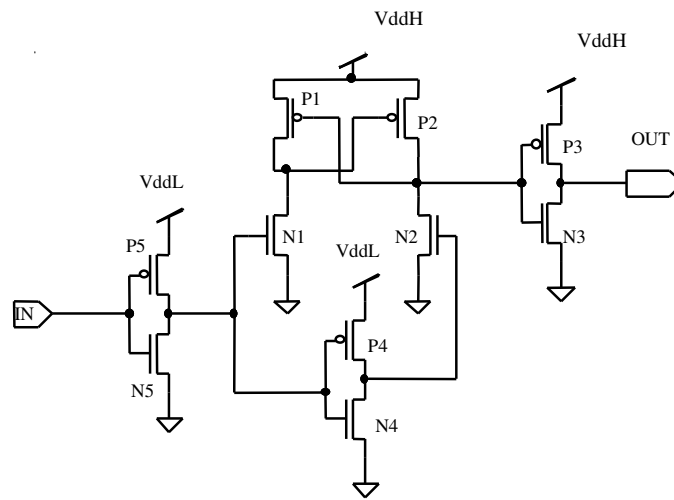
CMOS, delay, level shifter, power consumption and stacking technique.

1. INTRODUCTION

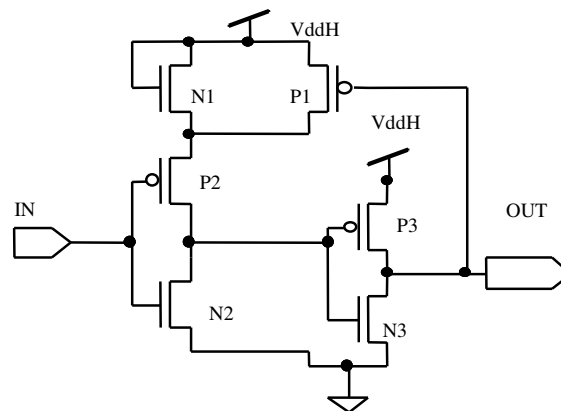
With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become major design consideration for VLSI circuits and system [1], [2]. With increase in power consumption, reliability problem also rises and cost of packaging goes high [3]. Power consumption in VLSI circuit consists of dynamic and static power consumption. Dynamic power has two components i.e. switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [4]. The static power of CMOS circuits is determined by the leakage current through each transistor. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance [4]. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage currents originate [5]. With the development of technology towards submicron region leakage power has become significant component of total power dissipation [6], [7]. Static power component of power consumption must be given due consideration if current trends of scaling of size and supply voltage need to be sustained.

In System on chip (SoC) design, different parts like digital, analog, passive component are fabricated on a single chip and needs different voltages to achieve optimum performance. Level converters are used to convert the logic signal from one voltage level to other level and are the significant circuit component in VLSI systems. Level shifters are also important circuit component in multi voltage systems and have been used in between core circuits and I/O circuit. Various design for level shifters have been reported in literature with single and dual supply [8]-

[16]. Conventional level shifter using 10 transistor with low voltage supply V_{ddL} and high voltage supply V_{ddH} has been reported [8], [10], [11], [12]. The conventional level shifters have disadvantages of delay variation due to different current driving capabilities of transistors, large power consumption and failure at low supply core voltage V_{ddL} [11]. The single supply level shifter allows communication between modules without adding any extra supply pin. Single supply level shifters have advantages over dual supply in terms of pin count, congestion in routing and overall cost of the system. Another benefit of single supply is flexible placement and routing in physical design. Single supply level shifters dissipate higher leakage power due to increase in leakage currents when input supply level is lower or V_{ddH} is higher than input supply level by more than V_{th} [12]. Contention mitigated level shifter (CMLS) using 12 transistors with reduced power consumption and delay than conventional level shifter has been reported [13]. Conventional level converters using bootstrapped gate drive to reduce voltage swings and power consumption has been reported [8]. In [14] method to modify the threshold voltage for reduce power consumption using dual supply voltage has been reported.



(a)



(b)

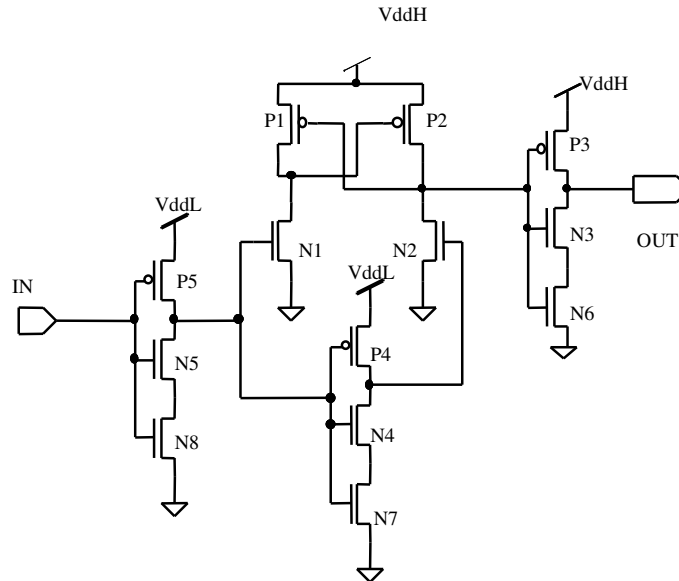


Figure.2 Conventional level shifter with stacking technique

Fig.3 shows modified single supply level shifter with stacking technique using two additional NMOS [N4-N5] transistors. NMOS transistors [N2-N3] with gate length $0.35\mu\text{m}$ and width $1.0\mu\text{m}$ have been replaced by four transistors [N2-N5] same gate length and width of $0.5\mu\text{m}$. Gate lengths of all transistors have been taken as $0.35\mu\text{m}$. Width (W_n) for [N1-N5] has been taken as $0.5\mu\text{m}$, preserving total width $1.0\mu\text{m}$. Normal values of widths $2.5\mu\text{m}$ have been taken for PMOS [P1-P3]. Supply voltage V_{ddH} has been taken as 3.3V .

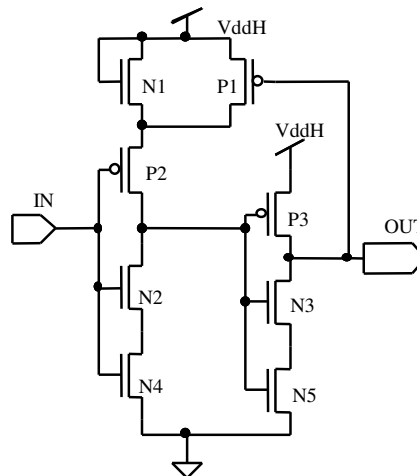


Figure.3 Single supply level shifter with stacking technique

Fig.4 shows modified contention mitigated level shifter employing stack forcing with addition of three NMOS transistors [N6-N8]. NMOS transistors [N3-N5] with gate length $0.35\mu\text{m}$ and width $1.0\mu\text{m}$ have been replaced by six transistors [N3-N8] with same gate length and width of $0.5\mu\text{m}$ preserving the total width $1.0\mu\text{m}$. Gate lengths of all transistors have been taken as $0.35\mu\text{m}$. Normal values of widths 1.0 and $2.5\mu\text{m}$ have been taken for NMOS [N1&N2] and PMOS [P1-P7] transistors respectively. Supply voltages V_{ddH} and V_{ddL} have been taken as 3.3V and 2.2V respectively. Level shifter circuits shown in Fig.1 also have been designed with gate

lengths of $0.35\mu\text{m}$ and widths of PMOS & NMOS have been taken as $2.5\mu\text{m}$ & $1.0\mu\text{m}$ respectively.

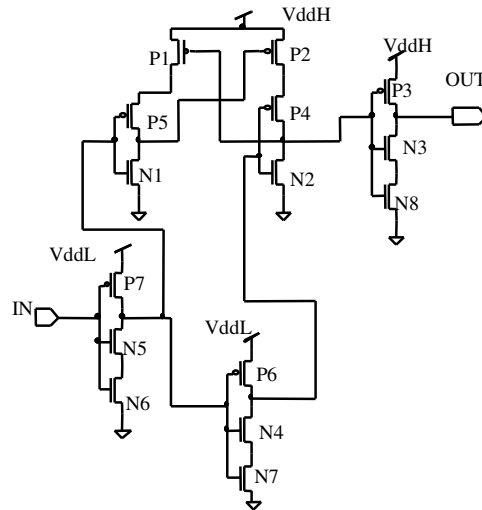


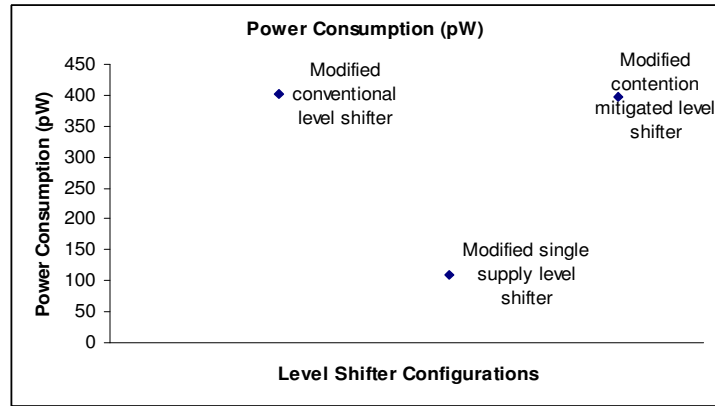
Figure.4 Contention mitigated level shifter with stacking technique

3. RESULTS AND DISCUSSIONS

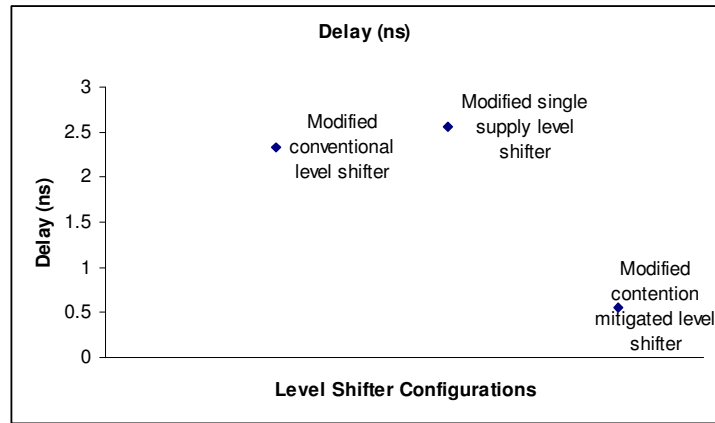
Modified level shifter circuits [Fig.2-4] with stack forcing have been presented and simulated in $0.35\mu\text{m}$ technology using TSMC0.35 model file. Table I shows the results for existing level shifter and Table II shows results of modified circuits. Modified conventional level shifter gives power consumption of 402.2264pW as compared to 0.49833nW with existing conventional circuit. Modified single supply level shifter shows 108.641pW compared to 31.06nW with existing circuit. Finally, the modified CMLS shows 396.75pW as compared to 0.4937354nW without modifications. Results show that power consumption has been reduced in modified circuits with application of stacking technique. Delays of existing and proposed circuits also have been obtained and shown in Table I&II. Fig.6 (a) and (b) shows power consumptions and delay of proposed level shifters circuits. For comparisons existing circuits have been simulated with same set of parameters as for proposed circuits. Fig.7 (a) and (b) shows power consumptions and delay of existing level shifters circuits. Results show that three proposed circuit's shows better performance in terms of power consumption with a little conciliation in delay.

Table-I Results for proposed circuits

Level shifter configurations	Power Consumption (pW)	Delay (ns)
Modified conventional level shifter	402.2264	2.3376
Modified single supply level shifter	108.641	2.564
Modified contention mitigated level shifter	396.75	0.55206



(a)

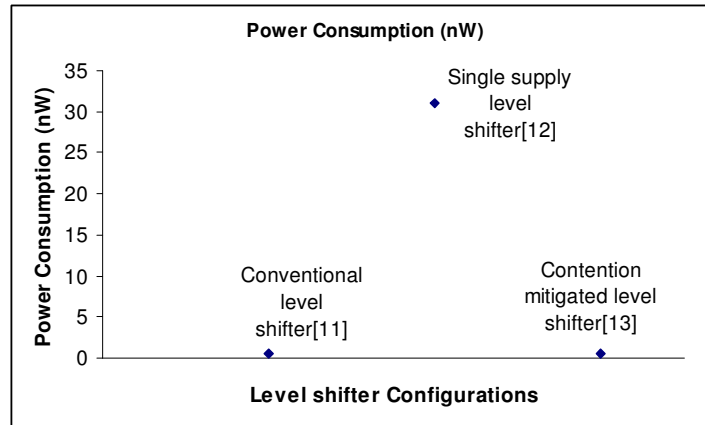


(b)

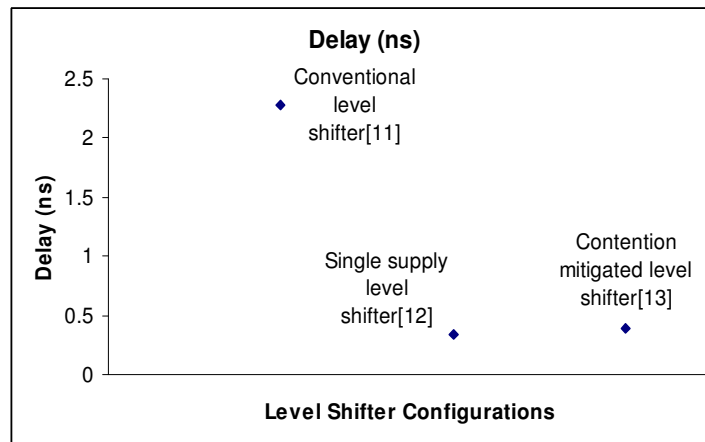
Figure.6 (a) power consumption (b) delay of proposed circuits

Table-II Results for existing level shifters

Level shifter configurations	Power Consumption (nW)	Delay(ns)
Conventional level shifter[11]	0.49833	2.2744
Single supply level shifter[12]	31.06	0.33474
Contention mitigated level shifter[13]	0.4937354	0.391815



(a)



(b)

Figure.7 (a) power consumption (b) delay of existing circuits

4. CONCLUSIONS

In present paper three new circuits of level shifters namely modified conventional, modified single supply and modified contention mitigated have been presented. Modified conventional level shifter gives power consumption of 402.2264pW as compared to 0.49833nW for conventional level shifter. Proposed single supply shows power consumption of 108.641pW as compared to 31.06nW for conventional single supply. Third proposed circuit's shows power consumption of 396.75pW as compared to 0.4937354nW for existing circuit. Maximum output delay results also have been obtained for proposed circuits and it has been observed that with little concession in delay, power consumption has reduced considerably.

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