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Electric Vehicle by using Modified Topology of Multilevel Inverter

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ABSTRACT:

This paper focused with extends the knowledge in studies and analysis of a new family of diode clamp multilevel inverter for electric vehicle application. The modified new diode clamp multilevel inverter concepts is related to reducing the components utilization, which has (n-1) switching devices, (n-3) clamping diodes, (n-1)/2 DC-link sources for achieving the same voltage level of traditional topologies. The proposed system is enhanced the voltage rating and reduce the total harmonics distortion in inverter output voltage. The switching scheme of Alternatively on Opposition Disposition pulse width modulation strategies is implemented to control multilevel inverter. The proposed system reduces the components utilization which has utilizes 45% of components for achieving the same level of voltage. The modified new diode clamp multilevel inverter is coupled with induction motor and its performance is validated with three phase induction motor for variable frequency drive. The inverter topologies performance has been investigated by prototype model.

KEYWORDS:

Multilevel inverter; APO-PWM; Induction motor; Total harmonic distortion; Topology

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1. Introduction

Now a day, electrical energy is one of the important factors for human being to survive in this world. The present and future technologies must meet the challenges in reliability and efficiency of energy. The flexibility of modern power electronics brought to bear to meet the challenges of reliable and efficient energy. The power electronic circuits not only indented the conversion of energy it also controls of electrical energy. These circuits are handling higher power flow than individual device ratings. The main objective of power electronics inverter is to provide a sinusoidal AC output waveform from a DC power supply. This type of conversion and control of waveform is required for electric vehicle, uninterrupted power supply, adjustable speed drives, flexible AC transmission system, active filter and voltage compensators etc,. The sinusoidal AC output waveform magnitude, frequency and phase should be controllable [1] [2]. In recent year, the high power apparatus are widely used in industrial applications. An individual power electronics semiconductor switching device is unable to withstand the medium grid voltage directly.

As a result, a multilevel inverter concept has been introduced since 1975 for high power and medium voltage situations. This has several advantages over a conventional two-level inverter such as reduces the dv/dt stresses and electromagnetic interference problems [3] [4]. The basic concepts of two-level and multi-level inverter topology are shown in Fig. 1. Multilevel inverter achieves the staircase of AC voltage waveform by using series of power semiconductor switches with numerous DC sources. The multilevel inverter topologies have been proposed during four decades. From the continuation of research in multilevel inverter and switching scheme the novel inverter topologies and unique modulation switching strategies has been developed. Moreover, three multilevel inverter topologies structure have been reported in literature, such as cascaded H-bridge multilevel inverter with separate DC sources, diode clamp multilevel inverter and flying capacitor multilevel inverter [5]-[7]. Similarly, plentiful modulation technique have been developed for multilevel inverter topologies such as sinusoidal pulse width modulation, selective harmonics elimination, space vector modulation, and others.

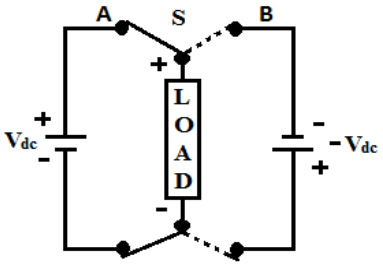


Fig. 1(a): Inverter topologies - Concept of two-level

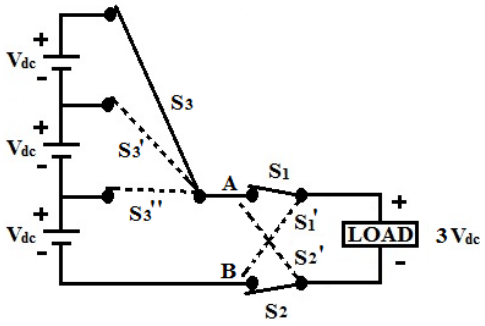


Fig. 1(b): Inverter topologies - Concept of multilevel

Multilevel inverter is one of most popular and very attractive for high-power and medium voltage operation for numerous applications such as industrial medium-voltage motor drives, power systems, train traction, ship propulsion, automotive applications, energy generation, conversion, and transmission [8]-[11]. Unfortunately, the multilevel inverter has few drawbacks; such drawbacks of traditional multilevel inverters are a higher number of switching devices, complex design of the gate drives circuit, require isolated voltage sources. The quality of harmonic levels is enhanced by increasing the number of levels. However, it requires a large number of semiconductor switching devices and gate driver circuits, which reducing the inverter reliability and system efficiency, and increases the system complexity and cost. For low-medium power application the utilization of a large number of switching devices is inadequate, therefore, researchers continue to focus on reducing the component count of the multilevel inverter[12]-[19]. This paper present the operating principle of modified new multilevel inverter topology for reduction of components counts and compare with traditional topologies. The APO-PWM strategy is used to generate a gate pulse for switching devices. The behaviour of new inverter topology with induction motor drives based electric vehicle has evaluated through prototype setup.

2. Modified multilevel inverter topology

2.1. System description

The traditional topology of 5-level diode clamp multilevel inverter typically consists of 2(n-1) switching devices, (n+1) clamping diodes and (n-1) DC-link capacitor, which has shown in Fig. 2. The 5-level inverter topology is taken for example to introduce the modified new diode clamp multilevel inverter which is shown in Fig. 3(a). It has augmented the output voltage level using minimum number of electronics components. The modified new diode clamp multilevel inverter circuit required (N-1) main switching devices, (N-3) clamping diodes and (N-1)/2 DC link capacitors. The circuit can be divided into two parts, which are DC link with DC source and diode clamped part. As seen from Fig. 3, the dc-link capacitor composed with dc source, clamping diode (D_1 and D_2) and centre tapped transformer. Also the clamping diode part is integrated with dc link capacitors (C_1 to C_2) and switching devices (S_1 to S_4). The modified new diode clamp topology has four working states and four kinds of output voltage levels. There are four switches in the proposed structure to achieve 5-level voltage. The dc-link voltage is assumed constant and equal to $V_{dc}/2$, where $V_{dc}/2$ is the voltage across each dc link capacitors. Four working states and their transitions of part are shown in Fig. 4, in which the arrows indicate that direction of conventional current.

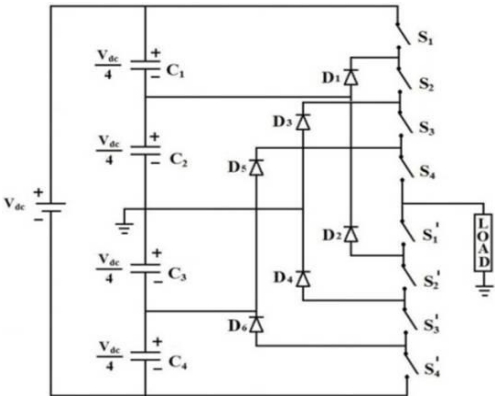


Fig. 2: Traditional method of single leg 5-level DCMLI

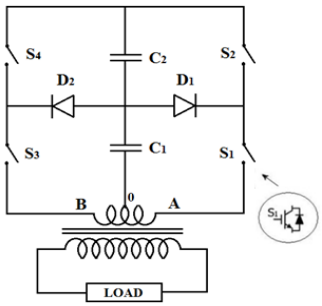


Fig. 3(a): 5-level modified new diode clamp multilevel inverter - single phase

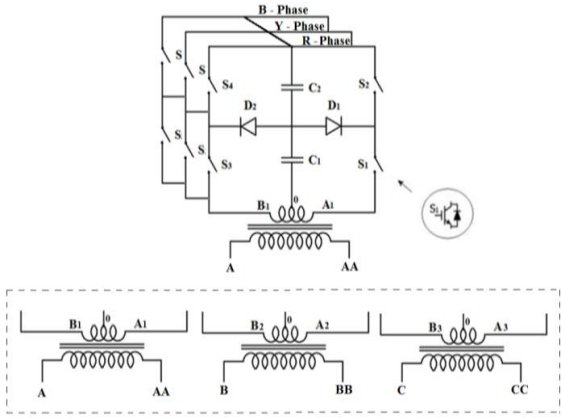
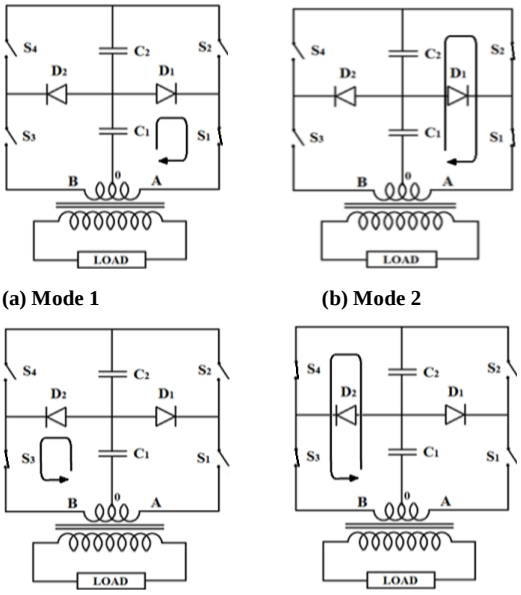


Fig. 3(b): 5-level modified new diode clamp multilevel inverter - three phase

Table 1 describes the operating switching state and its output voltage levels. The four modes of modified proposed system are described in Fig. 4. The centre tapped transformer middle point is permanently connected to negative. The dc-link positive terminal is composed with other two outer terminal of transformer primary winding through S_1, S_2, S_3 and S_4 switching devices and clamping diodes. In mode1: the switching device S_1 is turned ON and D_1 conducted due forward biasing, during the period the dc-link capacitor C_1 voltage $+V_{dc}/2$ connected with load through centre tapped transformer node A to 0. Similarly, in mode 2 the switching devices S_1 and S_2 turned ON and D_1 not

conducted due reverse biasing, during the period dc-link capacitors voltage of $+V_{dc}$ (C_1 and C_2) connected with load through centre tapped transformer node A to 0. While in modes 3 and 4 become redundant for output voltage $-V_{dc}/2$ and $-V_{dc}$ respectively. Every working state provide one kind of output voltage level and zero is another one of the level in inverter, in order to output 5-level voltage is obtained by using minimum number of components.



(a) Mode 1 **(b) Mode 2**

(c) Mode 3 **(d) Mode 4**

Fig. 4: Valid operating modes of MNDCMLI

Table 1: Switching states, clamping diode status and its output voltage

Working state	Switching states (1 = ON, 0 = OFF)				Output voltage	Clamping diode status	
	S_1	S_2	S_3	S_4		D_1	D_2
1	1	0	0	0	$+V_{dc}/2$	FB	NC
2	1	1	0	0	$+V_{dc}$	RB	NC
3	0	0	0	0	0	NC	NC
Mjoi-k4	0	0	1	0	$-V_{dc}/2$	NC	NC
5	0	0	1	1	$-V_{dc}$	NC	RB

Similarly, a single phase modified new diode clamp multilevel inverter is extended to three phase inverter topology which is shown in Fig. 3(b). The structure of three modified new diode clamp multilevel inverter is as single phase inverter topology, the modulation signals of switching pulses are varied per phase with 120 degree phase shift. The operating modes of three phase topology are similar of single phase topology. The secondary of three transformer outputs are connected with star connection and the three phase inverter topology performance is validated with three phase induction motor.

2.2. APO Disposition PWM using open loop sinusoidal reference

The Alternatively in Opposition (APO) disposition PWM is one of the efficient method in sinusoidal pulse width modulation technique. It contains four triangular signals (Ac) and keeping an open loop modulating sinusoidal signal (Ar). All the triangular waveforms are the same amplitude (Ac) and frequency (ωc). However, every triangular waveform is in opposite disposition as shown in Fig. 5. In APO disposition PWM, two triangular waveforms are placed in above the zero reference and other two triangular waveforms are placed below the zero reference. At every instant each triangular waveform is compared with the modulating sinusoidal signal. Each comparison gives 1 or -1 based on the modulation sinusoidal signal and carrier waveform, if the modulation signal is greater than the carrier waveform which has produced the pulse, zero otherwise. From the results of APO disposition PWM the various levels of voltage is appear in inverter topology output terminal.

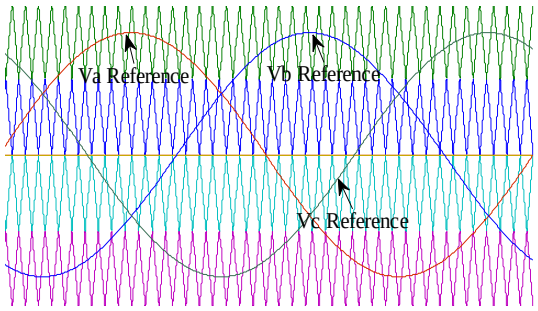


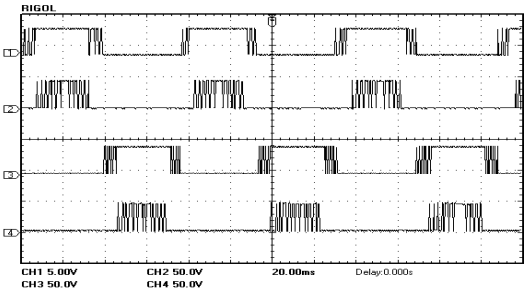
Fig. 5: Alternatively in opposition disposition PWM

3. Experimental results and discussion

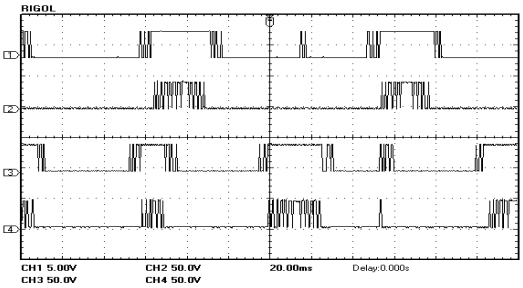
The validation of three-phase topology, a prototype model of three phase 5-level modified new diode clamp multilevel inverter is developed. The modulation signals of Alternatively in Opposition (APO) disposition PWM technique has been implemented using real-time DSP controller. The DSP controller provides the APO PWM signals based on 1 kHz of carrier waveform and 50Hz reference waveform respectively, the required three-phase inverter topology APO PWM pulses hardware results are shown in Fig. 6. The switching pulses are turning ON the MOSFETs (IRF540) of modified inverter topology through opto coupler circuits. The unidirectional conduction and blocking of each switching device and diode are analyzed. During the conduction mode, the voltage across the switching device and diode is 0.7V. Similarly, during the blocking mode the voltage across the switching device and diode are $V_{dc}/2V$. In each half cycle per leg, two switching devices are associated with load. The blocking and conduction voltage of single leg switching device is shown in Fig. 7. The three-phase modified inverter topology, output voltage has increased up to rated voltage level by using step up transformer, which also serves as freewheeling of RL load. The phase voltage , line voltage and THD of modified new diode clamp multilevel inverter hardware results are shown in Fig. 8 and Fig. 9 respectively.

The modified inverter topology provides the phase voltage of inverter is 225Volts, line voltage of inverter is 406Volts, 50Hz frequency and 28.7% of THD respectively. A Prototype model of 5-level modified new diode clamp multilevel inverter has tested on three phase 3 HP induction motor for variable frequency drives, the speed response of induction motor is smooth with

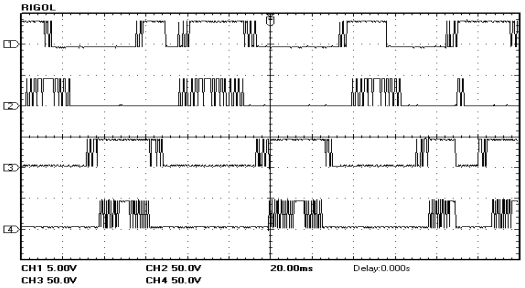
respect to variable frequency. And also proposed three phase inverter topology is investigated with 80% of full load test. The laboratory prototype multilevel inverter model connected with induction motor drives. This has consumed 1660 watts power and takes 3.5A for 80% of full load. This three phase induction motor obtains 1442 rpm speed and provides 92.2% of efficiency. The three phase 3HP induction motor details are given in Table 2. The experimental setup of prototype model of three phase modified new diode clamp multilevel inverter topology with induction motor drives photograph view is shown in Fig. 10.



(a) R - Phase

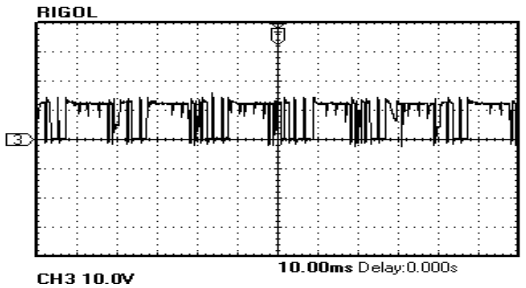


(b) Y - Phase

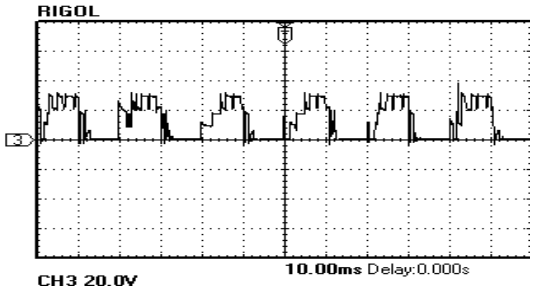


(c) B - Phase

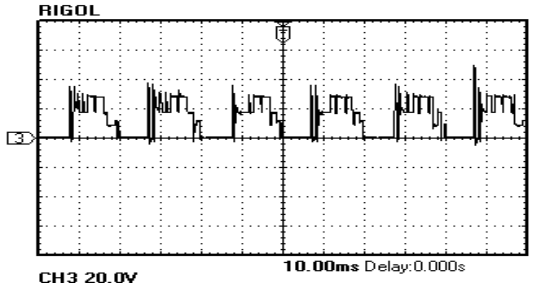
Fig. 6: Gate signals of three phase modified new diode clamp topology



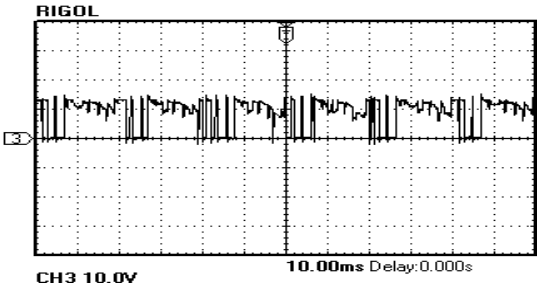
(a) Switch - 1



(b) Switch - 2



(c) Switch - 3



(d) Switch - 4

Fig. 7: Blocking and conduction voltage of switching devices

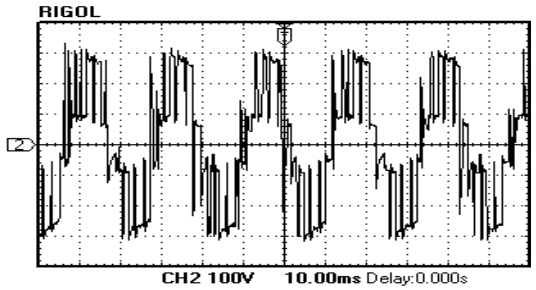


Fig. 8(a): Multilevel inverter R – Phase voltage

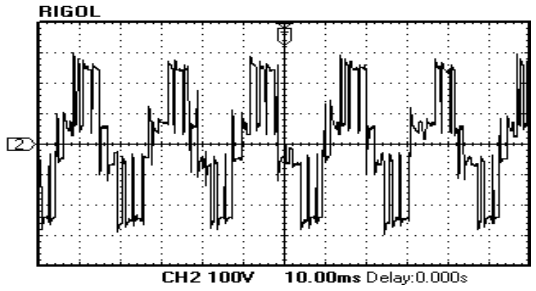
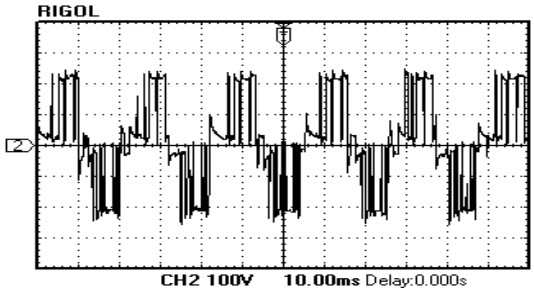
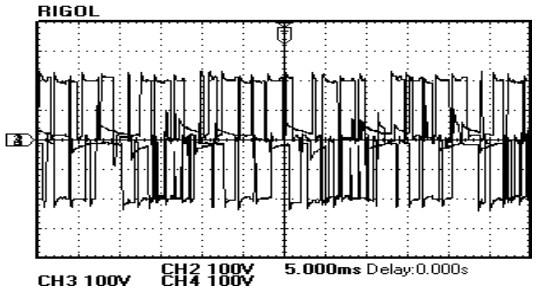


Fig. 8(b): Multilevel inverter Y – Phase voltage



(c). Multilevel inverter B – Phase voltage



(d). Multilevel inverter line voltage

Fig. 8: Three phase modified new diode clamp multilevel inverter output line and phase voltage

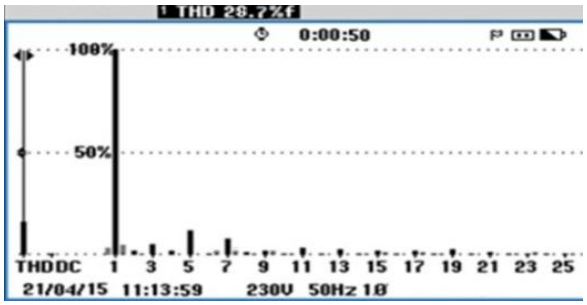


Fig. 9: Harmonics spectrum of real time voltage waveform.

Table 2: Name plate details of three phase induction motor

Phase	3 Phase
Connection	Delta
Insulation	B
kW	2.2
HP	3
Voltage	400V
Amps	4.3A
RPM	1440

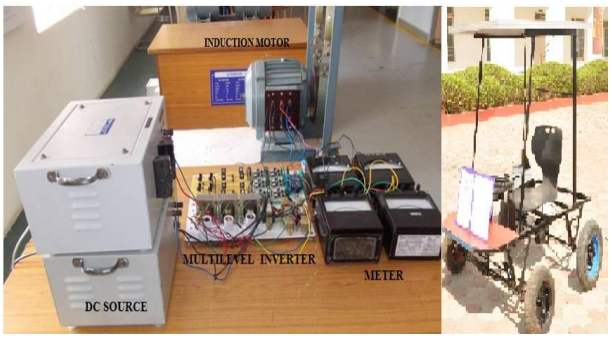


Fig. 10: Experimental set of three phase modified new diode clamp multilevel inverter with prototype model of electric vehicle

4. Components study

The modified new diode clamp multilevel inverter is compared with diode clamp, flying capacitor and cascaded multilevel inverter in terms of component requirements. The traditional topology of diode clamp multilevel inverter typically consists of 2(n-1) switching devices, (n+1) clamping diodes and (n-1) dc-link capacitor. For example, the traditional 5-level diode clamp inverter requires 8 numbers of switching devices and 6 numbers of clamping diodes and 4 numbers of dc-link capacitors. The flying capacitor multilevel inverter possess (n-1)(n-2)/2 flying capacitors, (n-1) DC link capacitors, 2(n-1) semiconductor switching devices, (n-1) upper and (n-1) lower side of semiconductor switching devices. For example, the traditional 7-level flying capacitor inverter topology requires 8 numbers of switching devices and 15 numbers of flying capacitor and 6 numbers of dc-link capacitors. The traditional topology of symmetrical source cascaded multilevel inverter consists of 2(n-1) switching devices, n-(n+1)/2 or (n-1)/2 dc source.

For example, the eleven-level cascaded multilevel inverter requires 20 numbers of switching devices and 5 numbers of dc sources. Similarly the 5-level multilevel inverter contains 8 numbers of switching devices and 2 numbers of dc sources. The proposed topology of a modified new diode clamp multilevel inverter is achieved the same performance with minimum numbers of dc source count and enhance the output voltage. This proposed multilevel inverter required (n-1) switching devices, (n-3) clamping diodes, (n-1)/2 dc-link capacitor and a step-up centre tapped transformer. For example, the 5-level modified new diode clamp inverter requires 4 numbers of switching devices and 2 numbers of clamping diodes and 2 numbers of dc-link capacitors. The performance of modified new diode clamp multilevel inverter is tested by prototype model for induction drive application. The performance of this multilevel inverter topology is not affected due to the static and dynamic behaviour of the induction motor. The comparative analysis of multilevel inverter with respect to number of components requirements is tabulated in the Table 3. Table 4 summaries the components requirements with respect to various voltage levels.

Table 3: Comparison of components requirements with various topologies for odd number of level

Devices	Traditional			Modified New DCMLI
	DCMLI	FCMLI	CMLI	
Switches	2(N-1)	2(N-1)	2(N-1)	(N-1)
Clamping diode	2(N-2)	-	-	(N-3)
dc-link capacitor / DC source	(N-1)	(N-1)	N-(N+1)/2, for 3,5,7,	(N-1)/2

Table 4: Comparison of switching devices

Inverter Topologies	5-level			7-level		
	Switch. devices	Clamp.. diodes	DC - source	Switch. devices	Clamp.. diodes	DC - source
FCMLI	8	-	4	12	-	6
DCMLI	8	6	4	12	10	6
CMLI	8	-	2	12	-	3
Modified DCMLI	4	2	2	6	4	3

5. Conclusion

In this paper, a new modified 5-level diode clamped multilevel inverter has been designed and tested with three phase induction motor drive for electric vehicle. The process of reducing the number of switching devices, clamping diodes and dc-link capacitor has been achieved. The output voltage calculations and its methods have described in this paper. Also, the experimental results have been shown clearly. Thus the result shows that the proposed topology works effectively as a driver for induction motor drives with reduced harmonics and switching devices.

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