Reason - A Technical Journal
ISSN 2277–1654
Vol - XII ● 2013

A DIGITAL DESIGN APPROACH AND IMPLEMENTATION FOR THERMAL ERROR COMPENSATION IN MACHINE TOOLS BY PRECISION POSITIONING AND FEEDBACK SIGNAL MANIPULATION

K.T. Navya[1], V. Shanmugaraj[2], G.C. Mohan Kumar[3] and P.V. Shashikumar[4]

[1]Post Graduate student, National Institute of Technology, Karnataka, Surathkal
Email: navya.kt1@gmail.com
[2] Scientist-E, Central Manufacturing Technology Institute, Bengaluru
Email: shanmugarajv@cmti-india.net
[3]Professor and Head, Mechanical Dept., National Institute of Technology, Karnataka, Surathkal,
Email: mkumargc@gmail.com
[4]Joint Director, Central Manufacturing Technology Institute, Bengaluru
Email: pvs@cmti-india.net

Manuscript received on: December 11, 2013, acceped after revision on: February 26, 2014.

Abstract: The proposed paper aims at designing a real time precision positioning control circuitry for a numerical control device used to control a machine tool with encoder type feedback. More particularly it is intended to design a digital compensating circuit for modifying a position control signal to effect a correction for repeatable linear errors such as the dimensional changes in the machine structure due to changes induced into the structure by operating temperature ranges. The error correction is performed by modifying encoder type position feedback signals supplied to the machine tool controller. This provides real time compensation for thermal errors in positioning of computer numerically controlled machine tools, coordinate measuring machines (CMMs), robots, assembly systems, and the like.

The error correction being accomplished by the Error Correction Circuit(ECC), which adds or subtracts a predetermined number of pulses to the pulses coming from a feedback device such as encoder to compensate for over shoot or under shoot of the machine tool respectively.

Keywords: Elongation of Ball Screw, Encoder Feedback Pulses, Pulse Addition and Subtraction, Thermally Induced Errors

1. INTRODUCTION

Precision machining means Machining and Measuring to exact specifications. This includes four basic areas to consider: dimensions, limits, tolerances, and allowances. With ever increasing demand for part quality and tight tolerances in machining, it is required that the machine tools be accurate and repeatable within the desired tolerance limits over the entire machining volume, and in a wide variety of operating conditions. However, in practice, the specified accuracies and repeatability are not achieved under operating conditions, due to a wide variety of errors induced in the machine tool by virtue of its geometry and assembly, thermal expansion of the machine components and the process itself. These errors in general, are not within acceptable limits and need to be eliminated or reduced to achieve the desired part dimensional accuracy [1].

2. IMPLEMENTATION

Considerable numbers of temperature sensors are placed all around the machine elements to measure the temperature variations and to generate the compensation value based on temperature compensation algorithm running in an embedded controller. This is not a part of the proposed paper. Once compensation is required, the error corrector circuit (ECC) of the proposed paper performs the necessary compensation.

The circuit is designed to compensate for positioning errors that can occur in the two axes of motion of the machine tool, say X-axis and Z-axis based on a control signal X/Z coming from an embedded controller. X/Z=1 for compensation along X-axis and 0 for Z-axis.

The compensation request comes from the embedded controller based on the control signals S1 and S0 as shown below.

Table 1 Compensation table

S1	S0	
0	0	Only encoder pulses
0	1	Only encoder pulses
1	0	Subtraction compensation
1	1	Addition compensation

where,

S1 is 1 if compensation is required else 0, and

S0 is 1 for addition and 0 for subtraction.

Once the compensation is performed, an acknowledgement is sent to the embedded controller to indicate the end of compensation process and hence it can request for the next compensation as per the requirement.

A basic block diagram is as shown in Fig.1. For subtraction of pulses, the encoder pulses are blocked in number specified by the compensation value by using a counter, comparator and AND gate.

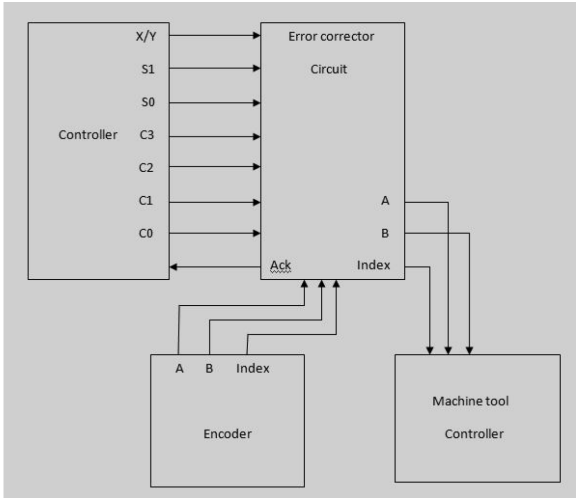

Fig.1 Block diagram of the setup

Addition of pulses is implemented by splitting each pulse into two for the required number of pulses using frequency doublers using Phase Locked Loop and XOR gate, pulse pre-conditioning circuit, 90° phase shifter, direction detector, direction corrector, full adder, counter, comparator and basic gates.

2.1. Pulse Subtraction

This is done by using a simple 4 bit magnitude comparator, counter and an AND gate. In the absence of subtraction compensation request, the counters in the subtraction block are in master reset state giving no output.

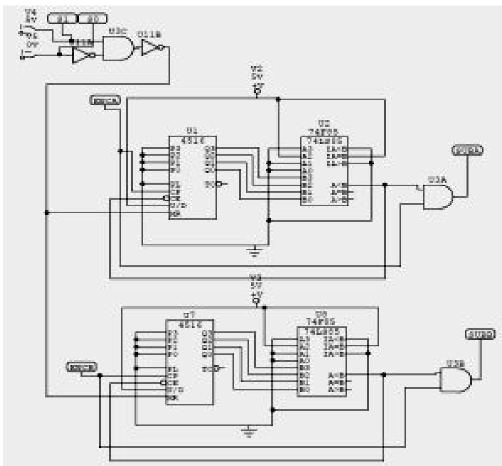

Fig.2 Pulse subtraction circuit

The comparator compares the compensation value(A) with the counter value of encoder pulses(B) from the counter output and gives out A<B=0 as long as the number of pulses equal to the compensation value are passed. This value is ANDed with the encoder pulses to block that many number of encoder pulses and to pass the remaining encoder pulses, thus yielding pulse subtraction. Also the A<B=0 condition is used to control the count enable pin of the counter which disables the counter once the required number of pulses are blocked, thus prevents the circuit from blocking extra pulses

2.2. Pulse Addition

Addition of pulses is accomplished by splitting the specified number of encoder pulses as demanded by the compensation value into two each, thus performing the addition operation. However, the modified encoder pulses coming out of the circuit need to have the necessary 90° phase shift between them so as to be qualified as encoder pulses and recognised by the machine controller as feedback signals.

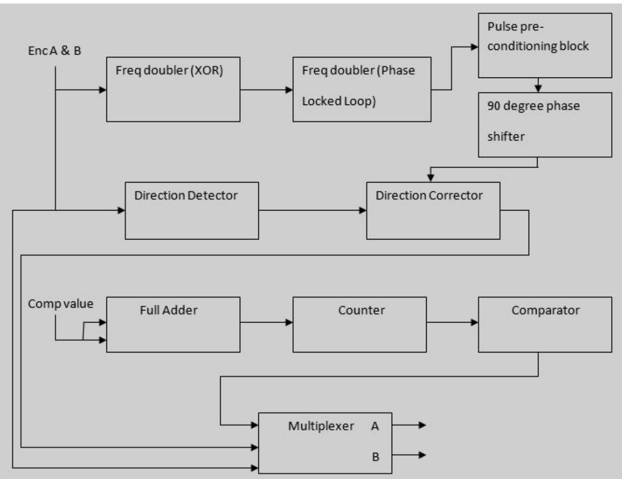

Fig.3 Block diagram for pulse addition

Since the frequency of the encoder pulses is variable from zero when the machine is at rest to a maximum value when the machine axis is moving at high speed, maintaining the required phase shift between the modified pulses is quite a challenging condition is to be taken care of as any error in the phase shift can become fatal by making the situation from bad to worse. Also care is taken to avoid the added pulses from overlapping on the encoder pulses.

2.2.1. Frequency doubler (XOR) block

Splitting of encoder pulses is done by doubling their frequency and XOR gate is the most basic component which can be used to obtain a doubled frequency signal, provided, the inputs to the XOR gate have 90° degree phase shift between each other with 50% duty cycle. Since encoder pulses A and B always satisfy this condition, XOR gate is used to obtain a doubled frequency signal.

Since the output (XOR) after XORing encoder A and B pulses is a single pulse train, another pulse train which has a 90° phase shift with respect to the output of the XOR gate is needed which can be sent as the modified encoder B pulse as long as the compensation is needed to accomplish addition. Since the frequency of encoder pulses keep varying continuously depending on the velocity with which the axis is moving, a phase shifter circuit which takes a single pulse train as input and gives out two pulse trains at its output with 90° phase shift between them and with a frequency which is half the frequency of the input pulse train is used.

But since it is needed that the modified B pulse has to have the same frequency as A pulse, one way of achieving that could be by using a signal which is double the frequency of the XOR signal as clock to the 90° phase shifter circuit so that it gives out two pulse trains whose frequency is same as that of XOR signal after its frequency division by the circuit and with a 90° phase shift between them.

2.2.2. Frequency Doubler (Phase Locked Loop)

To obtain a signal with double the frequency of XOR signal and with 50% duty cycle for a variable frequency range of encoder pulses, the best suited and simplest method is by using a phase locked loop (PLL) as frequency doubler. The circuit is as shown in Fig.4 below.

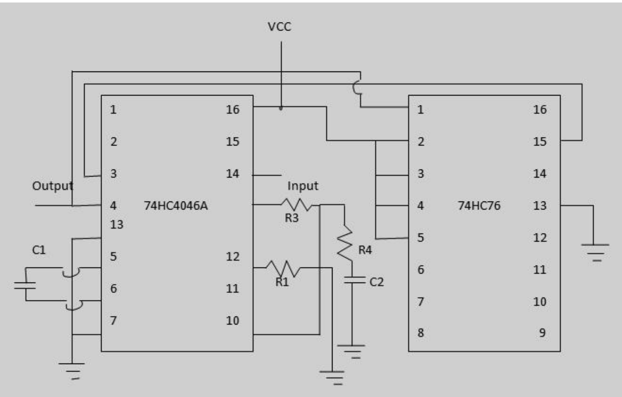

Fig.4 Frequency Doubler (PLL) ckt

PLL design:

The PLL is designed to double the frequency of XOR pulse in the range of 0 to 160 kHz. The encoder taken into consideration is of 2500 pulses per revolution specification for a ball screw pitch of 5mm with the fastest velocity to be 10 meters per minute. Hence the maximum frequency of encoder pulses is about 80000 pulses/sec (80 kHz). Since the XOR signal frequency is twice the frequency of the encoder pulses i.e., 160 kHz, and it is given as input to the PLL circuit, the fmax=160 kHz and fmin= 0.

Center frequency f0 = 80 kHz

Assuming C1 = 1000 pF

R1 = 57.87 kΩ 56 kΩ

C2 = 1 μF

R3 = 357 Ω 360 Ω

R4 = 97 Ω≈ 100 Ω

From the experimental setup, of the above design, it is observed that the PLL starts doubling the frequency of pulses from 700 Hz and it attains perfection from 2.3 KHz to 125 KHz and continues to double till 160 KHz.

2.2.3. 90° Phase Shifter Block

The output 2XOR from the frequency doubler (PLL) circuit is used as clock to the 90° phase shifter circuit to obtain two signals which are same in frequency as the XOR signal and with a 90° phase shift between them as shown in Fig.5 below.

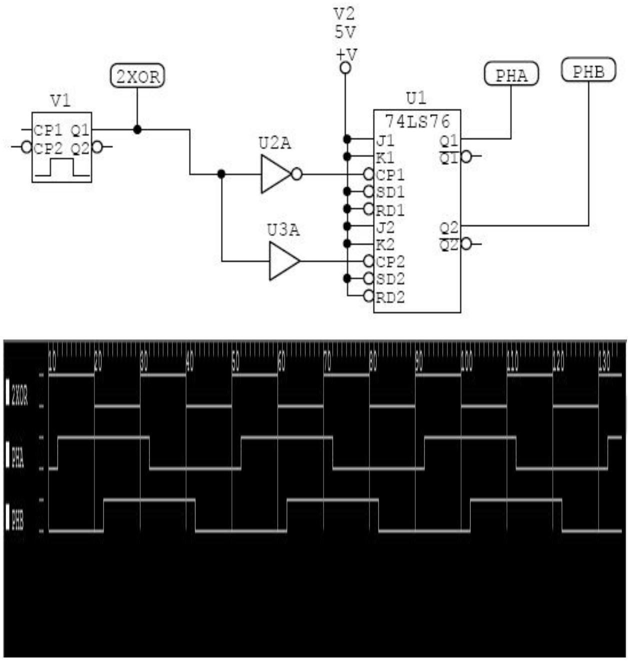

Fig.5 90°phase shifter ckt and simulation

2.2.4. Pulse Pre-Conditioning Block

Encoder pulses are produced based on transparent or the opaque area of the glass scale at the start of the pulse generation. This can cause a problem to the phase shifter circuit as there is no way that the format of the pulse is determined. Hence, a pulse pre-conditioning circuit is used as shown in the Fig.6 below.

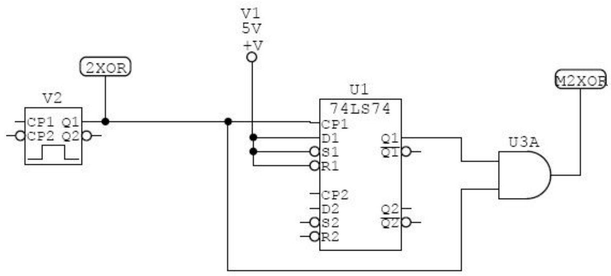

Fig.6 Pulse pre-conditioning ckt

This circuit ignores any falling edge in the beginning of pulse train and pass only the rising edge of the pulse first irrespective of the pulse format.

2.2.5. Direction Detector Block

The modified pulses need to have the same direction (A leading B or B leading A) as original encoder pulses in order to successfully complete the compensation process. The circuit is as shown in the Fig.7 below.

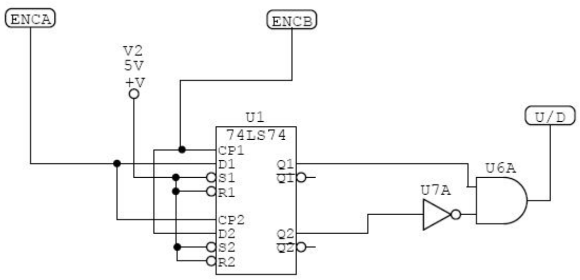

Fig.7 Direction detector ckt

It gives an output of 1 if it is A leading B (positive axis motion) and a 0 for B leading A (negative axis motion).

2.2.6. Direction Corrector Block

Once the direction of the original encoder pulses is detected, the pulses which are split and to be added into the original encoder pulse train are modified so as to have a A leading B or B leading A according to the direction of encoder pulses using a U/D signal as control signal to a 2 input MUX.

2.2.7. Full Adder, Counter and Comparator Block

After splitting each pulse into two for addition compensation, the total number of pulses passed when the compensation is in progress is twice the compensation value specified. As the maximum compensation value is limited to 15 to prevent unreasonable compensation to the machine thus avoiding a possible machine crash, a 4 bit binary full adder is sufficient to obtain twice the compensation value as it can add the maximum value (1111 in binary) twice that can come from the embedded controller.

This value of sum and Cout from the full adder is compared with the counter value which counts PHA and PHB pulses from phase shifter circuit and when the A>B output of comparator is high, the direction corrected pulses UDA and UDB are passed whose frequency is twice the frequency of encoder pulses and when it is low, the original encoder pulses are passed using a 2 input multiplexer.

2.3 Acknowledgement Block

Once the requested compensation is provided (addition or subtraction), an acknowledgement is sent to the embedded controller to indicate that the compensation process is over and it can request for the next compensation. The acknowledgement is a short duration pulse which is generated at the end of compensation. The circuit takes care of the acknowledgement coming from either X-axis board or Y-axis board.

2.4. Mux Block

A 4 input MUX is used to send the corresponding acknowledgement signal ACK to the embedded controller based on the control lines S1 and S0 for either addition or subtraction. Another dual 4 input MUX is used to pass the final modified signals at the output depending on the control signals S1 and S0 and is enabled if X/Y signal = 1 for X-axis and 0 for Y-axis.

3. RESULTS AND DISCUSSION

The results for subtraction compensation and addition compensation for a compensation value of 3 pulses are as shown in Fig.8 and Fig.9 below respectively.

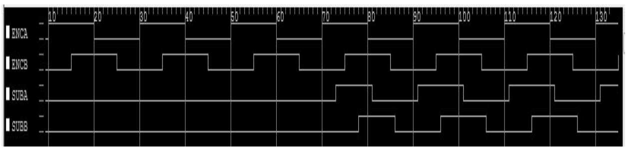

Fig.8 Result for Subtraction compensation

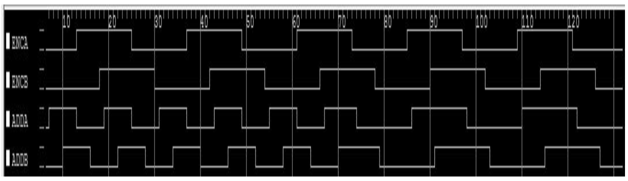

Fig.9 Result for Addition compensation

From the hardware implementation of the design, it is observed thatthe number of pulses added or subtracted stick to the specified value with good accuracy.

It can also be observed that the modified pulses have the required 90° phase shift between them irrespective of the frequency with which they are added or subtracted.

4. CONCLUSION

The circuit is designed to modify the feedback pulses from incremental rotary encoder to compensate for thermally induced positioning errors.

The hardware implementation of the design works successfully as required by subtracting or adding the required number of pulses maintaining the 90° phase shift between the A and B pulses at any given frequency and time.

The same hardware can be duplicated for any number of machine axes with minimal changes. This helps in correcting the positioning errors in a machine tool with good accuracy and precision.

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