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TRIPLE MATERIAL SURROUNDING GATE MOSFET FOR SUPPRESSION OF SCES

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Abstract: Continuous downscaling of conventional MOSFETs suffers from various detrimental short-channel effects (SCEs). A combination of novel device structures and material property improvement can overcome the SCEs in order to sustain the historical cadence of scaling. In this paper, a comprehensive analysis on the effect of downscaling in the performance of a novel gate-engineered Triple Material (TM) Surrounding Gate (SRG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is presented. With the help of device simulator Silvaco ATLAS, the effect of variation of the radius (R) and the channel length (L_g) on the surface potential, the Electric Field and the drain current is reported in order to provide an enticement for future theoretical studies and experimental researches of the critical aspects of the gate-engineered surrounding gate MOSFET. Results indicate that a trade-off between gate length L_g and channel radius R is necessary to achieve higher immunity against SCEs with a lower OFF-state leakage current to find its usage in ultra low-power applications.

Keywords: Nano-scale MOSFET; SCEs; TCAD; SRG MOSFET; Triple Material Gate; Gate Engineering.

1. INTRODUCTION

As a result of aggressive downscaling, short-channel effects (SCEs) become a major concern for future downscaling especially in the sub-100nm region [1]. In order to sustain the historical cadence of scaling by extending the ITRS roadmap beyond 100nm, SRG MOSFET evinces himself as a major promising candidate due to its higher scaling capability [2].

In 1999, Long et al. proposed a new type of Hetero-Material gate (HMG) FET structure [3] using "gate-engineering" technique to circumvent short-channel-effects (SCEs) [4]. The Dual-material gate (DMG) structure, a variant of HMG uses two gate materials have been fabricated [5] and theoretically studied [6]. In this structure, two metal gates with different workfunctions denoted by M_1 and M_2 are amalgamated together to form the gate terminal. For an n-channel MOSFET, the metal gate M_1 with higher workfunction (Φ_{M1}) is placed near the source-end, and the metal gate M_2 with lower workfunction (Φ_{M2}) is placed near the drain-end such that $\Phi_{M1} > \Phi_{M2}$. For a p-channel MOSFET, the placement of M_1 and M_2 is opposite as compared to an n-channel MOSFET [6]. For an n-channel MOSFET, the material having higher workfunction M_1 functions as a "control gate", to control the threshold behaviour of the MOSFET [6]. In contrast, M_2 works as "screen gate" to screen the channel region located underneath M_1 from the drain potential variation [7]. Such a configuration introduces a step-function at the interface of the two metals in the variation of the potential profile along the channel which shields the channel located underneath the "control gate" from drain potential variation, thus resulting in a reduction of SCEs [8]. This step-potential profile creates a step-function in the profile of the Electric

Field along of the channel. The peak of the Electric Field, located at the junction of the two metals, causes an increase to the carrier velocity, thus increases the carrier transport efficiency. Moreover, in a DMG structure due to the reduction of the peak of the Electric field located at the drain side, HCEs reduces [9], resulting in an increased device reliability [10].

It has been demonstrated that "gate-engineering" technique employing a Dual-Material-Gate (DMG) can improve the carrier transport efficiency by modifying the surface potential and Electric Field distribution along the surface of the channel [11]. The DMG technique has already been incorporated into bulk MOSFETs [12], silicon-on-insulator (SOI) devices [7], silicon-on-nothing (SON) MOSFETs [13], double-gate (DG) MOSFETs [14] and surrounding gate MOSFETS [15] to achieve improved performance and to diminish SCEs. Recently, DMG techniques have been encompassed to Tunnel FETs [16] in order to improve their electrical characteristics. DMG structure has been also added into junctionless nanowire transistors in order to obtain a number of desirable features [17]. In spite of the several benefits offered by the DMG MOSFETs, the major issue of concern that remains is the feasibility of fabrication. In our previous paper [18], this question is addressed to accentuate the challenges and the remedies to emphasize the current status of fabrication of DMG MOSFETs. In terms of the availability of many reported successful fabrication techniques [19], [20] it is evident that viability of fabrication of gate-engineered MOSFET should not stop the opportunity to catch the possible benefits offered by gate-engineering.

Going one-step ahead of DMG structure, Tiwari et al. proposed [21] Triple-Material-Gate (TMG) structures, in order to obtain further improvement in performance over DMG structures. Recently, in order to combine the advantages from gate engineering and surrounding gate structure, a novel gate-engineered surrounding gate MOSFET device structure was proposed [22]. Theoretical modeling study of gate-engineered surrounding gate MOSFET structure to reduce SCEs has been reported [23]. However, the effect of downscaling on the performance parameters followed by an optimization of device parameters has not been available. Therefore, in this work, our basic aim is to study the impact of the downscaling of device parameters such as radius, channel length and gate oxide thickness on the device performance in order to reduce SCEs.

In this study, the effect of variation of device parameters such as radius, channel length and gate oxide thickness on device performance are studied and then optimized parameters are found out. An analytical model [24] of TMSRG MOSFET previously reported using MATLAB conform the validity of the simulation methodology used in this work. Device simulator ATLAS was employed to investigate the effect of device parameter variation [25].

2. DEVICE STRUCTURE AND SIMULATION SETUP

The three-dimensional device structure of TMSRG MOSFET considered in this study is shown in Fig. 1. The device parameters are chosen according to the 35nm gate length technology specified in the International Technology Roadmap for semiconductors (ITRS) 2013 version for low operating power applications [26] and are shown in Table 1 below. The supply voltage is considered to be equal to 0.8V.

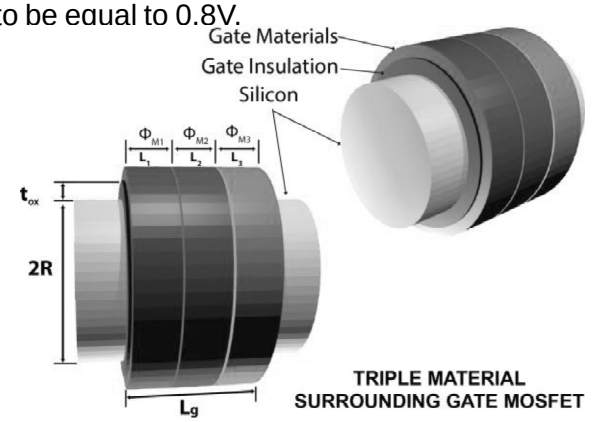

Fig. 1: 3-D device structure of TMSRG MOSFET

Table 1: List of values of the TMSRG MOSFET Device parameters used for simulation

Parameter	Value
Radius (R)	10-30 nm
Channel Length (L_g)	15-40 nm
Gate Oxide (t_{ox}) Thickness	1 nm
Length of The Source/Drain	15 nm
Uniform Source/Drain Doping Concentration	10^{20} cm ^{3}
Uniform Channel Doping Concentration	$2x10^{16}$ cm ^{3}

The simulated device uses an abrupt doping profile between the channel and the source/drain ends. The work function of the gate materials are in decreasing order from the source to the drain: Φ_{M1}= 4.8eV (e.g., Au), gate material Φ_{M2}=4.6 eV (e.g., Mo), and gate material Φ_{M3}=4.4 eV (e.g., Ti) with corresponding lengths L_1, L_2 and L_3 respectively. In this work, the ratio of the lengths of the three different gate-materials of TMSRG MOSFET structures considered is L_1:L_2:L_3= 1:1:1.

Device simulation is performed using carrier transport modeled by conventional drift-diffusion (DD) model combined with Fermi-dirac carrier statics model. To model recombination phenomenon, Schokley-Read-Hall (SRH) and Auger recombination model is adopted. As we are dealing with devices having radius greater than 5 nm and channel length greater than 10 nm, therefore quantum mechanical effects (QMEs) are negligible [27] and has not been considered in this work. CVT Lombardi mobility is adopted to model the field and concentration dependent mobility reduction. Newton and Gummel methods are employed to obtain the numerical solution of the coupled differential equations.

3. RESULTS AND DISCUSSION

Fig. 2 and Fig. 3 shows the simulated profile of the potential and lateral Electric Field taken at 0.1 nm below from the oxide surface as a function of the position along the channel from the source end to the drain end for different values of channel radius R of a TMSRG device. As a consequence of gate-material engineered structure, the surface potential profile and corresponding lateral electric field profile along the channel increases sharply at the interface of the two different gate materials. As a result of this sharp increase of the potential and lateral Electric Field, carrier velocity increase, and this in turn causes an increase in the carrier transport efficiency. From Fig. 2, it is observed that as radius R decreases, the minimum value of surface potential increases, and the position of the minimum surface potential shifts towards the source side, thus indicating more amount of band-bending, which results in a reduction of drain-induced barrier lowering (DIBL) and reduction of threshold voltage roll-off. Thus, it may be concluded that reduction in channel radius results in reduction of SCEs.

On the other hand, it is evident from Fig. 3 that as radius R decreases the peak of the lateral Electric Field decreases at the drain side. A high Electric Field near the drain side may results in the formation of highly energetic and accelerated “hot-carrier”, which under the influence of transverse Electric Field may tunnel into the oxide. As a result, the hot carriers may get trapped into the oxide region to damage the interface, thus causing concerns about device performance and device reliability. Thus, it may concluded that a decrease in Si film thickness results in the decrease in the drain side lateral Electric Field, thus ensuring the device reliability from hot-carrier effects (HCEs).

Fig. 4 and Fig. 5 shows the drain current I_D as a function of the gate-to-source voltage V_{GS} for different Si film thickness and different gate lengths respectively. The drain current I_D increases with the Silicon thickness being consistent with the fact that thicker Si film exhibits lower gate-controllability. This may be attributed due to the fact that for a thicker Si film, the gate

exerts reduced control over the channel center potential and hence an increase in the subthershold leakage current, which in turn causes a decrease in the subthershold swing. It is evident from Fig. 7 that the drain current I_D of a TMSRG or SMSRG MOSFET having large Si film thickness (R=50nm) varies without the regard of the gate-to-source bias V_{GS}, resulting in large subthershold leakage and hence in higher power dissipation. Moreover, Fig. 4 reveals that TMSRG MOSFETs provides higher drain current as compared to SMSRG MOSFETs of same dimension under same condition due to their higher carrier-transport efficiency attributed by its gate-engineered structure.

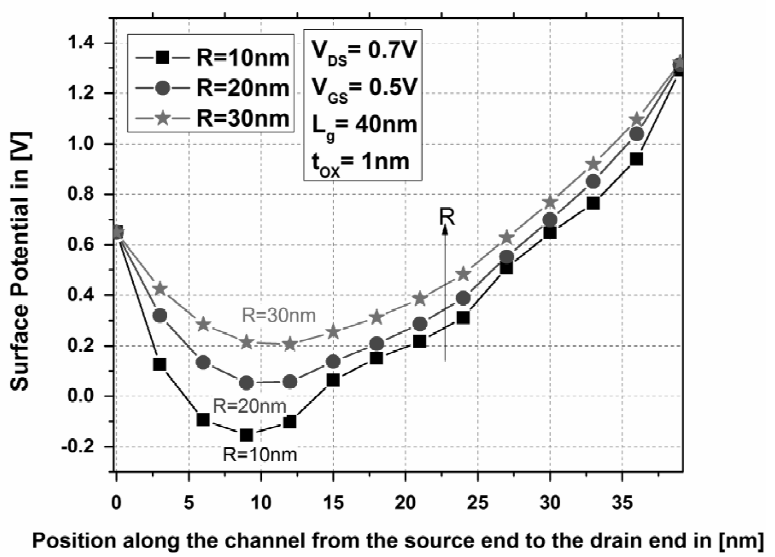

Fig. 2: Variation of Surface Potential as a function of position along the surface of the channel from the source end to the drain end for variable values of radius R ranging from 10nm to 30nm with gate length L_g=40nm, oxide thickness t_{ox}=1nm, V_{GS}=0.5V and V_{DS}=0.7V

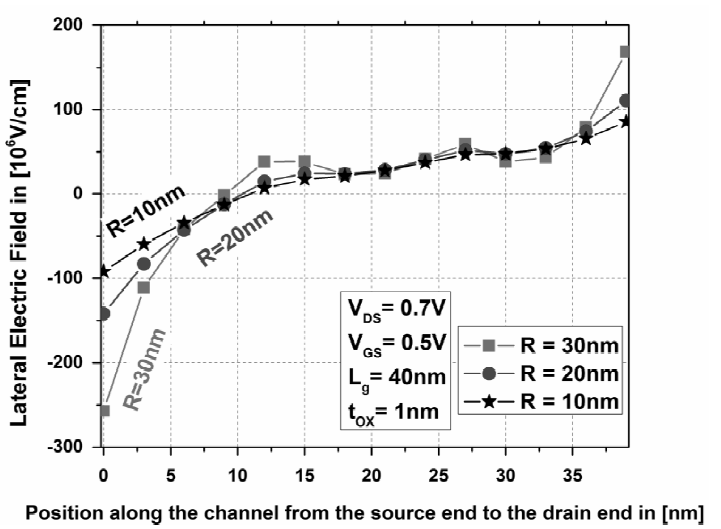

Fig. 3: Variation of lateral Electric Field as a function of position along the surface of the channel from the source end to the drain end for a TMSRG device with gate length L_g=40nm, oxide thickness t_{ox}=1nm, V_{GS}=0.5V, V_{DS}=0.7V for variable values of radius R ranging from 10nm to 30nm

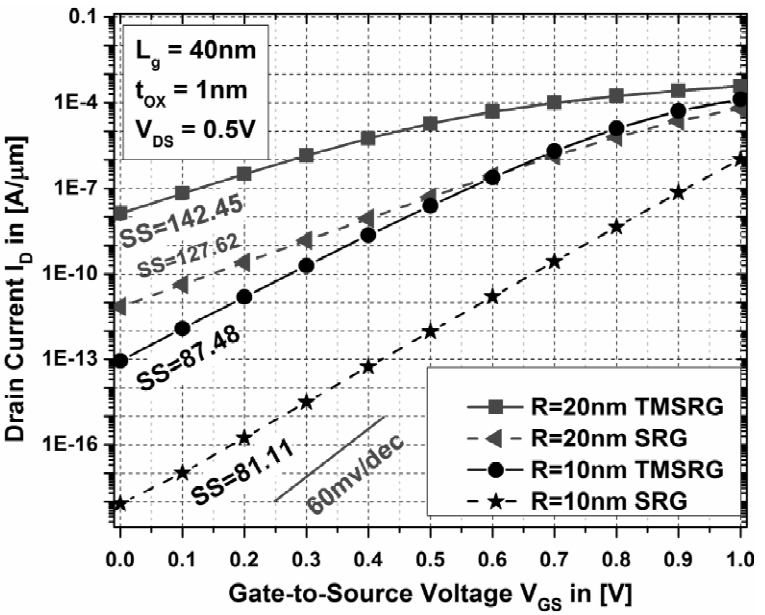

Fig. 4: The dependence of the drain current I_D on gate-to-source bias V_{GS} with subthreshold slope (SS) in mv/dec marked for different values of radius R ranging from 15nm to 50nm with V_{DS}=0.5V, L_g=40nm and t_{ox}=1nm

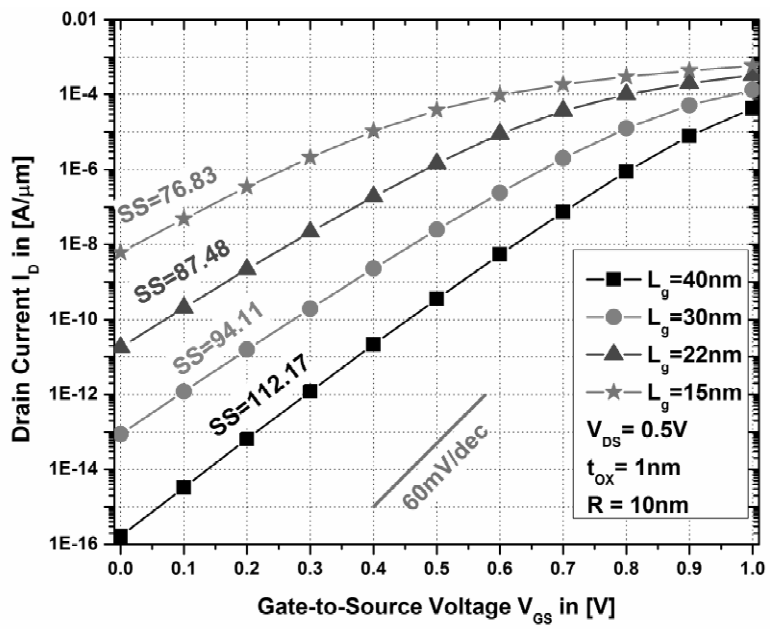

Fig. 5: The dependence of the drain current I_D on gate-to-source bias V_{GS} with their corresponding subthreshold slope (SS) in mv/dec marked for different values of gate length L_g ranging from 15nm to 40nm with V_{DS}=0.5V, R=10nm and t_{ox}=1nm

From Fig. 5, it is clear that for a given gate bias, the subthreshold drain current is lower for a longer channel length. This follows from the fact that the minimum channel potential at the surface, rises significantly with shorter channel lengths due to increasing SCEs. Thus, reduction of gate-length L_g causes reduction in subthershold swing exhibiting a slower transition between OFF (low current) and ON (high current) states.

4. CONCLUSION

This paper reports an extensive simulation-based analysis to find the impact of device parameters like the silicon thickness and gate length on the surface potential, Electric Field and drain current.

Result reveals that downscaled TMSRG MOSFET provides higher efficacy to prevent short-channel effects (SCEs) as compared to a conventional SMSRG MOSFET due to its enhanced carrier transport efficiency and better shielding of channel region located near the source from the drain potential variation.

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