A Type of Mechanical Electro Mechanism for Radiofrequency Telecommunication Purposes

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1. Introduction

Nowadays, modern distributed systems usually rely on multi-core processing Unit. The So called X-Scale Microprocessor's Design Approach makes the world come from a batch-command and Graphics Lack computer age into a true multi-tasking systems'age.

Currently, since many world renowned PCs are implemented using the so called Sun Micro-system Technology, typically using Virtual Box Core Implementation and coupled with cloud distributed control mechanisms imported by Fedora (in Fedora 2 core's brown filter design pattern).

The design patterns in this literature mainly focus on 3-dimensional Bayesian Algorithms and its implementation on IBM MIPS micro-controller by using the so called Labview design pattern in SAGE software. The design approach's aim is to do pattern classification on the designed system and implement antennas to do wireless telecommunications.

2. Microelectro-Mechnical-System Design Approach For Clouding Navigation System

In modern navigation systems, for instance, the GPS (Global Positioning System) and the improved version: Nucleus-Pole, Powered by Purdue University West Lafayette, which possess only minor parts by satellites, however, can also perform Unified AGF(Aviation and Ground Forwarding) for civilian purposes. the revised version of it: the North-Pole Navigation System Mechanism is proposed by Feng An in this literature.

The Design Patterns for this applications are as follows:

1) The Aviation Object Recognition by Implementation of 3D Bayesian Algorithms and

Relevant EM/MPM Algorithms on the sky's videos.

2) The Ground Object Recognition by Implementation of SUGAR Based Antennas Design Approach and their relevant Labview Powered Verilog & VHDL Models' Design Patterns.

3) The Global Unified Navigation Mechanism is primarily based on Cloud Computing Mechanisms and its relevant alternative Ubiquitous and Mobile Computing theories. For the Design Simplicity considerations, the design patterns of the system is primarily rely on three design Patterns: (1) Anti Electro Megnetic forces navigation; (2) Anti Electro Megnetic EMC (Electro Megnetic Interference) Navigation; (3) Anti Gravitational Pull Navigation. The Design Patterns Approach is mainly focus on applications by using Labview and its direct ESL Implementation via Verilog & VHDL Hardware Realization. The C# source coding is also used and C++ protocol unwrapping are implemented.

3. Design Patterns for Dynamically Pattern Recognition

The dynamically pattern recognition algorithms are based on modern control theory, the so called lumped system design approach guarantees that the dynamically distributed and mobile switchable Unified Navigation system is OK as it is a Bounded Input and Bourned Output (BIBO) system, and the system should be linear by retain the system's input and output structure as MIMO and also separately one-input-one-output's type correlated.

The Proposed system's IP Cores are designed in VHDL as follows:

Module 1: for calculation of the x-axis calibrition

```
Namespace LTD.'*stdio.ccr
Using namespaces on Quartus2 and Modeltech modelsimVRK Design patterns none.'*rrskelgasprz.';
Using x;'*
Using kkrlvc.//In order to get x-axis calibrition modules from Quartus Embedded Parts
End
```

Module 2: for calculation of the y-axis calibrition

Namespaces ccrsd.*.rrk
Design patterns none.*rrsgceqpa';rre
Using yccd' //In order to get y-axis calibrition modules from Quartus Embedded Parts
End

Module 3: for calculation of the z-axis calibrition
Namespaces rrpks'r'cg
Design patternbs none'ccf
Using zpps'rkec //In order to get z-axis calibrition modules from Quartus Embedded Parts
Module 4: for Unified Navigation and BIBO regulation Guarantee
Namespaces ccdrgtyuis; Using BIBO criterias; LLCVS:eesqa.

Module 5: for Implementation independent Algorithms (Unwrapping) Namespaces ewrtyusdfeghcvbdfnmj;
Cqreasdfgu ccp rre ccs picc maplab matlab.'; End

Module 6: for Aviation Object Recognition
Namespaces ccefk //to use the standard Quartus Algorithms for Aviation Object Pattern
Recognition
End

Module 7: for Implementation of 3D Bayesian Algorithms and Relevant EM/MPM Algorithms on the sky's videos
Namespaces ccdfret; //to use the 3D Bayesian Algorithms and EM/MPM algorithms held by
Quartus
End

Module 8: for Ground Object Recognition
Namespaces ccdfghytu.';rrf; // to use the standard GPS algorithms help in Quartus software's compiler
End

Module 9: Implementation of SUGAR Based Antennas Design Approach and their relevant Labview Powered Verilog & VHDL Models' Design Patterns
Namespaces ssdfert'.; // to use the standard Antenna Pattern's type 2 for Satellite Genre
Digital and Analog Separately communications
Using Labview9.0 maple ccs ddk dev rrp picc mplab For For For Rrp.';./ End End End

Module 10: Implementation of X-Scale MIPS processor's Structure
Usingnamespace MIPS standioports.'rref
End

Module 11: Implementation of Middle ware between the MIPS processing Cores and the antenna parts' modules in order to guarantee the MIMO characteristics of the digital communication system
Using maplespaces Mips And And And For For Or Nor Kks Kylix Using C++.'Rrk End

Module 12: Virtual Box Virtual Co-Processing Cores
Using maplespaces virtualvip.'*rre
End

Module 13: Fedora 13 Core's Hardware Implementation on MIPS processing core using the DSP Assembly Compilation Arithmetics
Using maplespaces virtualccr.'ccf
End

Module 14: On Fpga realization of multiple MIPS Cores By using off-chip oscillator clocks
(8-sample) from ON FPGA PIC Micro-controller Realization
UsingfpgaANDcpldANDrrp.'CCF; END

Module 15: On Fpga Clouding And Ubiquitous Mobile Computing Via Em/Mpm And Testile Segmentations And Relevant Mobile Distributed Networks Control (Multi-Core Accelerating) Onusingffe.'Cce.;Ffg./Mnj.;Edf.lopi.klop.cnmh.'Dfg
Ubiquitous.;Rrp Em/Mpm Using Gcc.;Pop Endnamespaces Cce.'Rre'.Vvb
End

Module 16: Auto Multi-Tasking Transformation Algorithm
Usingnamespaces.'Cvbnmhjuyt End

Module 17: Auto Multi-Threading Transformation Algorithm
Usingnamespaces./;'Ddfghyt End

Module 18: Auto Mobile Super-Computerized Design Algorithms By Using Network
Simulator3 (NS3)
Using Ns3 on Fpga and Ccdfgret'.Rre End
Module 19: LLVM Design Algorithms for the Hardware Implementation
Using Ccfghyuuj.';./...Mnj End

4. Hardware Implementation using C++ and llvm Design Protocols

After the Quartus Implementation of a Big IP core for using as a LLVM based GNSS Analysis Mechanism, the three proposed Navigation methodologies need to get implemented and will be made to do the auto data feedback to the LLVM based GNSS Analyzer.

The design patterns for the system's design approach lies in the following ways:

1) Cloud computing and Its direct Hardware Implementation. In the hardware realization on FPGAs, the cloud multi-core-ing design structures are highly welcome, and NOR based Hardware Implementation Design Methodologies are highly preferred.

In Part, the design of a typical Cloud Processing Hardware Core can be written in VHDL as:

Using Namespace Stdio Stdout Stdcc Stdrrk
Using Designs A&B Akb Aeb Arb Acb Cce Picc Css Devc Modelsim Maple Matlab.'Rrs
Using Patterns Matlab Maple Ccf Ggc Gghyuertyu.;.;""Kkl Successfeedbackdfghjkiolp.
End

2) Direct Improvement of Ubiquitous Computing and mobile control Computing by Clouding structures. The VHDL source of the Ubiquitous computing and mobile control computing by the LLVM and Aviation and Grounding Algorithms Are As Follows:

Using Namespace Stdccfghjuy:'*Ccvbnhg:stdio Stdout Stdcc Stdrrk
Using Designs A&B Akb Aeb Arb Acb Cce Picc Css Devc Modelsim Maple Matlab.'Rrs
Using Patterns Matlab Maple Ccf Ggc Gghyuertyu.;.;""Kkl Successfeedbackdfghjkiolp.
End

3) Multi-core-ing processing Unit's design patterns using VHDL and Verilog and C# as Scripts into the FPGA:

C# OCX control protocol modules are:
ccc.'rrf'ffg'ghjklopq'ccv'ccv'bbv''bnmvcdfrew.
Ocx c++ c-- crr cee cdd cff cghjkiuytredsawqzxsadew.'.'//;

The design patterns for the Verilog to get those VHDL IP Cores to work coherently with the C# and the C++ modules are as follows:

Using Namespace Stdio Stdout Stdcc Stdrrk
Using Designs A&B Akb Aeb Arb Acb Cce Picc Css Devc Modelsim Maple Matlab.'Rrs
Using Patterns Matlab Maple Ccf Ggc Gghyuertyu.;.;""Kkl Successfeedbackdfghjkiolp..'Ffghjklacfdertyuiop.
End

Using the namespaces for VHDL and Verilog, the following script core are for linking with FPGA's processing cores and hardware PLLs and hardware ocean type memories on chip:

Using Dsspace Verilog Pli And Verilog Micro Protocol Design Patterns For The Synopthesis Design Compilers
2.26Cce?Rrf;Eed;Rrf;Gfhjuytgfvbnmklopiu. End

As for the above listing, the LLVM design patterns for Unified Navigation using
non-satellite based global navigation is preferrable. This software design patterns can be implemented in NS2 (Network Simulator 2) 2.33 and with the following tcl/tk script to do as experimental verification:

Set topology 1000,000,000 ACMES
Set Output Topologies 1200,000,000
Set Antenna Pole Non
Set Antenna Pole Far Away And Far Infinite Set Propogation Type 1
Set Antenna Type 223 For Global Satellite Gerun
Set Antenna On Earch For 2000,000 As Topologies For Antennas. Run

To analysis and visualize the trace file, the following ns protocol is written, the thoroughput of the successful transmission times are calculated via Tracegraph and the relevant perl file can be written as:

Set Perl Environment 1
Set Perl Awk Limitations 2
Set Perl Thoroughput Auto Calculation 0

Output The Following: Thoroughput For Rts-Cts Udp Trp Internet-Ipv6

The final experimental results can be shown on computer screen. It shows that the

proposed North Pole Global Navigation System can do navigation for atleast 300 Independent objects on their voyage in the sky that is near earth lower than 200Kms from the common sea ground level and 10000 on land and on sea independent objects together. However, some minor errors where encounted when trying to load more aviation objects in substitutive for those on ground objects. A long as the aivation and on ground objects do not exceed the maximum amount listed above, adding or deleting nodes will not suffer from any zero pole or minor axis effects.

For hugh objects such as rockets and war ships and even bands of tanks the design patterns will change since EMC phenomenons will occur.

5. Biography

Feng An, fengan@alumni.purdue.edu, Feng An received his MS from Purdue University, Indianapolis Campus, Purdue School of Engineering and Technology, Department of Electrical and Computer Engineering by the Summer of 2010. His received his BS from Harbin Institute of Technology, Department of Microelectronics, School of Astronautics in 2008.

Feng An is working with Beijing Aerospace Control Device Institute in Beijing, Capital City of China. His research interests include: mobile computing and cloud ubiquitous computing, distributed differential systems design and Modern GPU and CPU design.