Indian Journal of Engineering & Materials Sciences
Vol. 30, August 2023, pp. 550-558
DOI: 10.56042/ijems.v30i4.2047

A New Electronically Tunable Current Differencing Transconductance Amplifier Based Meminductor Emulator and its Application

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Received: 30 May 2023; Accepted: 20 July 2023

In this paper, a simple electronically tunable meminductor emulator based on current differencing transconductance amplifiers (CDTAs) and passive components has been suggested. The proposed CDTA-based emulator is unique as it is memristor-less, uses only a single type of active building block, has simpler circuitry, is electronically tunable, and uses only grounded capacitors. The proposed emulator shows acceptable performance over a broad frequency range. Using the LTSpice tool and 0.18µm CMOS technology, simulations were conducted to test the performance of this emulator. The proposed meminductor emulator's functionality has been examined for the chaotic oscillator and adaptive learning circuit. The satisfactory performance of these circuits confirms the use of the proposed emulator in a practical environment.

Keywords: Current Differencing Transconductance Amplifier (CDTA), Meminductor, Adaptive learning, Chaotic oscillator

1 Introduction

The three basic circuit elements- resistor, capacitor, and inductor were known. A new element memristor was introduced by Prof. Chua in 1971[1]. In the year 2009, meminductor and memcapacitor were introduced as the extended notion of memristor[2] . These elements (memristor, meminductor, and memcapacitor) are commonly referred to memelements. The memelements are defined through four circuit parameters which are defined as q (electric charge), σ, Φ (induced flux), and ρ. Here, σ, Φ and ρ are calculated as the time integral of charge, voltage, and flux respectively. figure. 1 shows the relation among different circuit parameters of the three memelements. A lot of interest has recently been paid to meminductor and memcapacitor technology because of the wide range of applications they have, particularly in the area of neural networks. Since the physical realization of these elements has not been formulated yet, a lot of research has been done to get their emulators. The meminductor emulators suggested in the literature are designed using different analog.

Building blocks (ABBs) and can be broadly categorized as – the ones which are memristor based and the others which are memristor-less. In the year 2013, SPICE modeling of these memelements has been reported in[3] . An additional mutator that transforms memristor into meminductor and memcapacitor, employing second-generation current-conveyor (CCII), resistor, capacitor and a multiplier has been suggested in[4] . In the year 2014, a unique meminductor emulator suggested[5] . The design was unique as no memristor was used. It includes four AD844s, two op-amps, multipliers with resistors, and capacitors only. In the same year, a meminductor emulator with charge-controlled characteristics has been suggested[6]. The suggested design involved three op-amps, a multiplier, and MOSFETs along with resistors and capacitors. Another meminductor emulator with charge-controlled characteristics was outlined in[7] , the design was memristor-less and used four current conveyors, one multiplier, one adder, four resistors, and two capacitors. In 2016, a new meminductor emulator with flux-controlled characteristics utilizing four op-amps, two multipliers, and multiple resistors and capacitors was introduced[8] . In the same year, another meminductor mutator designed from memristor using op-amp based gyrator along with a few resistors and capacitors was suggested[9]. Afterward, OTA-based meminductor and memcapacitor emulators[10] were suggested in the literature. This reported design uses an OTA, along with a voltage reference, inductor and resistor. A universal mutator for realizing both grounded and floating type meminductor and memcapacitor emulator has been suggested in[11] . The design uses five current conveyors along with an AD633 (analog multiplier) resistor, and capacitor. For high-frequency applications, a

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meminductor emulator has been suggested in recent literature. This emulator was designed with the help of two voltage differencing transconductance amplifiers (VDTAs), and two passive capacitors[12] . Another floating mutator used to realize different mem-elements was designed with four AD844s, one op-amp, and one varactor diode, along with resistors and capacitors[13] . In[14] a meminductor emulator based on current buffered transconductor amplifier (CBTA) was suggested, it involved memristor and capacitors. An electronically tunable emulator circuit for memelements has been reported in[15] . The suggested emulator was realized using two OTAs, two multipliers, two resistors, and two capacitors. In recent literature[16], a mutator circuit employing voltage differencing current conveyor (VDCC) was suggested for meminductor and memcapacitor emulators. This design requires a memristor and capacitor. In[17] a meminductor emulator utilizing an op-amp memristor, capacitor and resistor has been reported.

It has been identified through analysis of recent literature that memristors form the basis for the majority of available meminductor emulators, which leads to complex circuitry. The few memristor-less meminductor emulators involve complex analog multipliers and excessive active and passive components. Moreover, the memristor-less emulators were realized using different combinations of active building blocks. This work proposes to design a simplified meminductor emulator circuitry without the need for a memristor or complex multiplier. Further, it uses only a single type of active building block – current differencing transconductance amplifier (CDTA) and requires only two capacitors. CDTA has been chosen in this work as it offers electronic tunability of the OTA[18] block while taking input in current form.

2 Materials and Methods

In this section, the review of the meminductive systems including basic equations has been presented that is followed by the brief explanation of basic active block used for designing the meminductor emulator.

2.1 Review of meminductive systems

Meminductors are considered a type of memelements, which have inductive properties along with memory characteristics. Meminductors form a relation between induced flux Φ (time integral of voltage) and ρ (time integral of flux). Here, ρ and Φ can be mathematically represented by Eq. (1) and (2) as[19,20] :

$$\rho = \int_{\infty}^{t} \Phi(t).\,dt \quad \ldots (1)$$

$$\Phi(t) = \int_{\infty}^{t} V(t).\,dt \quad \ldots (2)$$

The distinctive memory property of the meminductor is extended over its inductive characteristics and therefore the meminductor is defined as:

$$d\rho = M_L\, dq \quad \ldots (3)$$

Using Eqs. (1) and (2), Eq. (3) is modified as:

$$\Phi(t) = M_L\, I(t) \quad \ldots (4)$$

where, Φ(t) is induced flux, I(t) is current and M_L represents meminductance of the system.

2.2 CDTA characteristics

The current differencing transconductance amplifier (CDTA) is an important current mode active building block introduced by Biolek. Its first CMOS-based implementation was given by Keskin and Biolek in 2006[21] . The block diagram representing its various port terminals is shown in Figure. 2.

The CDTA block has five terminals, two are input current terminals (p & n), two are output current terminals (x+ & x-), and z is the intermediate current terminal. V_B is the biasing terminal for the CDTA block. This block can be modified to get multiple output current terminals by adding current repeaters for advanced application of the block. CMOS implementation of voltage tunable multiple output CDTA block diagram is given in Figure. 3[22] .

The CDTA block has high output impedance whereas its input impedance is quite low. Its input terminals are at virtual ground and the differential input current (I_p-I_n) decides the current through the z-terminal and is given as:

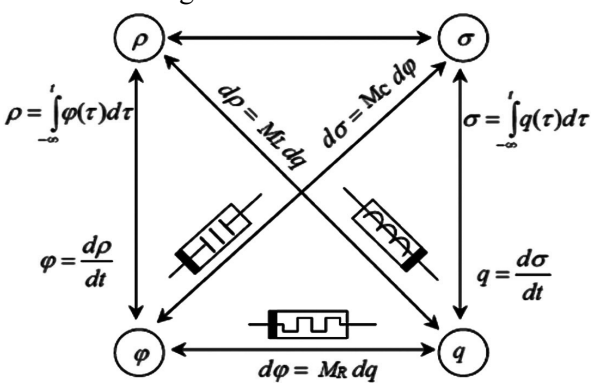

Fig. 1 — Relation between circuit parameters for memelements.

$$V_p = V_n = 0, \quad I_z = I_p - I_n \quad \ldots (5)$$

The voltage V_z developed at 'z' terminal due to external impedance serves as input for the transconductance part of CDTA. This voltage generates output currents I_{x+} and I_{x-} given in Eq. (6):

$$I_{x\pm} = \pm g_m V_z \quad \ldots (6).$$

where g_m is the transconductance of amplifier, which is proportional to biasing voltage (V_B) and is represented by Eq. (7):

$$g_m = \frac{K}{\sqrt{2}}(V_B - V_{ss} - 2V_{th}) \quad \ldots (7)$$

here, K is a transconductance parameter of CDTA and for the MOSFET based circuit depicted in Figure. 3, is given as:

$$K = \frac{\sqrt{\beta_7 \beta_{19} \beta_{20}}}{(\beta_{19}+\beta_{20})} \quad \ldots (8)$$

here, β^n represents a technological parameter of n^{th} MOSFET and is given as: $\mu_n C_{ox} W/L$; where μ_n represents electron mobility, W/L denotes aspect ratio and C_{ox} gives oxide capacitance per unit area.

For multiple output terminals, the relation is shown in Eq. (9)

$$I_{x1\pm} = I_{x2\pm} = \pm g_m V_z \quad \ldots (9)$$

2.3 CDTA based meminductor emulator

The circuit of proposed emulator employing CDTA is represented in Fig. 4. This circuit consists of two multiple-output CDTA blocks and only two capacitors. The first CDTA's Z-terminal receives the input voltage (V^{in}). The amplified current output are achieved at the X+ and X- terminals of this CDTA and are fed to the p and n terminals respectively of the second CDTA. Due to the feedback provided from X- and X+ terminals of the 2nd CDTA at p and n terminals respectively of the 1st CDTA, the input current (I_{in}) turns out to be proportional to input flux. Further, a similar current observed at the 2nd X-terminal of the 2nd CDTA controls V_{B1} through capacitor C_2. This causes the gain of 1st CDTA to be proportional to integral of input flux, leading to the meminductive behaviour of the designed circuit.

The following is a mathematical analysis of the suggested circuit:

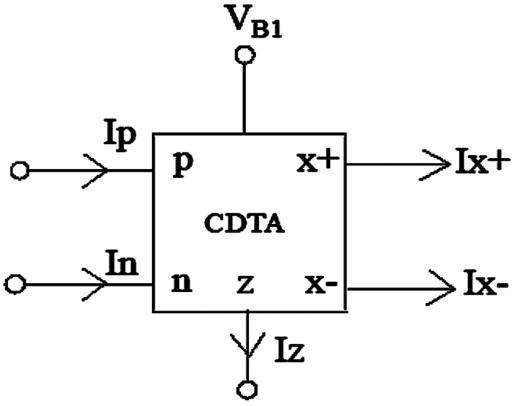

Fig. 2 — current diffrencing transcoductance amplifier block.

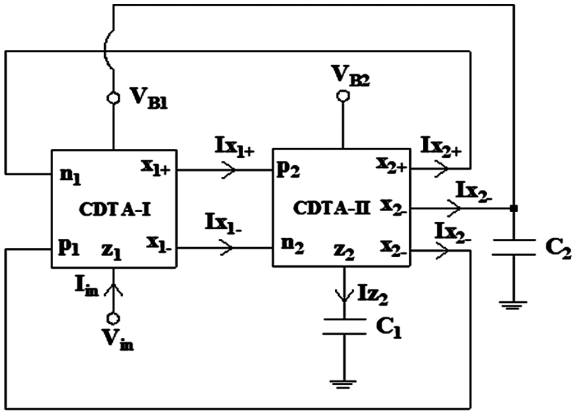

Fig. 4 — Proposed meminductor emulator.

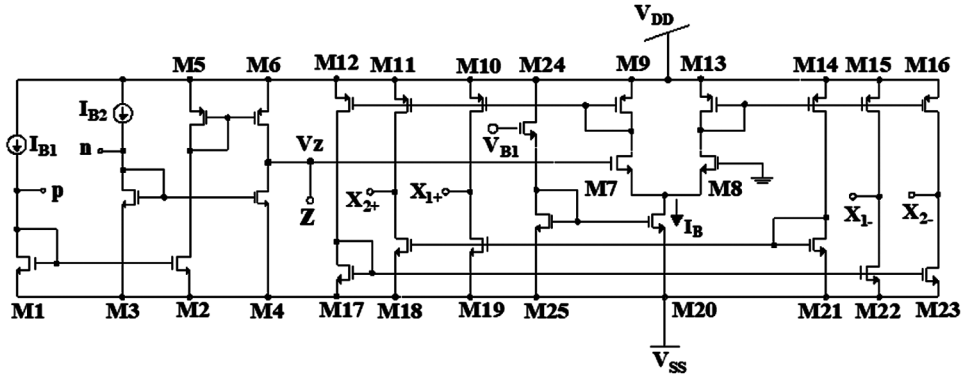

Fig. 3 — CMOS based circuit for multiple outputs CDTA[22] .

Performing routine analysis of Figure. 4 and using Eq. (6), for 1st CDTA I_{X1+} can be given as:

$$I_{x1\pm} = \pm g_{m1} V_{in} \quad \ldots (10)$$

The straightforward analysis of 2nd CDTA, using Eq. (9) along with Eq. (10) gives:

$$I_{x2\pm} = \pm \frac{g_{m2}}{C_1} \int I_{z2} dt \quad \ldots (11)$$

Substituting Eq. (9) and Eq. (10) in Eq. (11), we get:

$$I_{x2\pm} = \pm \frac{2 g_{m1} g_{m2}}{C_1} \int V_{in} dt \quad \ldots (12)$$

From Fig. 4, it can be observed that $I_{in} = -I_{z1}$; thereby, performing routine analysis of Figure. 4, along with Eq. (9) and Eq. (12), I_{in} can be defined as:

$$I_{in} = \frac{4 g_{m1} g_{m2}}{C_1} \int V_{in} dt \quad \ldots (13)$$

Considering, integral of input voltage (V_{in}) is defined as flux ($\varphi_{in}(t)$), Eq. (13) can be defined as:

$$I_{in} = \frac{4 g_{m1} g_{m2}}{C_1} \varphi_{in}(t) \quad \ldots (14)$$

In Figure. 4, biasing voltage of 1st CDTA (V_{B1}) is controlled by voltage developed across C^2, hence, V_{B1} can be given as:

$$V_{B1} = \frac{1}{C_2} \int I_{x2-} dt \quad \ldots (15)$$

Using Eqs. (12) and (15), V_{B1} can be represented as:

$$V_{B1} = -\frac{2 g_{m1} g_{m2}}{C_1 C_2} \int \varphi_{in} dt \quad \ldots (16)$$

$\rho(t)$ is considered to be the time integral of input flux ($\int \varphi_{in1}(t) dt$), thereby, Eq. (16) may be re-written as:

$$V_{B1} = -\frac{2 g_{m1} g_{m2}}{C_1 C_2} \rho(t) \quad \ldots (17)$$

Using Eq. (7), Eq. (14) can be transformed as:

$$I_{in} = \frac{4 g_{m2}}{C_1} \frac{K}{\sqrt{2}} (V_{B1} - V_{ss}) \varphi_{in}(t) - \frac{4 g_{m2}}{C_1} \frac{K}{\sqrt{2}} 2 V_{th} \varphi_{in}(t) \quad \ldots (18)$$

Substituting Eq. (17) in Eq. (18), we obtain:

$$I_{in} = \frac{4 K g_{m2}}{\sqrt{2} C_1} \left(-\frac{2 g_{m1} g_{m2}}{C_1 C_2} \rho(t) \right) \varphi_{in}(t) + \frac{4 K g_{m2}}{\sqrt{2} C_1} (-V_{ss} - 2 V_{th}) \varphi_{in}(t) \quad \ldots (19)$$

The relation of current and flux is given in Eq. (20).

$$I(t) = M_L^{-1}(q) \cdot \varphi_{in}(t) \quad \ldots (20)$$

On comparing Eq. (19) with (20), we get the value of M_L^{-1} (inverse meminductance) of proposed meminductor as:

$$M_L^{-1} = -\frac{4 K g_{m2}}{\sqrt{2} C_1} \left(\frac{2 g_{m1} g_{m2}}{C_1 C_2} \rho(t) \right) - \frac{4 K g_{m2}}{\sqrt{2} C_1} (V_{ss} + 2 V_{th}) \quad \ldots (21)$$

Equation (21) shows that meminductance of proposed meminductor consists of 2 terms: one is variable term dependent on input flux $\left(-\frac{4 K g_{m2}}{\sqrt{2} C_1} \left(\frac{2 g_{m1} g_{m2}}{C_1 C_2} \rho(t) \right) \right)$ and second is fixed term dependent on device and circuit parameters $\left(-\frac{4 K g_{m2}}{\sqrt{2} C_1} (V_{ss} + 2 V_{th}) \right)$

3 Results and Discussion

The suggested emulator design has been simulated using the LTSpice tool and a TSMC 180nm model file. The aspect ratios for CMOS-based circuit of the CDTA block shown in Figure. 3 are shown in Table 1. The supply voltages are considered as ±0.9V and the currents used for biasing of the block have been fixed to $I_{B1} = I_{B2} = 30\mu A$. The bias voltage for the second CDTA block (V_{B2}) is chosen as -0.1V. To perform various analyses, capacitors C_1 & C_2 are fixed at values of 230pF and 565pF respectively.

The transient response of the proposed circuit analyzed for a sinusoidal bipolar signal with an amplitude of 50mV and frequency 10kHz is shown in Figure. 5. This Figure plots the curves for (i) Input Voltage (Vin), (ii) Input Flux and (iii) Input Current. Analyses of these waveforms reveal that the phase of input flux and input current lags the phase of input voltage, a characteristic observed in inductive devices.

Non-volatility is an indispensable fingerprint of a mem-element. To verify this non-volatile behaviour for the suggested meminductor, a pulse signal with amplitude 25mV and time period 8µs with 2µs ON period has been applied to the circuit. The variations

Table 1 — Aspect ratios for CMOS based implementation of CDTA blocks

MOSFETs	W(μm)	L(μm)
M1-M4	32	2
M5-M6	42.5	0.36
M7-M8	16	1
M9-M16	9	1
M17-M19	4	1
M20	14	0.18
M21-M23	4	1
M24-M25	15	0.18

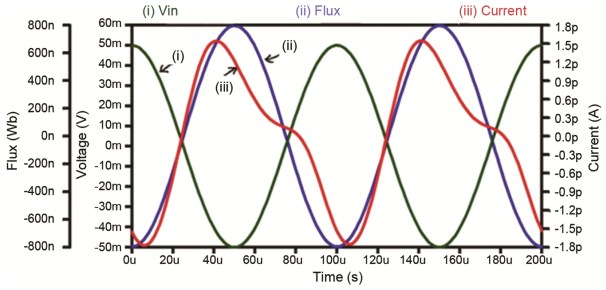

Fig. 5 — Transient response.

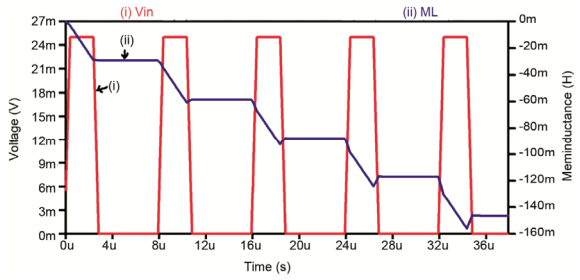

Fig. 6 — Non-Volatility response.

observed in meminductance have been presented in Fig. 6. This Figure shows that for each pulse, the meminductance (M_L) increases during the 'ON' period of the applied pulse, while its value is preserved during the 'OFF' time of the pulse.

To analyze the meminductive behaviour of the suggested meminductor, a 10kHz bipolar signal with 50mV amplitude has been fed to circuit's input terminal. The pinched hysteresis loop (PHL) observed on flux vs current plane has been plotted in Fig. 7 PHL curve obtained with zero-crossing confirms the behaviour of proposed emulator as meminductor.

The response of the proposed meminductor has been studied for sinusoidal signals with different frequencies. To obtain the zero-crossing PHL curve for different frequencies, the capacitors C1 and C2 are scaled. In Table 2, the capacitances utilized for various frequencies have been compiled. The PHL curves observed for frequencies ranging from 30kHz to 500kHz are plotted in Fig. 8.

Table2 — Values of capacitor C_1 and C_2 for different frequencies

Frequency (kHz)	C_1 (pF)	C_2 (pF)
30kHz	50	78
50kHz	20	31
70kHz	8	17
100kHz	3	9
200kHz	2	2.9
300kHz	0.9	1
500kHz	0.5	0.5

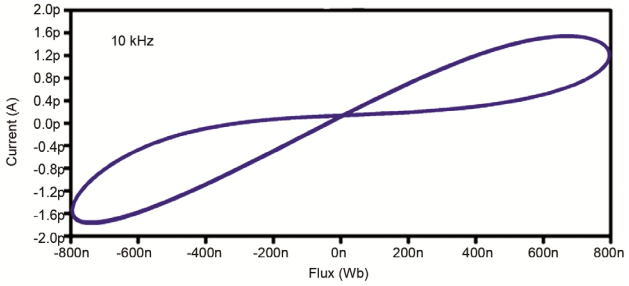

Fig. 7 — PHL response plotted on flux vs current plane.

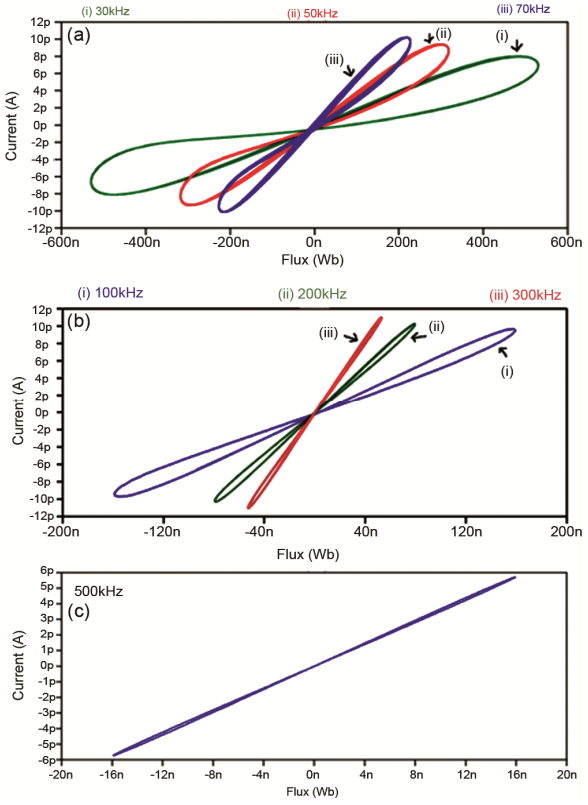

Fig. 8 — PHL curves observed for sinusoidal input signal of frequency: (a) (i) 30kHz, (ii) 50kHz, (iii) 70kHz; (b) (i) 100kHz, (ii) 200kHz, (iii) 300kHz (c) 500kHz.

To study the impact of capacitance variation on PHL curves of the suggested design, its behaviour with a sinusoidal signal of 50kHz, for multiple values of C_2 has been examined. The PHL curves observed

are plotted in Fig 9. From the obtained results, it can be observed that variation in C_2 leads to variation in the PHL loop and the pinching point shifts.

To verify the electronic tunability of the design, variations in PHL curves with changes in biasing voltage V_{B2} of CDTA-2 have been analyzed. For this, the design is simulated with a 50kHz sinusoidal input signal with varying V_{B2}. The observed results are shown in Figure. 10. The curves shown in Fig. 10 clearly depict that variation in V_{B2} leads to variation in the shape of PHL curves, thereby confirming the electronic- tunable characteristics of the design.

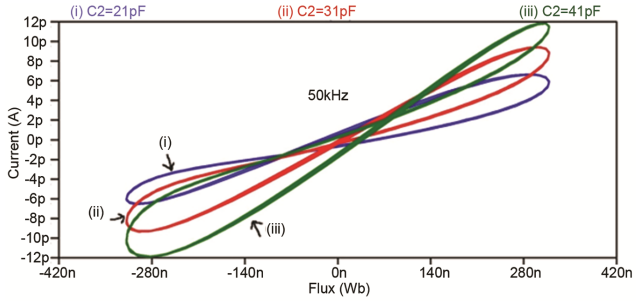

Fig. 9 — PHL curves observed on flux vs current plane with different values of C_2.

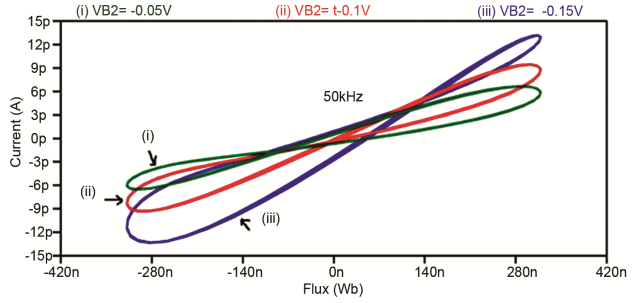

Fig. 10 — PHL response with V_{B2} variation.

3.1 Comparison of proposed emulator with meminductor emulators reported earlier in recent literature

In this section, assessment of the key specifications of the proposed meminductor emulator with previously reported structures available in recent literature is carried out. The comparison summary is presented in Table 3. The key parameters used for the comparison purpose are the count of active and passive elements, PHL frequency range and whether the design requires a memristor or not.

The conclusion of the comparison shown in table 3 is as follows:

1. The proposed meminductor emulator uses only a single type of active building block, as compared to other reported emulators [5-8,11-13] that require different types of active building blocks.
2. The suggested emulator circuit is memristor-less as compared with emulators reported in [4,9,14,16,17], which are memristor-based emulators.
3. For the proposed emulator design the maximum frequency for which the PHL curve can be obtained without distortion is 500kHz, whereas for meminductor emulators reported in [4-8, 10-11, 13-15] it is in the range of a few Hz to 100kHz only. On the other hand, for the emulator reported in[17] the maximum frequency range is up to a few MHz but it requires a memristor for operation.

3.2 Applications

This section presents two different applications namely chaotic oscillator and adaptive learning circuit

Table 3 — Comparison Table between proposed emulator and previously reported emulators

Reference number	Count of active components	Count of passive components	Memristor-less (Yes/No)	Maximum Frequency	Floating(F) Or Grounded (G)
[4]	3 CFOAs	1MR, 2R, 1C	No	20Hz	F
[5]	4 CFOAs, 2 op-amps, 1 multiplier	5R, 1C	Yes	36Hz	F
[6]	3 op-amps, 1 multiplier	2 R, 1 C, 12 MOSFETs	Yes	300Hz	G
[7]	4 CCII, 1 multiplier, 1 Adder	3 R, 1 C	Yes	5Hz	G
[8]	4 op-amp, 2 multipliers	8 R, 2 C	Yes	180Hz	F
[9]	2 op-amp	1MR, 4R, 1C	No	-	F
[10]	1 OTA, 1 voltage reference	1 L, 1 R, 1 C	Yes	500Hz	G
[11]	5 AD844, 1 op-amp, 1 multiplier	5 R, 1 C	Yes	5kHz	F
[12]	2 VDTA, 1 multiplier	2 C	Yes	1MHz	F
[13]	4 AD844s, 1 op-amp, 1 varactor diode	5 R, 2 C	Yes	8kHz	F
[14]	1 CBTA	1 MR, 1C	No	100kHz	F
[15]	2 OTAs, 2 multipliers	2 R, 2 C	Yes	10kHz	G
[16]	1 VDCC	1MR, 1C	No	700kHz	F
[17]	2 Op-amp	1MR,3R, 1C	No	2MHz	G
Proposed	2 CDTA	2C	Yes	500kHz	G

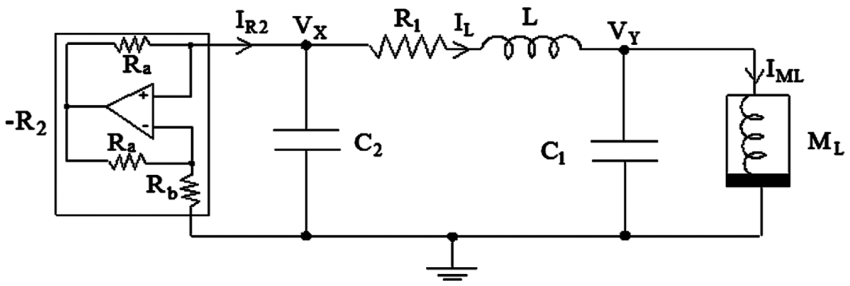

Fig. 11 — Chaotic Oscillator circuit

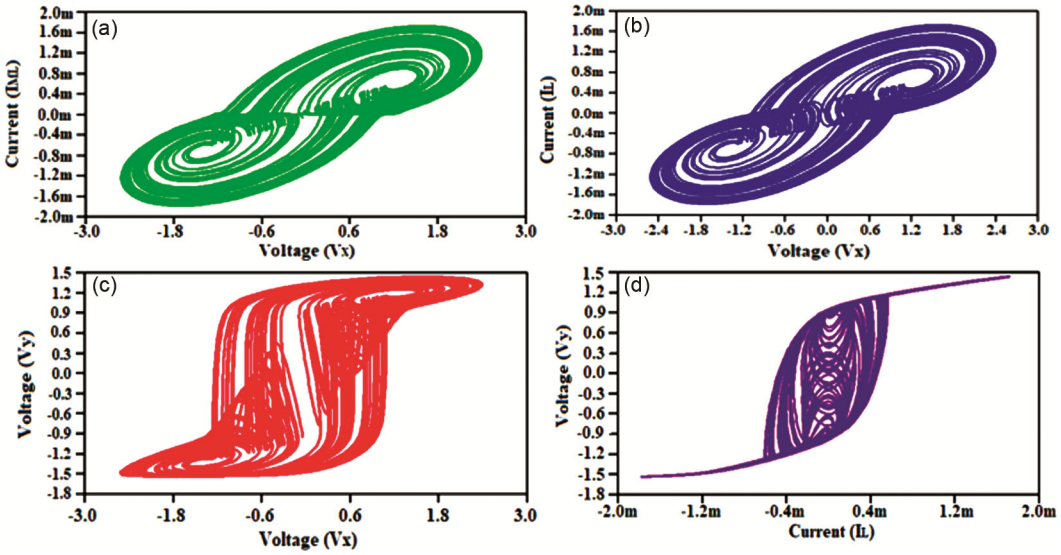

Fig. 12 — 2-D Plots for Chaotic Oscillator Circuit between (a) V_x and I_{ML} (b) V_x and I_L (c) V_x and V_y (d) I_L and V_y .

based on the proposed emulator. These applications verify the workability of the proposed emulator circuit.

3.2.1 Chaotic Oscillator

In this sub-section, the realization of a chaotic oscillator designed with the help of the proposed meminductor emulator circuit has been presented. In order to produce chaotic waveforms, Chua's oscillator is thought to be the most basic type of circuit. A simple form of Chua's chaotic oscillator circuit is drawn in Figure. 11. This oscillator contains a negative resistor (-R2) realized using op-amp based negative impedance converter, two capacitors (C1 & C2), one inductor (L), one resistor (R1) and meminductor (M_L). In this circuit, voltages developed at the capacitor terminal (V_x and V_y), meminductor current (I_{ML}) and inductor current (I_L) are considered as state variables. The first-order differential equations illustrating the dynamics of state space variables of the meminductor-based chaotic oscillator are given as follows:

$$C_2 \frac{dV_x}{dt} = -I_L + \frac{V_x}{R_2} \quad \ldots (22)$$

$$C_1 \frac{dV_y}{dt} = I_L - I_{ML} \quad \ldots (23)$$

$$L \frac{dI_L}{dt} = V_x - V_y - I_L \cdot R_1 \quad \ldots (24)$$

$$M_L \frac{dI_{ML}}{dt} = V_y \quad \ldots (25)$$

The negative resistance ($-R_2$) has been realized with Op-amp based negative impedance converter, taking R_a = 2kΩ and R_b= 2kΩ.The value taken for passive components are L=120mH, C_1=65nF, C_2 =10nF & R_1 =100Ω. The 2-D projection—plots observed between different state space variables are presented in Figure. 12 (a-d).

3.2.2 Adaptive Learning circuit

This sub-section has analyzed and confirmed the suggested meminductor's use in an adaptive learning circuit. An adaptive learning circuit imitates the behaviour of amoeba towards its environmental

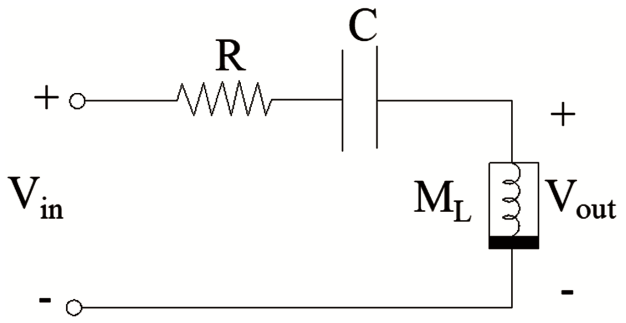

Fig. 13 — Adaptive Learning Circuit.

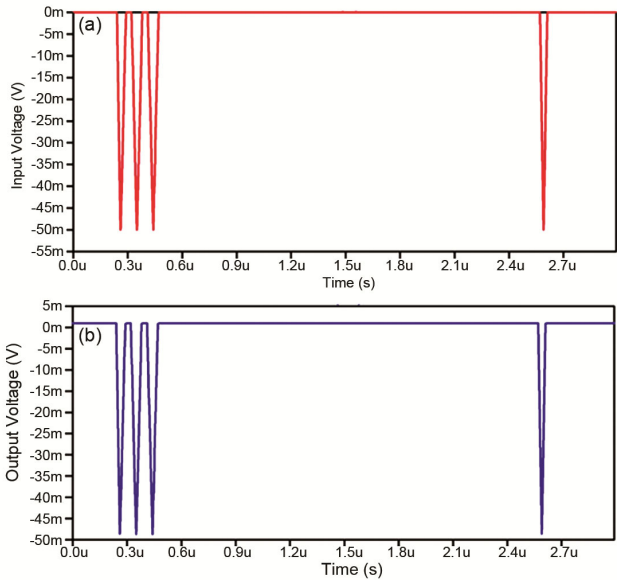

Fig. 14 — Adaptive Learning Response (a) Input (b) Output.

change[23]. The circuit has been developed using passive components (a resistor (R), capacitor (C)), and proposed emulator (M_L) is shown in Figure 13. This circuit simulates an amoeba's locomotive response to a change in its environment. For emulation, temperature gradation in its surrounding is represented by applied input (Vin), and the corresponding behavioural response in terms of locomotive action is represented by output (Vout).

Amoeba's behavioural response to environmental change is a process of learning and remembrance. Amoeba can create appropriate behavioural responses in the future in response to similar environmental variation because they can remember and learn from periodic changes in their environment. The meminductance fluctuations with applied voltage can be used to tune the adaptive learning circuit. The constructed adaptive learning circuit's response, which is depicted in Figure. 13, confirms this behaviour. For simulation the components R=0.5kΩ and C=50nF was used. It may be inferred from the response in Figure. 14 that the output (Vout) varies for 0.5µs in accordance with environmental change represented by input (Vin). It is also observed that for an irregular change after 2.5µs, this circuit considers the previous response. This behaviour is comparable to how amoebae learn and remember things.

4 Conclusion

In this work, a memristor-less CDTA-based grounded meminductor emulator circuit has been proposed. The suggested circuit comprises only a single type of active block (CDTA), along with simple circuitry consisting of two grounded capacitors. The proposed design is free from the requirement of an analog multiplier, adder, memristor, or any other complex circuit. The PHL curves are observed for a wide span of frequency range from 10kHz to 500kHz. The suggested emulator is electronically controlled, and the PHL's shape can be changed by adjusting the bias voltage. The chaotic oscillator and adaptive learning circuit employing the suggested emulator circuit produced satisfactory results, proving the design's viability.

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