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A Low Input Impedance Wide Bandwidth Flipped Voltage Follower Current Mirror

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Current mirror is considered as a fundamental block in the design of analog circuits. For this reason its stable high performance operation has been a key requirement by the IC engineers. A flipped voltage follower based low voltage current mirror with better stability is proposed in this paper. The proposed architecture used super cascode configuration at its output which resulted in boosted output resistance whereas the reduced input resistance is achived through super transistor configuration. Furthermore, an external capacitor is used to suppress the peaking effect observed in the frequency plot. The current mirror showed satisfactory performance with minimal error till 1 milli ampere while the power dissipated ranges in micro watts. The -3db bandwidth found to be around 2.5 giga hertz. The input and output resistances is calculated as 0.407 ohm and 103 mega ohms respectively. The robustness analysis against process and temperature variations is also presented in this paper. The proposed circuit is designed and analyzed using HSpice on 0.18 micrometer mixed-mode twill-well technology with using dual polarity supply of 0.5 volt.

Keywords: Flipped voltage follower, Current mirror, Feedback, Cascade, Resistance

1 Introduction

Low voltage analog circuits are widely used in design of low power analog VLSI systems. Current mirror (CM) is one among such which is said to be a building block of any analog system, most frequently seen in design of current conveyors, comparators[1]. The role of a CM circuit is to generate output current as a function of input. This output should be produced at a high impedance node by which the output current becomes constant & do not change with load variation. The parameters governing its performance include operating range which should be high, the bandwidth should be also high, input resistance to be ideally zero and output resistance to be ideally infinte. Apart from these, the supply voltage requirement is also an important factor which affects the circuit performance. To address this, techniques have been reported in literature, applying which enables the current mirror to work efficiently at reduced supply. Few highly cited low voltage low power current mirror circuits reported in literature[2] is basically based on - bulk-driven[3-5], floating gate[6-7], quasi-floating gate[8,9] and bulk-driven quasi-floating gate[10-12]. For low voltage operation, the aforementioned techniques uses an auxiliary input to take care of threshold & makes input signal path free from its effect. However, few of these lead to reduced transconductance of MOS transistor due to which input resistance of current mirror cannot be reduced to the expected level. Besides these techniques do need additional fabrication cost. However, the voltage operation can also be achieved by using low voltage cells for circuit implementation, rather than going for special devices. For example- the flipped voltage follower[13] (FVF) is extensively being used to build the circuits for sub-volt operation. The FVF is basically a cascode amplifier with a negative shunt feedback. The advantage with FVF is its low impedance output node. From CM point of view, the objective of reduced input resistance can be easily accomplished through this node. The low voltage CMs based on such concept can be found in literature[14-19]. In this paper, a low voltage FVF CM having better performances in terms of operating range, better frequency response and resistances both input as well as the output is proposed.

2 Materials and Methods

The voltage follower/source follower/common drain, is mainly used for buffering and so demands for high input and relatively low output resistances, with a large swing. Considering the conventional design, i.e. common drain configuration, such impedance levels cannot be achieved.

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2.1 FVF Current Mirror

In this context, the FVF structure shown in Fig. 1(a) is widely used. The structure represents a cascode with a shunt feedback. The node impedance at the output is relatively very low compared to conventional source follower, i.e. scales down by a factor of ($g_m r_0$). Performing analysis shows the value to be ($1/gm_2gm_{1r01}$) where gm_i and r_{0i} are the transconductance and output resistance of transistor M_i respectively. The conventional FVF CM design is shown in Fig. 1(b).

As can be observed, it use four N-channel transistor (M_1-M_4) where M_3 with I_{B1} current source creates a negative feedback resulting in a low impedance at M_1 drain terminal. This node can be used as input[18] (I_{in}). As I_{B1} is a fixed current source the input signal variation is causes change in gate-to-source voltage M_1 gets reflected to M_2 and accordingly changes M_2 drain current. The applied DC V_{bias} ensures transistors M_3 & M_4 to be in saturation. Performing analysis showed input resistance in range of ohms calculated as ($1/gm_1gm_3r_{03}$) and the output ranges in kilo ohms calculated as ($gm_4r_{04}r_{02}$).

2.2 Proposed FVF Current Mirror

This section presents in brief the proposed FVF CM which enhances the parameters of FVF CM and modifications supported by mathematical analysis of parameters governing the performance. The architecture of proposed design is shown in Fig. 2.

The current mirror architecture consists of N-type MOS transistors (M_1-M_8). An offset current (I_{offset}) of very small value is added to the output MOS transistor to reduce the current mismatch. The working principle remains similar to FVF current mirror discussed earlier. For boosting output resistance, the super cascode stage is incorporated from where the output is extracted. Such change introduces an extra component $(g_m r_0)^2$ in output resistance. The said cascode stage is implemented through M_5 and M_6 where M_6 is driven by the drain potential of M_4 via the inverting amplifier. Using M_5 and I_{B5} inverting amplifier is realized which is also responsible for additional impedance boosting. The effective output resistance calculated is observed to be in the range of mega ohms. However, the

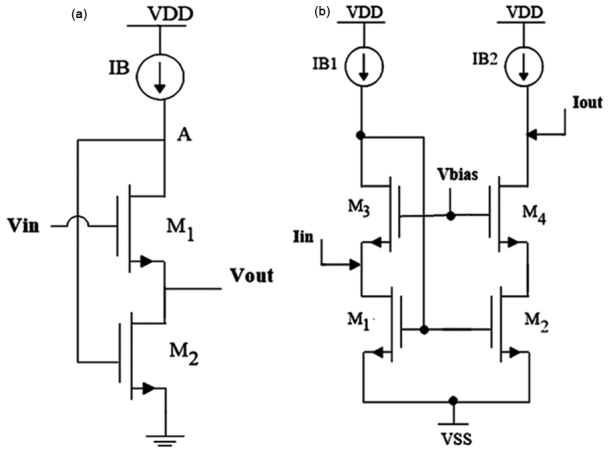

Fig. 1 — (a) Flipped Voltage follower, & (b) FVF Current Mirror.

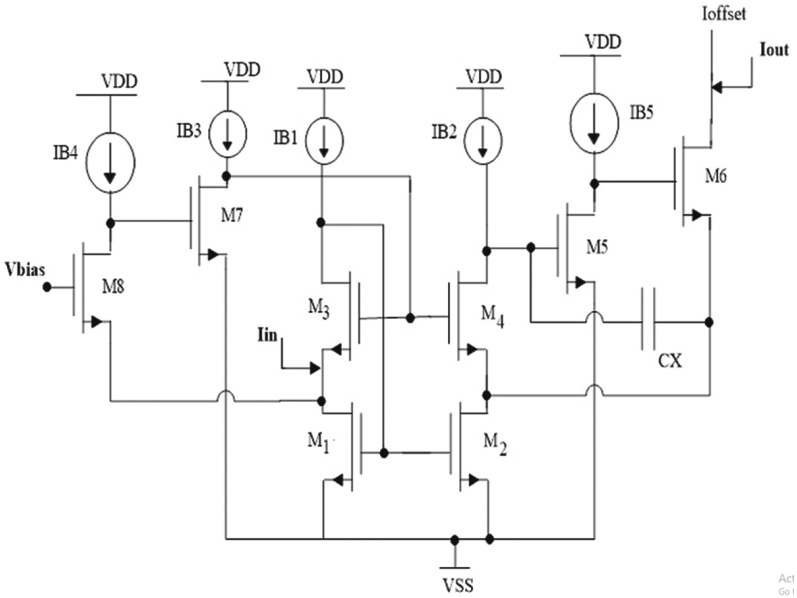

Fig. 2 — Proposed High performance FVF current mirror.

inverting amplifier shows a miller capacitance effect due to which a peak in the frequency plot is seen at high frequency. To suppress, a capacitor C_x is used at its input which ensures the current mirror stability at high frequency. Further improvement is achieved in reduced input resistance by using feedback configuration similar like used in output. The MOS transistors added as M_7 and M_8 along with M_3 forms a local feedback loop. These two changes together scales down the input resistance to a very lower value. The DC current sources I_{B3} and I_{B4} are used to bias the MOS transistors M7 and M8. Compared to conventional FVF CM, the input resistance scales by a factor of $(g_m r_0)^2$.

2.2.1 Frequency response

The small-signal model for current gain calculation is shown in Fig. 3.

Here

$$i_{in} = \frac{C_{gs3}\left(C_{gs1}+C_{gs2}\right)}{g_{m3}} \left(s^2 + \frac{g_{m3}}{C_{gs3}}s + \frac{g_{m1}g_{m3}}{C_{gs3}\left(C_{gs1}+C_{gs2}\right)}\right)V_1 \quad \text{... (1)}$$

$$i_{out} = \frac{g_{m2}g_{m5}g_{m6}\left(g_{m4}+sC_X\right)}{\left(\left(g_{m4}g_{m5}C_{gs6}+g_{m5}g_{m6}C_X\right)s+g_{m4}g_{m5}g_{m6}\right)}V_1 \left(C_{gs5}C_{gs6}C_X + C_{gs4}C_{gs5}C_{gs6} + C_{gs4}C_{gs6}C_X\right)s^3 + \left(g_{m5}C_{gs6}C_X + g_{m4}C_{gs5}C_{gs6}\right)s^2 + \quad \text{... (2)}$$

From (1) & (2)

$$g_{m2}g_{m3}g_{m4}g_{m5}g_{m6}\left(1+\frac{C_X}{g_{m4}}s\right)/$$

$$A_{I,prop.} = \frac{\left(C_{gs1}+C_{gs2}\right)C_{gs3}C_{gs4}C_{gs5}C_{gs6}}{\left(\left(1+\frac{C_X}{C_{gs4}}+\frac{C_X}{C_{gs5}}\right)s^3\frac{g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}}\right) + \left(\frac{g_{m5}C_X}{C_{gs4}C_{gs5}}+\frac{g_{m4}}{C_{gs4}}\right)s^2 + \left(\frac{g_{m4}g_{m5}}{C_{gs4}C_{gs5}}+\frac{g_{m5}g_{m6}C_X}{C_{gs4}C_{gs5}C_{gs6}}\right)s + \left(s^2+\frac{g_{m3}}{C_{gs3}}s+\frac{g_{m1}g_{m3}}{C_{gs3}\left(C_{gs1}+C_{gs2}\right)}\right)} \quad \text{... (3)}$$

$$A_I = \frac{g_{m2}g_{m3}g_{m4}g_{m5}g_{m6}/\left(C_{gs1}+C_{gs2}\right)C_{gs3}C_{gs4}C_{gs5}C_{gs6}}{\left(s^3+\frac{g_{m4}}{C_{gs4}}s^2+\frac{g_{m4}g_{m5}}{C_{gs4}C_{gs5}}s+\frac{g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}}\right)\left(s^2+\frac{g_{m3}}{C_{gs3}}s+\frac{g_{m1}g_{m3}}{C_{gs3}\left(C_{gs1}+C_{gs2}\right)}\right)} \quad \text{... (4)}$$

The equation (3) is the transfer function of the proposed FVF CM. The necessary condition required for stability is when $\left(\frac{g_{m4}}{C_{gs4}}+\frac{g_{m6}}{C_{gs6}}\left(\frac{C_X}{C_{gs4}}-1\right)\right)>0$. Since $C_X > C_{gs4}$, the proposed current mirror remains inherently stable. However, in the absence of C_X equation (3) reduces to equation (4), and the required condition to maintain stability in (4) is met only when $\left(\frac{g_{m4}}{C_{gs4}}-\frac{g_{m6}}{C_{gs6}}\right)>0$ which may not be always possible.

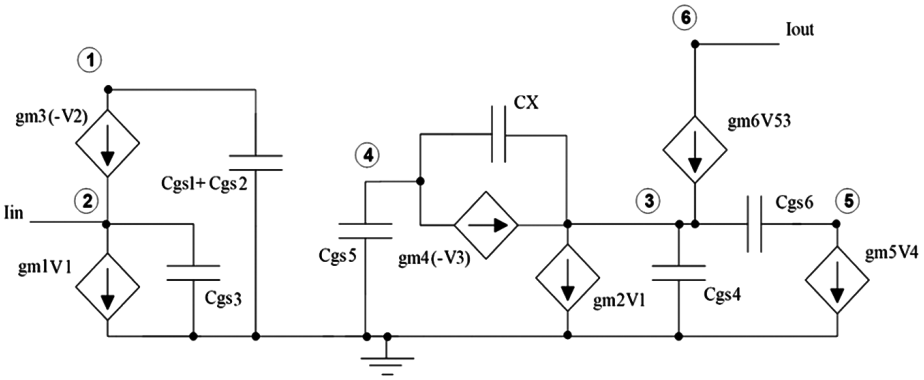

Fig. 3 — Small signal model for calculating current gain.

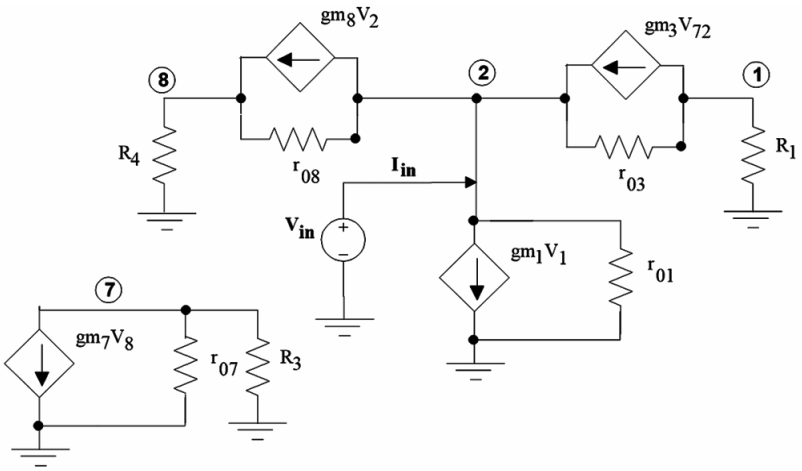

Fig. 4 — Small signal model for calculating input resistance.

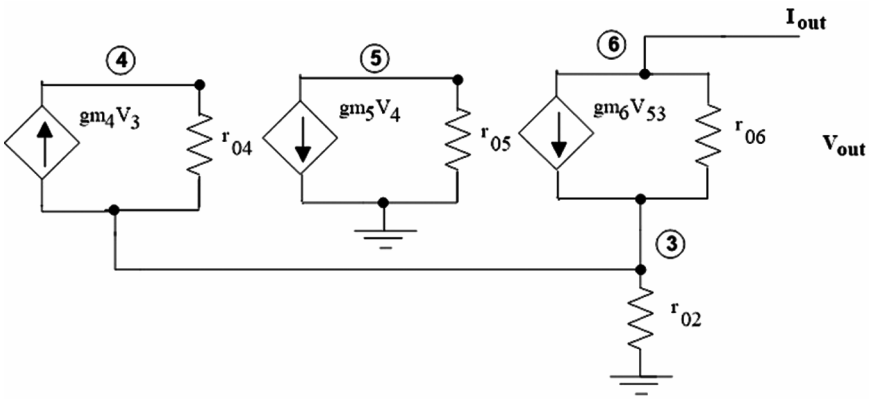

Fig. 5 — Small signal model for calculating output resistance.

2.2.2 Input Resistance

The small signal model for input resistance ($R_{in,prop.}$) calculation is shown in Fig. 4. The R_1, R_3 and R_4 are the impedances of current source I_{B1}, I_{B3} and I_{B4} respectively.

Solving

$$i_{in} \approx g_{m1}g_{m3}g_{m7}g_{m8}\left(R_1 // r_{03}\right)\left(R_3 // r_{07}\right)\left(R_4 // r_{08}\right)V_2 \quad \ldots (5)$$

Assuming ideal sources, $R_1 = R_2 = R_3 = R_4 = \infty$

$$R_{in,prop.} = \frac{V_2}{i_{in}} \approx \frac{1}{g_{m1}\left(g_{m3}r_{03}\right)\left(g_{m7}r_{07}\right)\left(g_{m8}r_{08}\right)} \quad \ldots (6)$$

It is clear from (6), the input resistance gets scale down by $(g_{m7}r_{07})$ $(g_{m8}r_{08})$ times.

2.2.3 Output Resistance

The small signal model for output resistance ($R_{out,prop.}$) is shown in Fig. 5.

Solving

$$V_6 \approx \left(g_{m4}r_{04}\right)\left(g_{m5}r_{05}\right)\left(g_{m6}r_{06}\right)r_{02}i_{out} \quad \ldots (7)$$

Table 1 — W and L of MOS transistors used in proposed CM

Transistors	W(μm)	Other parameters
M1, M2	25	Supply= ± 0.5V,
M3, M4, M6, M8	5	IB1=IB2=10uA,
M5	2	IB3=IB4=20uA, IB5=15uA,
M7	0.24	Cx=200fF

$$R_{out,prop.} \approx \left(g_{m4}r_{04}\right)\left(g_{m5}r_{05}\right)\left(g_{m6}r_{06}\right)r_{02} \quad \ldots (8)$$

It is clear from (8), applying the cascode at its output boosts the resistance by (gm_5r_{05}) (gm_6r_{06}) times.

3 Results and Discussion

The proposed FVF CM is designed using MOS transistor in 0.18 micron mixed-mode twin-well technology at ± 0.5V supply. The channel length of transistors have been kept at 0.24 micron. The widths & other parameters considered is summarized in Table 1.

The Fig. 6 shows the current transfer characteristic and Fig. 7 percentage error in current transfer

respectively. The output keep track of input current with minimal error. Also the error is less for high input current, i.e. the plot varies from 10% for low input current and further decreases to less than a percent for higher values.

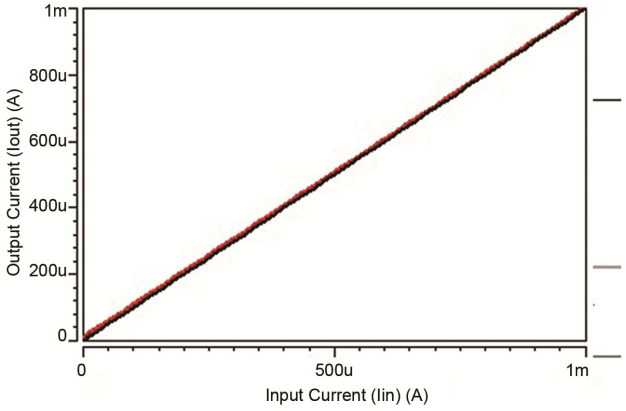

Fig. 6 — Current transfer characteristic.

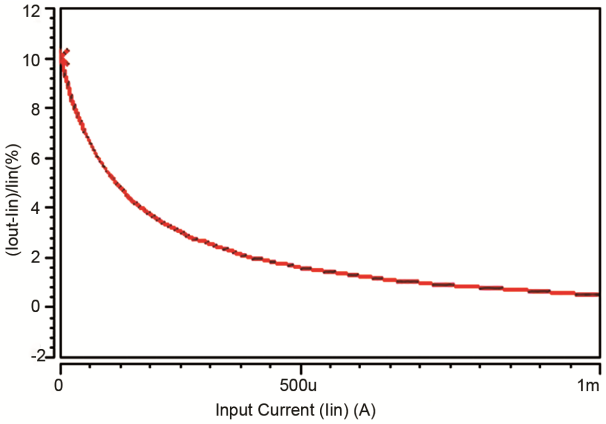

Fig. 7 — Error in current transfer.

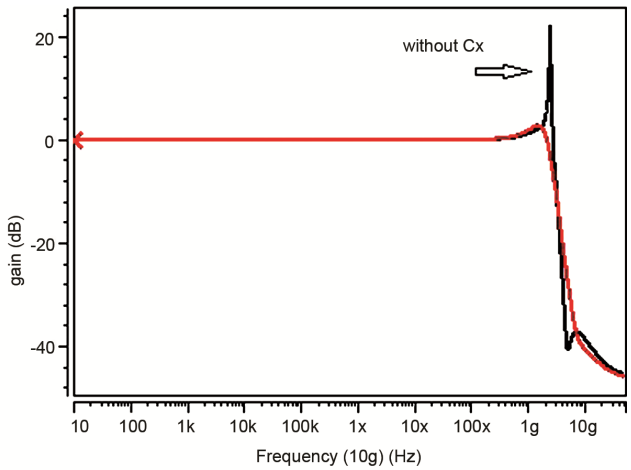

Fig. 8 — Frequency plot.

The Fig. 8 is the frequency response plot of proposed FVF CM. As discussed earlier, a peak is observed in frequency plot in the absence of capacitor Cx where the bandwidth is around 2.8 GHz. Using Cx, the bandwidth do not degrade and is calculated to be 2.5 GHz. The other parameter like resistances, the input resistance due to presence of feedback gets reduced to a value lesser than an ohm, i.e. 0.407 ohm while the output resistance ranges in mega ohms, i.e. 103M ohm.

The robustness against environmental variations of proposed FVF CM is done with the help of process corner analysis and temperature variation. The three process corners considered is Slow, Typical and Fast. The temperature analysis is carried from -25°C to 75°C in the steps of 25°C. The said analyses is performed for percentage error as shown in Fig. 9 while the temperature variation effects is shown in Fig. 10.

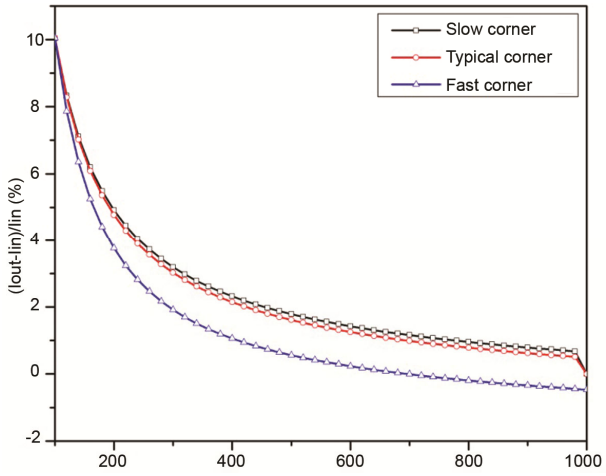

Fig. 9 — Percentage error at different process corners.

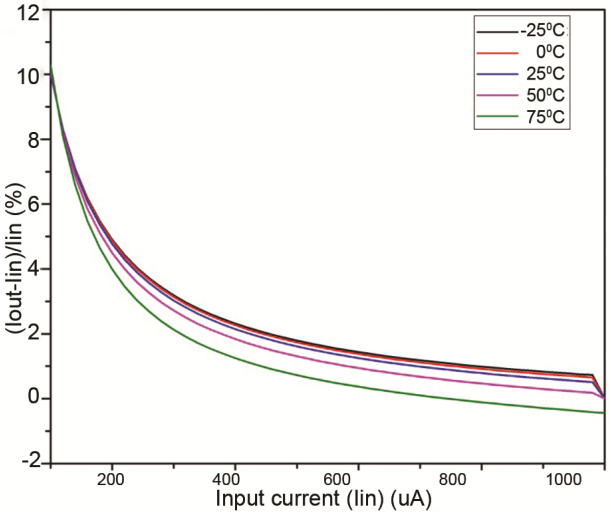

Fig. 10 — Percentage error at varying temperatures.

Table 2 — Comparison of parameters

Parameters	[14]	[15]	[16]	[17]	[19]	This work
Input current range (uA)	300	100	1000	0-200	0-500	0-1000
Current transfer error (%)	0.28	0.6	0.16	0.22	0.409	0.54
Input resistance (ohm)	12.8	496	68.3	130	17	0.407
Output resistance (ohm)	39.5G	1M	10.5G	9.5G	750K	103M
Bandwidth (Hz)	216M	181M	402M	2.7G	4.5G	2.5GHz
Supply (V)	1	0.9	1	0.8	± 0.5	± 0.5
Power (uW)	42.5	150	110	79.33	140	160
Technology (um)	0.18	0.18	0.18	0.18	0.18	0.18

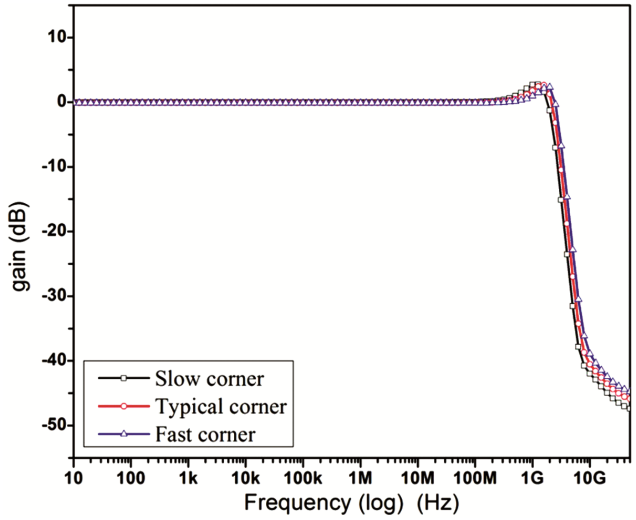

Fig. 11 — Frequency plot at different process corners.

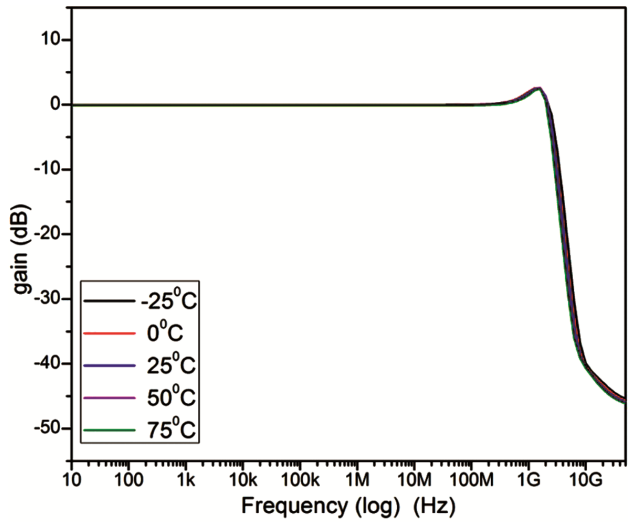

Fig. 12 — Frequency plot at varying temperatures.

Similarly, the frequency plot is analyzed on aforementioned process corners is shown in Fig. 11 and the temperature variations is shown in Fig. 12. The complete results of proposed FVF CM are summarized in Table 2 along with comparison with relevant current mirrors.

4 Conclusion

A sub-volt low power high performance robust current mirror circuit was proposed in this paper. As seen the architecture incorporated the FVF stage at input stage, due to which not only low voltage operation was achieved but also the low impedance output node of FVF helped to achieve reduced input resistance in ohms which finally reduced to 0.407 ohms. For such improvement, the used feedback topology do not required any compensation approach as it has been locally generated. The similar concept was used for increasing the output resistance. The super cascode topology at its output introduced twice the intrinsic gain factor in output resistance and the proposed current mirror showed output of 103 mega ohms. The bandwidth achieved was 2.5 giga hertz which can be beneficial in high speed system designs. The values obtained through simulations well match to the mathematical analysis carried. Also the robustness analysis against mismatches encourages its wide applicability for high speed portable electronic devices.

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