# Diamond Chip

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## Abstract

The aim of this paper is to review emerging technology "Diamond Chip" also known as Carbon Chip. Electronics without silicon is unbelievable, but it will come true with the evolution of Diamond or Carbon chip. Now a day we are using silicon for the manufacturing of Electronic Chip's. It has many disadvantages when it is used in power electronic applications, such as bulk in size, slow operating speed etc. Now research people found that Carbon is more advantages than Silicon. By using carbon as the manufacturing material, we can achieve smaller, faster and stronger chips. They are succeeded in making smaller prototypes of Carbon chip. They invented a major component using carbon that is "CARBON NANOTUBE", which is widely used in most modern microprocessors. Manufacturers plan to build a diamond chip that can withstand temperatures of 500 C, compared to only about 150 C for silicon chips. The chips would be most useful in devices located near hot-burning engines, such as those used in automobiles or airplanes.

## 1. Introduction

Diamond chip or carbon chip is an electronic chip manufactured on a Diamond structure Carbon wafer. Japanese microphysist S.IIJIMSb had already invented a major component in Diamond Chip i.e. CARBON NANO TUBE (CNT). Carbon nano-tubes were discovered in 1991. It is a nano -size cylinder of carbon atoms. They are made of one or several concentric walls in which carbon atoms are arranged in hexagonal pattern, measuring several tens of microns in length and less than a few nanometers in diameter. Imagine a sheet of carbon atom, which would look like a sheet of hexagon. If you role that sheet you get a CARBON NANO TUBE, its property depend on how it is made how the sheet is rolled.

### 1.1 Description of carbon tube

There are two types of carbon nano tube. They are
1. Metallic Carbon Nanotube
2. Semiconducting Carbon Nanotube

**Metallic Carbon Nanotube** is defined as a Nanotube, which exhibit metallic properties. The band gap is approximately zero in this case. Multi walled nanotube's are mostly metallic. This is mainly used of interconnection inside the chip. These ones offer small resistance to current. So the current loss is very small in carbon nanotubes.

**Semi conducting nanotube** is defined as a Nanotube, which exhibit semiconductor properties. Usually semi conducting Nanotube have a narrow energy band gap of 0.3 eV and above. All single walled carbon nanotube are semi conducting. Semi conducting carbon nanotubes are more important compared with that of metallic carbon nanotube. For the manufacturing of active electronics devices, semi conducting carbon nanotube are used. Pure Diamond structural carbon is non-conducting in nature. In order to make it conducting we have to perform doping process. We are using **Boron** as the **p-type** doping Agent and the **Nitrogen** as the **n-type** doping agent. The doping process is similar to that in the case of Silicon chip manufacturing. But this process will take more time compared with that of silicon because it is very difficult to diffuse through strongly bonded diamond structure.

**Figure.1** *Pattern arrangement of carbon atoms.*

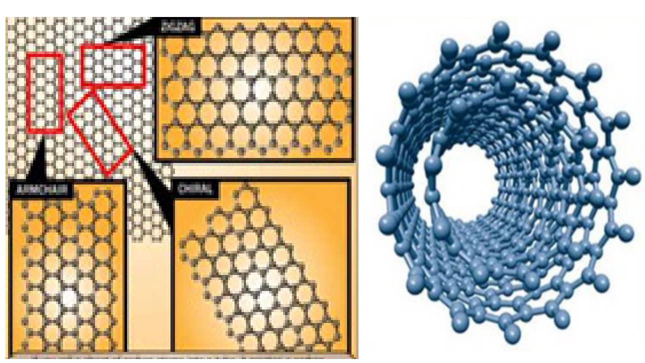


Figure1, specifies that if you roll a sheet of carbon atoms into a tube, it creats a carbon nanotube. Depending on the direction the sheet is rolled into different pattern emerge. With the right arrangement of carbon atoms, a carbon nano-tube can be hundreds of times stronger than steel, but six times lighter.

### 1.2 Production methods of carbon nanotube

There are various production methods. Three main methods are:

1. Arc discharge method.
2. Pulsed laser evaporation.
3. Silicon carbide vaporisation.

### 1.3 Arc discharge method

The arc-plasma evaporation of pure graphite rods led to the discovery of carbon nanotubes (CNTs) by Iijima. The arc apparatus used was the same as that for the production of ultrafine SiC particles by a gas evaporation method. CNTs were obtained in the cathode deposit prepared by a dc arc discharge method in rarefied He gas. The cathode deposit was obtained as a byproduct of fullerene production by the arc discharge evaporation of pure graphite rods. The arc discharge method for producing fullerene is a modification of Krätschmer's method for evaporating two carbon rods in contact by ac resistance heating. By separating the contact and applying a dc arc discharge between two pure carbon rods, the evaporation of the anode carbon realized the mass production of fullerene. This arc evaporation of carbon electrodes produced a deposit on the cathode, which included multiwalled carbon nanotubes (MWNTs). The smallest innermost tube of MWNTs was obtained by this method in pure hydrogen gas ambient. By a method similar to that for MWNT production, but using graphite rods including catalytic metals, single-walled carbon nanotubes (SWNTs) were discovered in chamber soot (not in cathode deposit).

**Figure.2** *Arc-evaporation apparatus for producing CNTs, which is a vacuum chamber.*

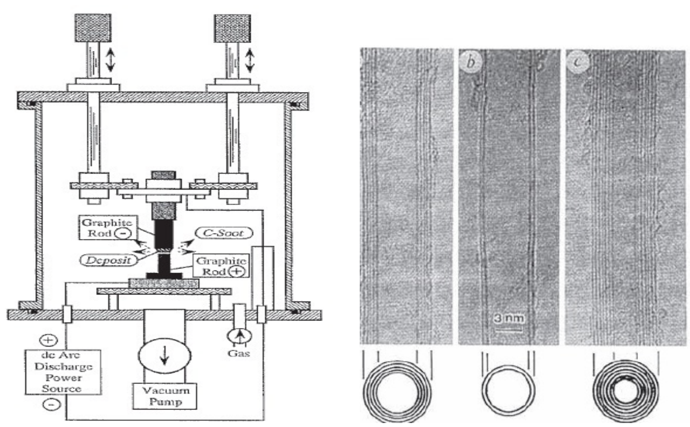
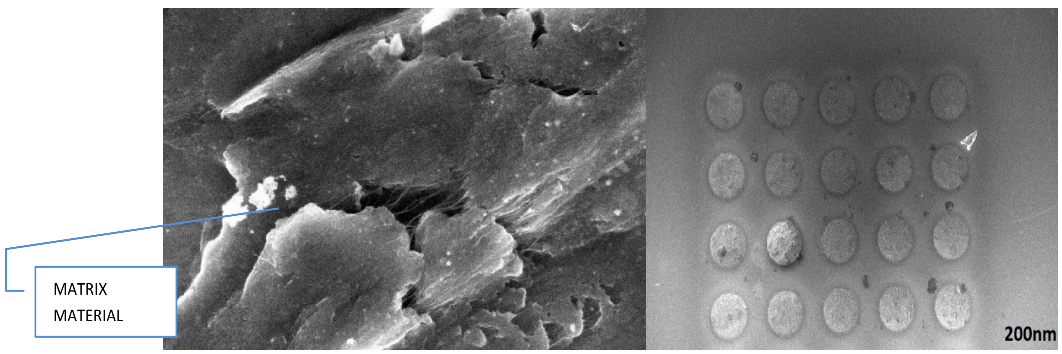



Figure2, of the arc-evaporation apparatus for producing CNTs, which is a vacuum chamber. Two graphite electrodes are installed vertically, and the distance between the two rod tips is maintained in the range of 1–2 mm. After the evacuation of the chamber by a diffusion pump, rarefied ambient gas is introduced. When a dc arc discharge is applied between the two graphite rods, the anode is consumed, and fullerene is formed in the chamber soot. Then, part of the evaporated anode carbon is deposited on the top of the cathode; this is called the 'cathode deposit'. On the top of cathode A, a deposit having columnar texture B is formed, and its thickness d is approximately 6 mm. Part C is the top of the cathode deposit facing the anode. Iijima observed samples obtained from region B by transmission electron microscopy (TEM) and found MWNTs. Region A is the tip of the cathode. Region B has a columnar texture and contains MWNTs. Region C is the top of the cathode deposit facing the anode. Region D shows hard graphite layers. d is the thickness of the deposit. HRTEM micrographs of first MWNTs discovered by Iijima. Symmetrical parallel lines correspond to the projections of graphene sheets coaxially arranged with a constant spacing of 0.34 nm. New Diamond and Frontier Carbon Technology, lines around the central line correspond to the projections of graphene sheets coaxially arranged with a constant spacing of 0.34 nm. The central part with no contrast is the real projection of the tubes.

### 1.4 PULSED LASER EVAPORATION

Using the Matrix-Assisted Pulsed Laser Evaporation (MAPLE) process developed at the Naval Research Laboratory, carbon nanotubes and carbon nanotube composite thin films have been successfully fabricated. MAPLE is conducted in a conventional vacuum chamber equipped with a window of high transmittance for the wavelength of the pulsed laser to be used. The target is a frozen matrix consisting of a volatile solvent, e.g., water, methanol, chloroform, etc., and a low concentration of the film materials, in this case SNW and a polymer which is dissolved in the solvent. The criteria for choosing the volatile solvent are high absorption of the laser light; high solubility for the polymer of choice; and is volatile at room temperature which allows it to be pumped away quickly. The substrate is placed directly in front of the target. Deposition proceeds by illuminating the target with laser pulses. The laser pulse initiates a photo-thermal process, vaporizing the frozen solvent, and releasing the solute and SWN into the chamber. The momentum, resulting from the vaporization process, carries the solvent, solute, and SWN to the substrate. Because the solvent has a high vapor pressure at room temperature, it will rapidly be removed by the pumping system. The polymer and SWN will then form a continuous and dry film. The key to the MAPLE process is that the laser interaction occurs primarily with the solvent molecules, the polymer and SWN should be undamaged and remain intact**.** The as-received SWN are suspended in toluene with a trace amount of NaOH and some particulate of soot or graphite. The toluene is first removed by evaporation or pumping and replaced by chloroform. To make the MAPLE target, 1.1 gm of polymer, either polystyrene (PS) or polyethylene glycol (PEG), is mixed with 25 gm of solution. Because the ratio of SWN to chloroform cannot be determined, the exact ratio of SWN/polymer in the target is not known. A drop of the as-received SWN solution is allowed to dry on a piece of Si forming a SWN film (Figure.3).

**Figure.3** *Pulsed Laser Evaporation in small area*

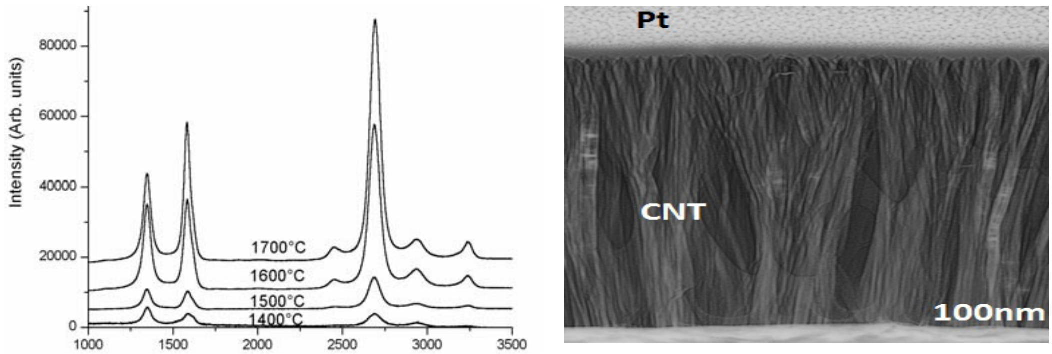



## 1.5 Silicon Carbide Vaporisation

Aligned carbon nanotubes (CNT's) are formed on the surface of silicon carbide (SiC) wafers during high temperature anneals. The exposed 4H SiC surface transforms into CNT's for temperatures in the range of 1400-1700°C and under moderate vacuum conditions (10-2 – 10-5 torr). The rate of formation on the C face (0001¯) is about three times the rate on the Si-face (0001), but both rates increase with anneal temperature. SEM, TEM and Raman scattering measurements have confirmed the presence of both single-wall and multi-wall CNT's. The carbon source is believed to be residual carbon from the SiC left on the surface after preferential evaporation of Si. CNT formation is believed to be catalyzed by low concentrations of residual oxygen in the chamber. Patterning of both n-type and semi-insulating substrates with Si3N4 masks, prior to annealing, results in CNT-free regions. Vertically aligned carbon nanotubes are desired for applications in vacuum microelectronics as field emission devices. The growth method primarily used to form dense arrays of vertically aligned carbon nanotubes (CNT's) is metal catalyzed chemical vapor deposition. An unwanted result from this method is that the CNT's retain the catalyst after the growth procedure. A catalyst-free CNT growth method dubbed "surface decomposition" results from heating silicon carbide (SiC) wafers in a vacuum furnace. However, the growth mechanism and structural and electrical properties of the CNTs by this method have not been fully understood.

In this work, we report on the growth and characterization of aligned CNT films with the "surface decomposition" method on bulk SiC substrates. Commercial grade 4H-SiC substrates were used for this study, including both n-type and semi-insulating substrates. Samples were placed on a graphite stage in a resistance-type furnace with either the Si face (0001) or C-face (0001¯) exposed. The samples were then turbo pumped to a moderate vacuum (10-5 Torr) and annealed at 1700oC for set time intervals between 30 min and 5 hours. Additionally, for patterning experiments, one half of the sample surface was masked with Si3N4 prior to insertion in the furnace. After annealing, the masked regions no longer contained Si3N4, did not develop CNT's, and instead a graphite layer was formed. Micro-Raman spectroscopy confirmed the nanotube nature of the films. Generally, the spectra show a multi-component composition including single wall CNT's, multi-walled CNT's, and graphitic structures. Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM), and transmission electron microscopy (TEM) were also used to characterize the CNT's. The effects of variations in growth time, temperature and vacuum level on CNT characteristics are reported. For electrical characterization of the CNT's, Ni contacts were evaporated on the CNT and non-CNT surfaces. The current vs. voltage (I-V) characteristics were measured across these structures using a general-purpose source-meter. Figure.4, evaluate the I-V results on semi-insulating and n-type substrates for potential device applications.

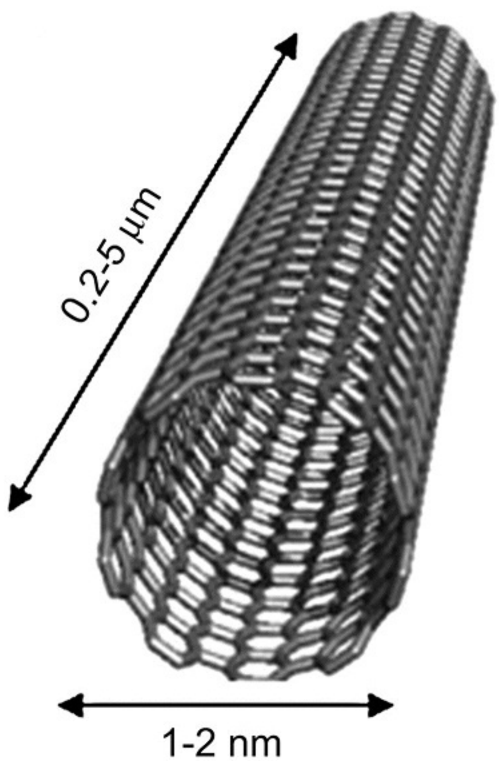
**Figure. 4** *Characteristics plot and description of carbon nano-tube*




### 1.6 Single Walled carbon nanotubes

Single Walled Nanotube is a nanotube, which has only one graphite layer. It is assumed that one graphite layer is taken and it is folded in a cylindrical shape to make a carbon Nanotube. Single walled Nanotube is semiconductor, which exhibits band gap energy of 0.3 eV. Current conduction takes place through the walls. As the diameter increase the band gap energy decreases and it exhibit metallic properties (Fig. 5).

**Figure**.*5: Pictorial view of single walled nanotube*




## 2. Multiwalled carbon nanotube

Multi walled carbon nanotube is a nanotube which has multiple layer boundary. It is assumed that a set of graphite layers is taken and which is folded cylindrical shape to make the multi walled carbon nanotube. Multi walled carbon nanotubes are mostly metallic in nature. The energy band gap is approximately zero .The diameter of multi walled carbon nanotube is larger than that of single walled carbon nanotube. It is mostly used in applications like inter connection between chip components (chip's like microprocessor), because it has a very high conductivity, so the information transfer will be very fast. It is not used for the manufacturing of semiconductor devices like (cnt) carbon nanotube transistor because it will not give a ‘cut off’ on the application of the gate voltage.

**Figure. 6** *Pictorial view of Multiwalled carbon nanotube*

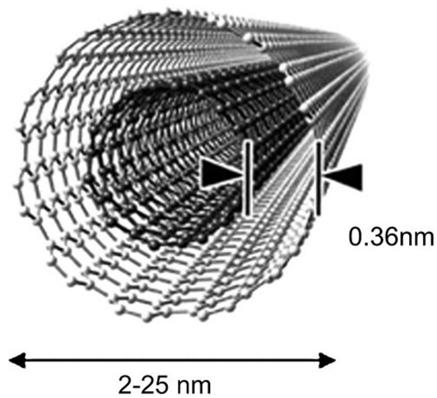
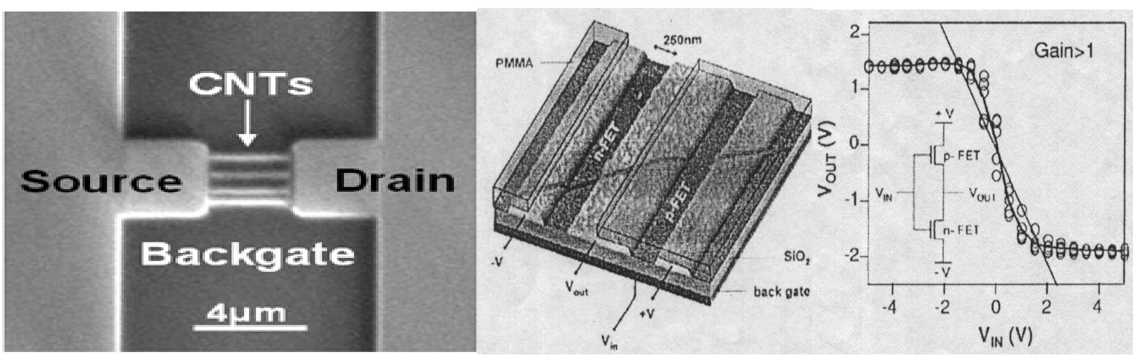



**Fig.ure. 7** *Scanning electron microscope image shows a carbon nanotube field effect transistor with four aligned carbon nanotubes forming the channel.*

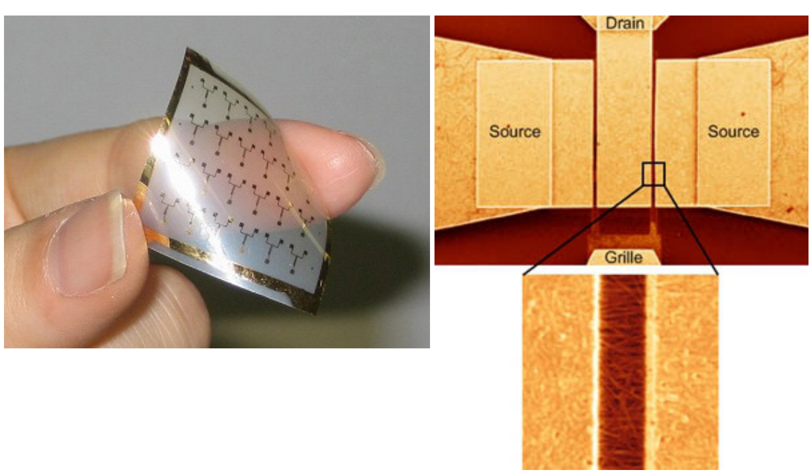



## 2.1 Advantages of carbon nanotube (Cnt)

### 2.1.1 Average diameter Of 1.2 Nm – 1.4 Nm

The Japanese Scientist made the smallest carbon nanotube; the diameter of that carbon nanotube is just 0.4nm.The average diameter of the carbon nanotube is 1.2 nm to 1.4nm.The diameter varies according to the manufacturing process. E-beam lithography can create lines of 50 nm wide (Fig. 7).

**Figure. 8** *Micro viewed transistor*



#### 2.1.2 Highly stable

Carbon nanotubes can with stand high temperatures. It can withstand a temperature up to 2800 degree Celsius in vacuum. Ordinary silicon chip transistors can operate smoothly up to 150 degrees only (Fig. 8).

#### 2.1.3 High current density

Maximum current density is one billion ampere per Centimeter Square. Ordinary copper conductors will burn out at a current density of one million amperes per Centimeter Square.

#### 2.1.4 Good thermal conductivity

The thermal conductivity of the carbon nanotube is 6000 w/m/k so the heat dissipation in the circuitry is quickly passed to the heat sink or other cooling mechanism. On comparison pure diamond will transmit heat at the rate of 3320 w/m/k.

#### 2.1.5 High tensile strength

Carbon nanotube has a tensile strength of 45 billion Pascal. Where as a high strength steel alloy break at about 2 billion Pascal .So NASA is planning to use carbon nanotube for spacecraft component manufacturing.

#### 2.1.6 High density

Carbon nanotube has very high density of 1.33 to 1.40 grams per Cm Square. So NASA is planning to use CNT alloys in the nozzles of future space shuttles.

#### 2.1.7 Twisting Angle Dependence

Carbon nanotube has an important property called TWISTING ANGLE DEPENDENCE. Ordinary multi walled carbon nanotube exhibit metallic nature. But it is dependent on its twisting angle. The band gap of the carbon nanotube increases with its twisting angle .So this method can be used to convert metallic carbon nanotubes in to semi conducting carbon nanotubes. Atomic force microscope is used to make twist in the carbon nanotube .It is operated in contact mode to make these twist.

#### 2.1.8 High Mobility

Mobility of the electrons inside the doped diamond structural carbon is higher than that of in the silicon structure. As the size of the silicon is higher than that of carbon, the chance of collision of electrons, with larger silicon atoms increases as compared to carbon chip.

## 3. Applications Of Carbon Nanotube (Cnt)

1. Inter Connection Inside The Chip.
2. Carbon Nanotube Transistor Manufacturing.
3. Molecular Logic Circuit.

### 3.1 Inter Connection Inside The Chip

At first we are placing catalyst that is to grow microscopic, whisker like carbon nanotube on the surface of the silicon wafer. The catalysts are very carefully placed, so that the direction of carbon nanotube growth can be clearly defined. After that we are doing a chemical vapour deposition on the surface of the wafer. The gas used here is methane. It will trigger the growth of carbon nanotube in the wafer. After the growth of the carbon nanotube we are depositing a layer of silicon over the carbon nanotube growth on the chip to fill the spaces between the carbon nanotube. Finally the surface is finished flat.

### 3.2 Carbon Nanotube Transistor Manufacturing

Transistor less than one quarter the size of the tiniest silicon and potentially more efficient can be made using sheets of carbon just one tenth of a nanotube thick. The transistors are made of grapheme, a sheet of carbon atoms in a flat honeycomb arrangement. Graphene when stacked in layers, and carbon nanotubes when rolled into a tube. Grapheme also conducts electricity faster than most materials since electrons can travel through in straight line between atoms without being scattered. This could ultimately mean faster, more efficient electronics component that also require less power.

Fig.8: Micro viewed Transistor

### 3.3 Molecular Logic Circuit

The IBM team made a “voltage inverter”- one of the three fundamental logic circuits that are the basis for all three fundamental logic circuits that are the basis for all of today’s computers from a carbon nanotube, a tube shaped molecule of carbon atoms that is 100000 times thinner that a human hair. Building a computer circuit “Inverter” out of carbon nanotubes. The IBM scientist used nanotubes to make a “Voltage inverter” circuit also known as NOT gate. They encoded the entire inverter logic function along the length of a single nanotube, forming the world's first intra-molecular or single molecule logic gate.

## 4. Conclusion

Thus diamond chip replaces the need of silicon in every aspect in future generation. Thus we can get fast, small electronic devices.

## 5. References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