Cascaded Multilevel Inverter of 11 Levels for RL Load with Reduced Distortion

A. Santhi Mary Antony*

Department of Electrical and Electronics Engineering, Sathyabama University, Chennai - 600119, India;
msanthimary@gmail.com

Abstract

Cascaded H-bridge multilevel inverter structure allows modularized circuit layout and packaging, but they are prone to high switching losses due to high switching frequency. This problem can be alleviated by reducing the number of semiconductor switches and decreasing the number of switching per cycle. To overcome the foresaid drawbacks, this paper presents an 11 level cascaded H-bridge inverter feeding RL load, with reduced switching losses and less harmonic distortion. The inverter output voltage can be shaped by having unequal voltage sources. With proper switching, number of levels can be increased thus reducing the harmonic distortion, meanwhile the number of switching are also to be optimized. The proposed asymmetrical H-bridge inverter uses lesser number of switches and switching.

Keywords: Cascaded Multilevel Inverter, Harmonic Reduction

1. Introduction

Multilevel converters have become an integral part of high and medium power industrial applications[1-4]. Multilevel inverters have got many advantages as they can develop very high voltages as well as high power without involving transformers and dynamic voltage balancing circuits[5-8]. The attractive features of a multilevel converter can be briefly summarized as staircase waveform quality, common mode voltage elimination, low voltage stress on semiconductor switches and high efficiency. The three major categories of a multilevel inverter as far as topology is concerned are the Neutral Point Clamped (NPC), Cascaded H Bridge (CHB) and Flying Capacitor (FC) multilevel inverters. Out of the three topologies of a multilevel inverter it is found that the CHB topology uses lesser number of semiconductor devices for generating the desired level of voltage when compared to the other two topologies[9-11]. When the number of semiconductor devices decreases the switching losses also decrease in direct proportion and therefore the efficiency of the entire

system increases[10]. For this reason a CHB multilevel inverter can be considered as an effective option for high medium and high voltage applications[11,12]. However use of higher level multilevel inverters may impose other problems such as higher number of switching devices, cost complexity etc[13]. In this paper a topology for 11 level multilevel inverter with reduced number of switching components and reduced number of switching is proposed. The proposed switching configuration gives almost sinusoidal output voltage. Therefore the harmonic content as well as distortion factor are reduced.

2. Cascaded 11-Levels Inverter

The circuit diagram of 11–level inverter is shown in Figure 1. It consists of an H-bridge with switches S10-S13 and 9 switches S1-S9 which are used to control the voltage levels across H-bridge. 5 voltage sources V_{dc1}-V_{dc5} with unequal magnitudes are used as DC sources. This configuration consists of less number of switches compared to all the referred configurations.
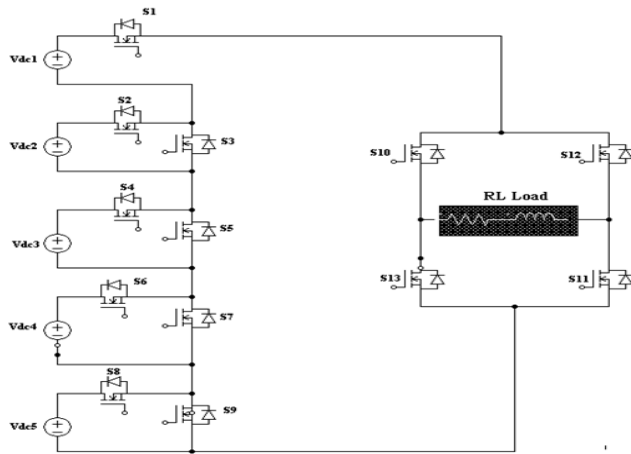
---

* Author for correspondence

Figure 1. Cascaded 11-Levels Inverter for RL Load.

The input voltage magnitudes are given in Table 1.

Table 1. Input Voltages

Voltage Source	Value (V)
V_{dc1}	500
V_{dc2}	400
V_{dc3}	300
V_{dc4}	200
V_{dc5}	100

The switching configuration to obtain 11-level output voltage is given in Table 2.

Table 2. Cascaded 11-Level Inverter-Switching Table

Voltage Level (V)	Switching States								
	S1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	0	0	0	0	0	0	0	0
±500	1	0	1	0	1	0	1	0	1
±900	1	1	0	0	1	0	1	0	1
±1200	1	1	0	1	0	0	1	0	1
±1400	1	1	0	1	0	1	0	0	1
±1500	1	1	0	1	0	1	0	1	0

Switches S10, S11 and S12, S13 conduct for positive and negative half cycles respectively.

3. Simulation Results

The simulation is carried out using PSIM software. The simulation circuit is shown in Figure 2. The switching frequency is taken as 10kHz. The load resistance is 20Ω

and the load inductance is 100μH. The switching pulses are shown in Figure 3. The Inverter output voltage and output currents are shown in Figure 4. The FFT analysis is carried out and the FFT spectra are shown in Figure 5. As observed from switching pulses, the total number of switching per cycle is 28 which are comparatively less. Therefore the switching losses are substantially reduced. The output voltage is almost sinusoidal rather than staircase waveform. Therefore the distortion in output voltage is less and also it is observed from the FFT analysis that results that the lower order harmonics are completely eliminated, therefore the output voltage is sinusoidal.
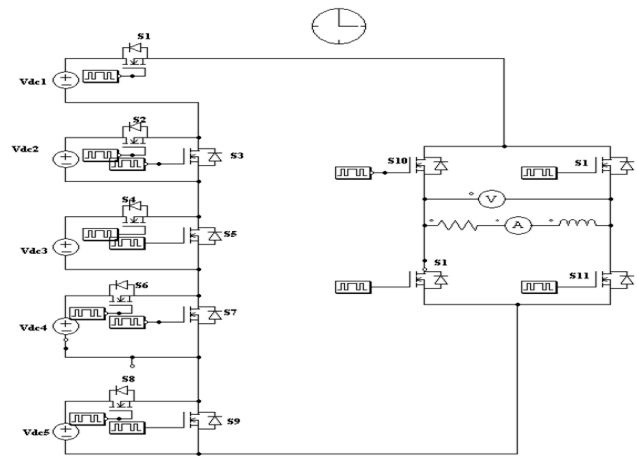

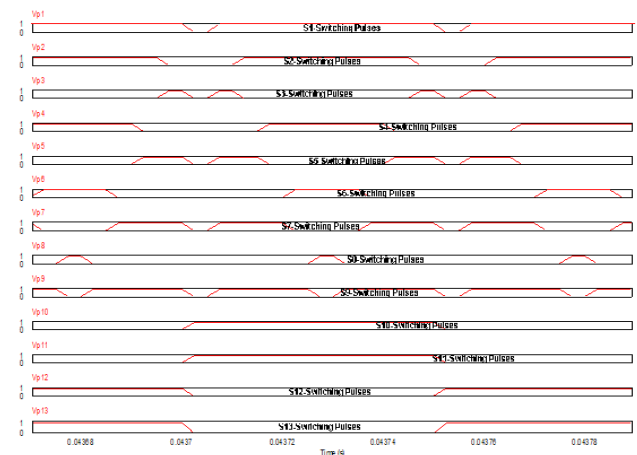**Figure 2.** Simulation Circuit – Cascaded 11- Level Inverter.

Figure 3. Switching Pulses for the Switches S1-S13.

The lowest THD in the references was found to be 5.76% in[11], where as in the proposed configuration the THD is 4.6%.
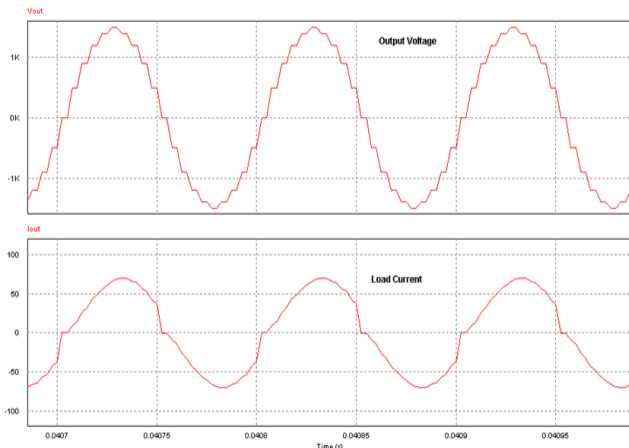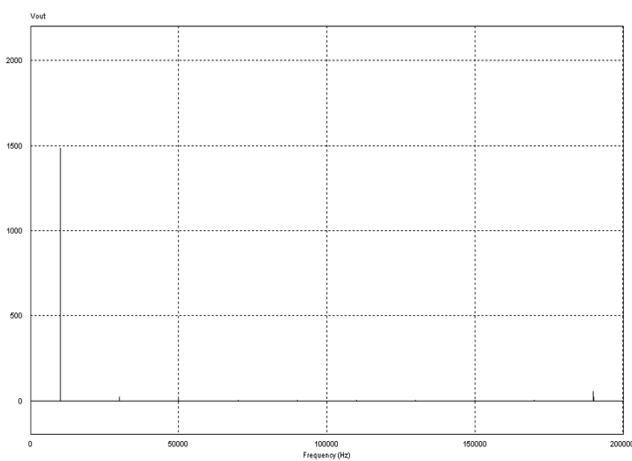
Figure 4. Output Voltage and Current.

Figure 5. FFT Spectra

4. Conclusion

A cascaded MLI of 11 levels with reduced number of switches and switching was proposed, simulated and analyzed. The results show that almost sinusoidal voltage is obtained with less distortion. Further the work can be extended to control the output voltage using pulse modulation techniques during load variations.

5. References

1. Rajeevan PP, Sivakumar K, Gopakumar K, Patel C, Abu-Rub H. A nine level inverter topology for medium voltage induction motor with open-end stator winding. IEEE Trans Ind Electron. 2013 May; 60(9):3627–36.
2. Rashmi MR, Anu B. Cascading of diode clamped multilevel inverter boosters for high voltage applications. International Journal of Applied Mechanics and Materials. 2013; 313–314:876–81.
3. Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM. The age of multilevel converters arrives. IEEE d Electron Mag. 2008 Jun; 2(2):28–39.
4. Rodriguez J, Lai J-S, Peng FZ. Multilevel inverters: A survey of the topologies, controls, and applications. IEEE Trans Ind Electron. 2002 Aug; 49(4):724–38.
5. Sivakumar K, Das A, Ramchand R, Patel C, Gopakumar K. A hybrid multilevel inverter topology for an open-end winding induction-motor drive using two level inverters in series with a capacitor-fed H-bridge cell. IEEE Trans Ind Electron. 2010 Nov; 57(11):3707–14.
6. Lakshmi TVVS, George N, Umashankar S, Kothari DP. Cascaded seven level inverter with reduced number of switches using level shifting PWM technique. ICPEC '13; 2013 Feb. p. 676–80.
7. Ahmed RA, Mekhilef S, Ping HW. New multilevel inverter topology with minimum number of switches. Proceedings of the 14th International Middle East Power Systems Conference (MEPCON '10); Cairo, Egypt; 2010 Dec. p. 1862–7.
8. Seyezhai R. A comparative study of asymmetric and symmetric cascaded multilevel inverter employing variable frequency carrier based PWM. International Journal of Emerging Technology and Advanced Engineering. 2012 Mar; 2(3):230–7.
9. Khajehoddin SA, Bhakshai A, Jain PK. A simple voltage balancing scheme for m-level diode clamped multilevel converter using voltage level modulation. IET Power Electron. 2008; 23(5):2248–59.
10. Malinowski M, Gopakumar K, Rodriguez J, Perez M. A survey on cascaded multilevel inverters. IEEE Trans Ind Electron. 2010; 57(7):2197–206.
11. Nirupama PK, Rashmi MR. Cascaded H Bridge multilevel inverter booster as a dynamic voltage restorer. Journal on Advanced Research in Electrical and Electronics Engineering. 2014; 1(5):93–100.
12. Villanueva E, Correa P, Rodriguez J, Pacas M. Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems. IEEE Trans Ind Electron. 2009 Nov; 56(11):4399–406.
13. Mosazade SY, Fathi SH, Radmanesh H. An overview of high frequency switching patterns of cascaded multilevel inverters suitable for PV applications and proposing a modified method. Indian Journal of Science and Technology. 2014 Sep; 7(9):1342–13.