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Power Consumption Analysis of BCD Adder using XPower Analyzer on VIRTEX FPGA

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Abstract

Adders are the integral part of any digital circuit operation. Optimization of adder's supremacy along with its vicinity is a demanding chore. In this work an efficient BCD ADDER[1] is analyzed in terms of power consumption by scaling the various parameters like voltage, frequency and load capacitance. In addition to this the focus is also given on the airflow of the device to reduce the power. Finally the power is reduced by sending different encoded data at the input. The proposed designs are hardened and implement by means of VHDL and Xilinx ISE (integrated Software Environment) 14.5 and validated using XPower targeting Virtex FPGA. Power consumption is discussed in terms of clock, signals, logic, input/outputs and leakage. A comparative analysis has been shown at the end to validate the obtained results.

Keywords: BCD Adder, Low Power, Saif File, Scaling, VHDL, Xilinx

1. Introduction

In most of the papers the prime focus has been given to increase the speed of the computation of the BCD Adder. The BCD addition process has been modified by different researchers and they proposed unique algorithms like parallel processing and pipelining technique is introduced to reduce power consumption[1]. Decimal speculative addition[2,3], direct decimal addition[4] are cases of such production. The increase in performance also increases power consumption which decreases the life of battery and therefore packaging cost and cost for cooling is increased[6]. Now days energy as well as power consumption are highly alarmed factors for FPGA users and vendors. In this work the goal is to achieve an efficient BCD ADDER in terms of power consumption. This is observed by scaling various parameters like voltage, frequency and load capacitance. In addition to these, focus is also given on the airflow and heat sink of the device to reduce the power. The paper is sectioned into different parts: Section 2 provide the essential depiction on BCD adder. Section 3 is about low power FPGA. Section 4 provides the study of the various parameters regarding the power consumption on Virtex-6. Section 5 focuses on the additional features - heat sink and air flow. Section 6 includes the different Virtex FPGAs. Section 7 discusses encoded data formats using Saif file and 8 the result. Section 9 concludes the paper.

2. Insight to BCD Adder

In BCD addition each sum digit should be adjusted to skip the six unused codes. The addition is carried together with a possible carry from a previous least significant pair of digits (assuming maximum value for input digits) viz., 9 + 9 +1 would result in 19. Figure 1 shows a basic BCD

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adder[1]. The input digits in binary are A3A2A1A0 and B3B2B1B0. S3'S2'S1'S0' are the outputs of the first stage 4 bit adder, to which correction bits 0110(6) is added at the second stage to produce the BCD number S3S2S1S0 shown in equation (2)-(5) along with carry output CN shown in equation (1). The carry CN will be one for digits exceeding 9 or else it will be 0.

$$C_N = C_{OUT} + S_3'S_2' + S_3'S_1' \quad (1)$$

$$S_0 = B_0 \quad (2)$$

$$S_1 = B_3'B_1 + B_3B_2B_1 \quad (3)$$

$$S_2 = B_3'B_2 + B_2B_1 \quad (4)$$

$$S3 = B3B2'B1' \quad (5)$$

3. Low Power FPGA

Power consumption can be divided into two broad categories i.e. power as static and power as dynamic. Mainly static power is developed due to enhancement of leakage current inside the transistors composed of FPGA fabric and on other hand switching of transistors results into dynamic power.

$$P_{(dynamic)} = C.V^2.f \quad (6)$$

$$P_{(total)} = P_{(static)} + P_{(dynamic)} \quad (7)$$

The main concern of an embedded system designer is to have as minimum dynamic power as possible and that would be our main concern here. As given in equation (6), the clock frequency 'f' is directly proportional to dynamic power as compared to supply voltage 'V' which varies quadracticly. There are several models embrace in the journalism to estimate FPGA power-consumption. For modern FPGAs this has been an important factor from design point of view, including Xilinx's Vertex[7] 5 and Altera's Stratix III FPGA[8] architectures. There have been an only some FPGA vendor that are directing their strategies to the low-power itinerant area.

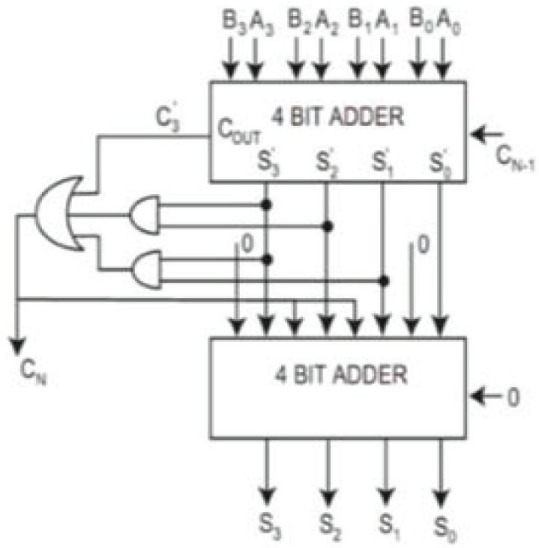

Figure 1. Block Diagram of BCD Adder[1].

4. Scaling Different Parameters

As given in equation (6), the power depends upon three factors i.e. capacitive load, clock frequency and voltage supply.

4.1 Capacitance Scaling

Reducing the capacitance directly affects the power consumption. Following parameters are kept constant for this scaling technique - Time Period = 1ns, with 50% duty cycle Voltage = 1V.

4.2 Frequency Scaling

Frequency scaling can also affect the performance of the adder but this can be dealt with parallelism technique[1]. At very high frequencies (indicated by grey shade in Table 1) the junction temperature exceeds the maximum value of 85 °C. In order to reduce the junction temperature, either improve the cooling aspects of the system (i.e. increase air flow or add a heat sink). Following parameters are kept constant for this scaling technique - Voltage = 1V & Capacitance = 5pF.

4.3 Voltage Scaling

Voltage scaling can sometimes also affect the performance of the adder. For the same throughput in performance pipelining can be introduced[1]. Following parameters are kept constant for this scaling technique- Time Period = 1ns, with 50% duty cycle Capacitance = 5pF.

Table 1 shows that as the capacitance and frequency increase, the power consumption also increases as already stated their linear dependency (6). The increase in voltage increases the power consumption considerably as their dependency is quadratic (6).

Table 1. Scalling different parameters scaling technique - Time Period=1ns, with 50% duty cycle Voltage = 1V

	CAPACITANCE			FREQUENCY			VOLTAGE		
ON-CHIP(W)	5pF	15pF	25pF	100Mhz	10000Mhz	1Ghz	1 V	1.15V	1.20V
CLOCKS	0.006	0.006	0.006	0.006	0.012	0.640	0.006	0.007	0.007
LOGIC	0.000	0.000	0.000	0.000	0.016	0.018	0.000	0.000	0.000
IOs	0.001	0.001	0.001	0.001	0.046	3.699	0.001	0.001	0.001
SIGNALS	0.007	0.010	0.013	0.007	0.035	2.391	0.007	0.007	0.007
LEAKAGE	0327	0.327	0.327	0327	0.329	0.421	0327	0.407	0.439
TOTAL POWER	0.341	0.344	0.347	0.341	0.438	7.169	0.341	0.422	0.455
JUNCTION TEMPERATURE (C)	52.8	52.9	52.9	52.8	53.6	109.5	52.8	53.5	53.8

Table 2. Power Variation regarding airflow & Heat Sink

	AIRFLOW		HEAT SINK			
ON-CHIP (W)	250 LFM	500 LFM	Medium profile	High Profile	Custom TSA(C/W)=3.0	Custom TSA(C/W) =1.0
CLOCKS	0.001	0.001	0.001	0.001	0.001	0.001
LOGIC	0.002	0.002	0.002	0.002	0.002	0.002
IOs	0.002	0.002	0.002	0.002	0.002	0.002
SIGNALS	0.502	0.502	0.502	0.502	0.502	0.502
LEAKAGE	1.304	1.297	1.304	1.300	1.296	1.280
TOTAL POWER	1.812	1.805	1.812	1.808	1.804	1.788
JUNCTION TEMPERATURE (C)	54.9	54.0	54.9	54.4	54.0	51.9

5. Varying Airflow and Heat Sink

For reducing the power and junction temperature the following techniques are individually discussed below. For these observations Voltage is taken as 1V, Time Period is 1ns and Capacitance is 5pF.

5.1 Airflow

Air velocity or Airflow is measured as distance traveled as given per unit time and is generally articulated in LFM (Linear Feet per Minute). When air velocity is multiplied with cross section area of the duct then air volume which is curving past a point is calculated.

5.2 Heat Sink

Heat sink can be defined as type of heat transformer which is passive in nature that cooled down a device by exposing heat into nearby environment. From Table 2 it can be observed that at higher airflow and higher heat sink profile power consumption is reduced.

6. Comparison of Two Different VIRTEX FPGA Families

The latest 7 series FPGA architectures have flexible and augmented architectures to protect IP savings and can be compatible with 6 series of designs. So a comparison of Virtex-7 with Virtex-6 is discussed below. For these observations the capacitance is kept at 5pF, Voltage is 1V, Time Period is 1ns with duty cycle of 50%. Airflow is maintained at 250LFM. Heat sink is medium profile. It can be observed from the Table 3 that though all parameters are kept constant, when the FPGA changes the power consumption gets affected as the Virtex family increases power consumption is reduced and same goes for the junction temperature.

7. Different Encoding Techniques and their Comparison

It is possible to save significant amount of power reducing the number of transactions, i.e. the switching activity,

Table 3. Power variation in Virtex family

ON-CHIP (W)	VIRTEX-7	VIRTEX-6
CLOCKS	0.002	0.001
LOGIC	0.002	0.002
IOs	0.003	0.002
SIGNALS	0.069	0.502
LEAKAGE	0.413	1.304
TOTALPOWER	0.218	1.812
JUNCTION TEMPERATURE(C)	25.3	54.9

at the processor I/O interface. One possible approach for reducing the switching activity is to do suitable encoding of the data before sending it over the I/O interface and a decoder is used to get back the original data at the receiving end. To reduce switching activity it is necessary to increase correlation among the signal values transmitted over the I/O pins. The input is given in different coding ways and the power is calculated using the SAIF file generated which is then after used in XPower Analyzer.

The coding techniques implemented are:

7.1 Binary Coding

It is a phenomenon of expressing a number in base 2, by means of which power of 2 is sentenced to each place. 0 and 1 are representations in binary digits. This coding is used in the previous given techniques.

7.2 Grey Coding

Gray coding produces a code word sequence in which adjacent code words differ only by one-bit, i.e. hamming distance of 1. The number of transitions for binary representation will approach 2 for large values of n. On the other hand, the number of transitions for gray code will always have 1 transition.

7.3 Silent Coding

This coding technique is meant for departure of the transmission energy through protocol of serial wire.

$B^{(t)}$ [n-l: O]: represents n-bit data word by a sender at time instant t.

$B^{(t)}$ [n-l: O]: represents n-bit encoded data word at time instant t.

Below equation represents the encoded data form:

$$B^{(t)}_{[i]} = b^{(t)}_{[i]} \text{ XOR } b^{(t-1)}_{[i]} \qquad \text{for } i = 0 \sim n-1$$

Table 4. Comparison of power for different coded inputs

Coding Techniques	Dynamic Power(w)	Total Power(w)
BINARY	0.023	0.462
GRAY	0.005	0.444
SILENT	0.008	0.450

Serially transmitting these programmed terms ensure reduced figure of switching or transition of the sequential line, and the line appears silent.

8. Results and Discussion

The efficient BCD adder in terms of power consumption after the scaling parameters and other features came out to be with a capacitance of 5pF, time period to be 1ns, voltage is 1V, airflow is 250LFM and heat sink is custom with TSA(C/W) = 1.0 on Virtex-7. The power comes out to be 0.218W with junction temperature 25.3 C.

9. Conclusion

In this document a proficient BCD adder is projected with most favourable parameter values in addition of airflow and heat sink techniques. The silent coding being the input to the adder. Extensive comparison regarding different values for the parameters (capacitance, frequency, voltage) is made. A comparison regarding VIRTEX FPGA is also shown.

10. References

1. Mishra S, Verma G. Low Power and Area Efficient Implementation of BCD Adder on FPGA. International Conference on Signal Processing and Communication (ICSC-2013); 2013 Dec 12-14; JIIT, Noida: IEEE' Xplore; 2013. p. 461–5.
2. Zhao P. Design of Sequential Elements for Low Power Clocking System. IEEE Transactions of (VLSI' Systems). 2009.
3. Vijeyakumar KN, Sumathy V, Babu AD, Elango S, Saravanakumar S. FPGA Implementation of Low Power Hardware Efficient Flagged Binary Coded Decimal Adder. International Journal of Computer Application. 2013 May; 46(14):41–5.
4. Al-Khaleel OD, Tulie NH, Mhaidat K. FPGA Implementation of Binary Coded Decimal Digit Adders

and Multipliers. IEEE of the 8th International Symposium on Mechatronics and its Applications (ISMA); 2012. p. 1–4.
5. Czapski PP, Sluzek A. Power Optimization Techniques in FPGA Devices: A Combination of System- and Low-Levels. World Academy of Science, Engineering and Technology. Waset.Org/Publication/8418. International Journal of Computer Information Science and Engineering. 2007; 1(4).
6. Anderson JH, Najm FN. A novel low-power FPGA routing switch. Proceedings of the IEEE 2004 Custom Integrated Circuits Conference; 2004. p. 719–22.
7. Lamoureux J, Luk W. An Overview of Low-Power Techniques for Field-Programmable Gate. NASA/ESA Conference on Arrays Adaptive Hardware and Systems; 2008 (AHS '08); London: Imperial College; 2008. p. 338–45.
8. Sabri MFM, Othman IN, Husin MH. Development of 5-bit, 4-Inputs PWM Generator on FPGA through VHDL Programming. International Conference on Advance Science and Contemporary Engineering 2012 (ICASCE' 2012); 2012. p. 50.
9. Pandey B, Yadav J, Rajoria N, Pattanaik M. Clock gating based energy efficient ALU design and implementation on FPGA. IEEE International Conference on Energy Efficient Technologies for Sustainability-(ICEETs); 2013 Apr 10-12; Nagercoil, Tamilnadu. 2013. p. 93–7.
10. Chen D, Cong J, Fan Y. Low-power high-level synthesis for FPGA architecture. Proceedings of the 2003 International Symposium on Low Power Electronics and Design (ISLPED' 03); Californian University, USA. 2003. p. 134–9.
11. Chen D, Cong J, Xu J. Optimal module and voltage assignment for low-power. Proceedings of the Asia South Pacific Design Automation Conference; 2005. p. 850–55.
12. Curd D. Xilinx, Power Consumption in 65nm FPGAs. 2007.
13. Xilinx, Optimizing FPGA power with ISE design tools. Xcell Journal. 2007; (60):16–9.
14. Roy K. Power-dissipation driven FPGA place and route under timing constraints. IEEE Transaction on Circuits and Systems. 1999; 46(5):634–7.