

A Modified Algorithm for Voltage Assignment and Floorplanning of SOC Designs

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Abstract

Background/Objectives: Dynamic Power reduction has become a very important issue in the design of System on Chip (SOC). One of the methods for reduction is use of multiple supply voltage (MSV). In this MSV design, the modules are placed in the contiguous region such that modules of same operating voltage are placed in a same region. Such regions are called as Voltage Island. In this process, voltage assignment is followed by floor planning to avoid geometric constraints and physical information of the design. But increase in number of voltage island causes increase in number of level shifters between voltage islands. In this paper, we consider the Intellectual Property (IP) core based Voltage Island driven floorplanning problem including voltage island reduction. Voltage island reduction is carried over by matching algorithm. **Methods/Statistical Analysis:** The proposed matching algorithm constructs a graph G consisting of vertices as Voltages Island and edges as connectivity between Voltage Islands. The proposed matching algorithm takes care of number of modules and interconnects in between Voltage Island while contracting the vertices. **Findings:** The result of proposed matching algorithm is taken as candidate solution represented by Sequence Pair technique, for floorplanning. A new genetic algorithm based optimization is proposed to give the best solution of floorplan which reduces the dynamic power. The proposed algorithms are compared with two approaches such as partitioning the modules on the critical path and partitioning the modules of same operating voltage. Experimental results show that our proposed algorithm for voltage Island reduction and floorplanning minimizes the number of level shifters and overall Dynamic Power of circuit. **Applications/Improvements:** The proposed algorithm plays a significant role in the developing CAD software for the SOC Design. Our future work is on developing a suitable data structure for the floorplanning for multiple voltage design which includes IR drop in power rails as constraint. We also planned to focus this issue of multiple voltage design towards 3D ICs.

Keywords: Floorplanning, System on Chip, VLSI, Voltage Assignment

1. Introduction

Multiple Supply Voltage (MSV) has become one of the popular choice to satisfy low power design, as it allows the designers to assign high voltage for timing critical modules while low voltage for non-critical modules^{1,2}.

Voltage islands based type is one of the efficient methods in MSV where some special regions are provided by special voltages to save power. These special regions are made by partitioning the chip into areas called Voltage islands. These Voltage islands are communicated with each other by level shifters. In Voltage-island based method³⁻⁵, the process involved are island partitioning, voltage assignment and floorplanning. All the above three

steps are to be solved simultaneously under area, power, timing and other physical constraints as they will mutually affect each other.

1.1 Voltage Assignment Problem

In⁶, Voltage islands are formed by perturbations. Perturbations provide change of voltages to voltage islands/island. Further, this process of perturbation merges the one/many voltage islands to another thereby reduce the number of voltage islands⁷. An island level floorplanning or compaction is performed to shrink area of Voltage Island which allows positioning of Compatible Island adjacently. In⁷, voltage assignment and voltage

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island generation is done in placement stage to minimize the number of level shifters. A 0-1 Integer linear programming is used in⁸ for voltage assignment and partitioning is performed based on the different candidate solutions of floorplan. The metrics such as area and cost of interconnects are evaluated to act as constraints.

In practical designs, number of voltages used in a simple chip is smaller than number of supply voltages provided as it creates many CAD related issues such as need for libraries like level shifters⁹, isolation cells, state retention registers etc. Existence of an algorithm or method with generation of smaller number of voltage islands will reduce those CAD related issues.

A proper choice in range of supply voltage will help to lead an optimal solution for reducing Voltage islands. A delay-power curve based model is suggested in^{10,11} which characterize the delay-power of each block. This helps the designers to assign voltage to each block in a simpler fashion. Thereafter blocks operating in same voltages are placed together in a voltage island. A Dynamic algorithm based voltage assignment table for each block is used in¹². Partitioning is done based on a power state model which is build based on states of each blocks such as IDLE, ACTIVE etc.

1.2 Floorplanning Problem

Floorplanning is a crucial step in MSV design as it involves positioning of blocks in proper Voltage islands, positioning of voltage islands adjacently and reducing the area of entire chip by shrinking the silicon occupied area. For this, selection of proper data structure (representation) to blocks plays an important role. The various representations available for classical floorplan are B*tree, Normalized polish expression, Transitive Closure Graph (TCG), Sequence pair etc., in slicing and non-slicing topologies.

In¹³, a slicing floorplan topology is adopted with Normalized polished expression for MSV designs. Simulated annealing is used as optimization process taking wirelength, area and power dissipation as constraints. But it is concluded from classical floorplanner literature that non-slicing topology is better compared with slicing based on complexities in concern to data structure and runtime. Hence, Sequence pair representation is used in^{6,8,12,14,15} for MSV design. This representation is used for non-slicing topology. It gives information about the neighboring blocks such as “above”, “below”, “left of” and

“right of” for a given block. As in classical sequence pair, perturbations are performed by exchange of modules between the sequences or within the sequence. Simulated annealing is used to evaluate the best solution considering wirelength, area, and power as constraint. In¹³ SKB tree which has all advantages of classical B*tree representation is introduced for MSV designs using non-slicing topology. The specialty of SKB tree is the left child of root node is skewed in the tree. Each root node in a level represents various voltage levels. This reduced the run time complexity compared with B*tree. Perturbations are performed by exchanging child nodes in different voltage level nodes. Contouring is used for compaction of blocks as in B*tree. Simulated annealing is used for attaining best solutions considering area, power dissipation and wirelength as constraint. But as like in Sequence pair, SKB tree fails to provide the information about the neighboring blocks.

Our contribution in this paper is,

- A graph matching algorithm based is used for voltage island reduction considering timing and power dissipation.
- Genetic algorithm based optimization is performed for Sequence pair representation given in¹⁴.
- Results are obtained in real time benchmark circuits. On experimenting best delay power value of each block, choice of supply voltage is given to the designer.

Since all the related works are deals with benchmarks where the voltages of each blocks area assumed, we have implemented our work in real time benchmark circuits. Section-2 focuses on the implementation of special voltages to the blocks in the critical path. Section-3 focuses on the implementation of special voltages to the blocks by analysis the best operating characteristics with respect to power dissipation. Section-4 focuses on the proposed method for Voltage assignment. Section-5 we illustrate the method of Genetic algorithm in Sequence pair technique.

2. Method-1 (Partition based on Critical Path Delay)

In this method as in¹⁶, blocks present in the critical path are grouped and enclosed in a partitioned P_1 while remaining blocks are grouped and partitioned as P_2 . After evaluating the best operating voltage of these partitions, partition P_1 is assigned with a minimum voltage while partition P_2 with same operating voltage of the processor.

Advantages

- Improves overall delay.
- Floor planning becomes easier as it has only two partitions.

Disadvantages

- Drastic increase in Power dissipation.
- Inter delay in the partitions gets affected as the blocks.

3. Method-2(Partitions based on Operating Voltages)

In this method, power and delay values of the different modules are analyzed for the predefined set of voltage values. The voltage at which the module gives considerable amount of power reduction is noted. Then the modules with same operating voltages are grouped and partitioning is done. These partitions are called as Power Domains. In this method it is found that the number of power domains is increased compared to the method-1. Then as in¹⁴, the floor planning algorithm is performed. The floor planning algorithm used in this method is Sequence pair algorithm. The sequence pair algorithm cannot be used in the method-1 as it has only two power domains as the number of the modules.

4. Method-3(Proposed Graph Theory Method)

In this method the conventional graph matching algorithm is used. After the power domains formed with the considerable power values and delay values, the power domains are assumed as vertexes and the connectivity between them as the edges.

A graph is constructed based on this information. In addition to this, the vertex weight and edge weight is also calculated. The Vertex weight corresponds to the number of elements present in each power domains and the edge weight corresponds to the number of interconnections between these power domains.

The following matching algorithm is used to merge the number of power domains and thereby the number of power domains is reduced.

Matching Algorithm

Input: Weight Graph G which includes vertex weight and edge weight

Output: Contracted Graph.

- Vertices are ordered in decreasing order of weights.
- Choose the first Vertex in v in the order.
- Run BFS(v).
- Choose the last vertex v at the end of BFS(v).
- Choose the minimum weight edge $e_1 = (u,v)$ incident on u.
- Contract e_1 and Update the corresponding node and edge weights.
Node Weight= (Node weight of u) +(node weight of w)
Edge Weight = (Maximum of edge weights. $e_1, u(p(u)), w(p(u))$).
- Repeat Step 1.

In this algorithm, the numbers of power domains are reduced by performing the vertex matching. As the vertices are weighted. Vertices in the graph are visited in alphabetical order. The Breadth first search (BFS) is used for visiting the vertices in the graph. The matching is performed with following conditions:

- Vertex whose edge weight is maximum of all the edges in the graph.
- On contracting the vertex addition of weight of vertex should be less than overall weight of the vertices of the graph.

Condition 1 is given, to reduce the number of connectivity between the power domains. Condition 2 is given, such that on contracting the vertices the number of modules inside the partitions should not exceed a number of modules inside in all the partitions as it increases the number of modules inside the partitions which in turn increases congestions inside the partitions thereby it increases the intra connectivity delay. The Figure 1 shown describes the way the algorithm is applied for a graph.

5. Floorplanning

The data structure used here is Sequence pair as in^{14,17}. The Sequence pair is created by generating the positive and negative step lines. The following swap of the modules in the sequence pair is applied.

- Swapping the random pair of modules in the first sequence.
- Swapping the random pair of modules in the both sequence.
- Rotating the random module by 90 degree.

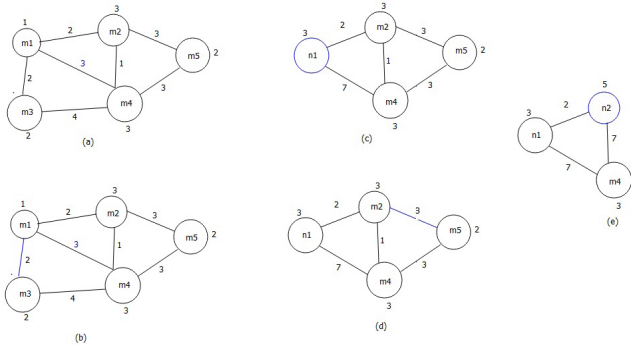


Figure 1. Algorithm implementation in graph given in the figure (a), figure (b) shows the reduction of the nodes m1 and m3 considering the node weight and edge weight, figure (c) shows the graph after contracting the vertices with new node 1, figure (d) shows the identification of the edge between the node m2 and m5 and figure (e) shows the graph with after contraction of vertices with new node 2.

5.1 Genetic Algorithm in Sequence Pair Technique

To avoid the run time complexity of the optimization process due to simulated annealing a modified Genetic algorithm is proposed.

Let SP(S1,S2) is sequence pair. The Sequence S1 is assumed as chromosome 1 and S2 is assumed as Chromosome 2. One point Crossover is applied and the children of the generations are generated as Child 1, Child 2, Child 3 and Child 4. The Child 1 and Child 2 are considered as Sequence pair SP1 and Child 3 and Child 4 are considered as Sequence pair SP2. The Repetition of the genomes in the chromosomes are avoided by inserting the missing chromosomes.

Consider the example given below.

SP (17452638,84725361).

Chromosome 1 (17452638).

Chromosome 2 (84725361).

One point Crossover is applied.

Chromosome 1 (1 7 4 5||2 6 3 8).

Chromosome 2 (8 4 7 2||5 3 6 1).

After Crossover the new chromosomes are;

Chromosome 3 (1 7 4 5 5 3 6 1).

Chromosome 4 (8 4 7 2 2 6 3 8).

In the Chromosome 3 (1 7 4 5 5 3 6 1) there are repetitions in the modules 5 and 1. The missing modules are 2 and 8. These modules are inserted in the Chromosome. Thus after reconstructing the chromosome will be (1 7 4 5

2 3 6 8). Similarly the on reconstructing the chromosome 4 the resultant chromosome will be (8 4 7 2 1 6 3 5). Now the new sequence pair as the result of first Generation is SP2 (1 7 4 5 2 3 6 8,8 4 7 2 1 6 3 5). Based on SP2 neighbors of each modules i.e., above, below, left-of, right-of each modules will be noted and the floor plan is constructed.

The Fitness of this floor plan is evaluated by using the fitness function $f(x) =$ where P(C) denotes the Dynamic power of the entire design. The best floor plan is identified based on the rank ordering. The Generations are stopped if for a floor plan the dynamic power is less than the power of the floor plan of the single supply voltage.

6. Experimental Results

Experiments are performed using GSRC benchmarks. The proposed methods are implemented in the Cadence Digital Encounter System. The Power Domains are created by using the Common Power Format (CPF). This CPF is then called in the Cadence Digital Encounter Environment of calculation of Dynamic Power. All the experiments were run on the Intel i5 CPU 3.20GHz with 4 GB RAM.

The Dynamic power is compared for the three methods with conventional Sequence pair and the proposed Sequence pair floor planning. The Table 1 shows the Dynamic Power consumption of the benchmarks with and without multiple supply voltages. It is observed from the Table 1 that the implementation of multiple supply voltage has the influence in the overall dynamic power reduction in the chip.

But it is observed that the power reduction in considerable amount. The above table is obtained by partitioning of modules in from net list. As mentioned in the Method-2, the performance of the modules is identified and voltages are assigned by grouping the modules. Initially the modules in the partitioning are randomly positioned. But after positioning taking up the Sequence Pair (SP) algorithm as given in the¹⁴ results are tabled in Table 2.

Table 1. Comparison of Overall Dynamic Power with and Without MSV

| Benchmark Circuits | Without MSV(mW) | With MSV(mW) |
|--------------------|-----------------|--------------|
| s298 | 0.26 | 0.03693 |
| s382 | 0.083 | 0.060 |
| s344 | 0.175 | 0.04241 |

Table 2. Comparison of Overall Dynamic Power with and Without Sequence pair

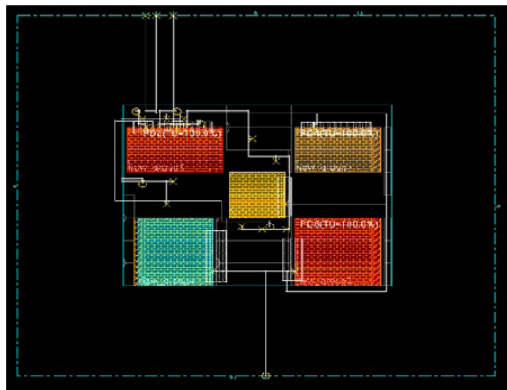
| Benchmark Circuits | Without SP(mW) | With SP(mW) |
|--------------------|----------------|-------------|
| s298 | 0.03693 | 0.0363 |
| s382 | 0.060 | 0.5856 |
| s344 | 0.04241 | 0.04209 |

Table 3. Reduction Dynamic Power in by method 1

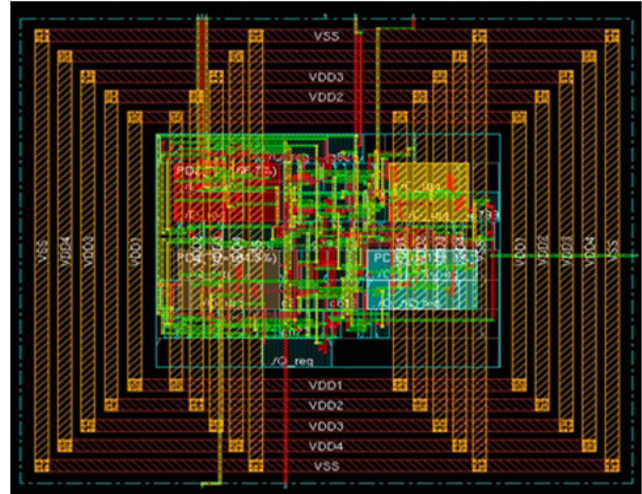
| Benchmark Circuits | Conventional | Method-1 |
|--------------------|--------------|----------|
| s298 | 0.008 | 0.00745 |
| s382 | 0.007 | 0.006 |
| s344 | 0.1715 | 0.1589 |

Table 4. Comparison of Overall Dynamic Power with and Without Modified Genetic Algorithm in Sequence pair

| Benchmark Circuits | Without GA | With GA |
|--------------------|------------|---------|
| s298 | 0.03423 | 0.0205 |
| s382 | 0.05014 | 0.0302 |
| s344 | 0.0396 | 0.0378 |

**Figure 2.** Power domains created before applying the proposed matching algorithm.

The Table 3 shows that the reduction of the Dynamic Power by method-1 i.e., grouping elements in the critical path as partitions. But as mentioned earlier this forces the choice of supply voltage to single voltage by neglecting the performances in the other voltages. The proposed Genetic Algorithm (GA) based sequence pair algorithm is implemented in the new power domains. It is observed that the proposed algorithm shows better results compared to the other methods. The results after implementation in proposed algorithm are tabulated in Table 4.

**Figure 3.** Power domains created after applying the proposed matching algorithm.

7. Conclusion

In this paper, we have proposed a graph theory based matching algorithm. In addition, we have applied genetic algorithm as optimization technique for sequence pair data structure in floor planning. The experimental results have demonstrated that proposed method can get better results than existing methods.

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