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Threshold Voltage Extraction of 220nm FDSOI Device using Linear Extrapolation Method

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Abstract

Objectives: The objective of this research article is to extract threshold voltage of fully depleted silicon on insulator (FDSOI) device@ gate length of 220 nm. **Methods/Analysis:** This paper aims at modeling of fully depleted silicon on insulator (FDSOI) device @ gate length of 220nm. This work finds threshold voltage of FDSOI device using linear extrapolation method. **Findings:** Threshold voltage of the device is found to be 0.21 V. For different gate voltages, drain current versus drain voltage characteristics curves are plotted in this paper. **Novelty /Improvement:** The modeled device is applicable in designing ultra-low power circuits which are useful in portable and wearable devices.

Keywords: Drain Current, Drain Voltage, FDSOI Device, Gate Voltage, Linear Extrapolation, Threshold Voltage

1. Introduction

Silicon-On-Insulator (SOI) is the most capable technology for the future VLSI circuits as these devices provide many advantages over bulk-CMOS devices. Previously researchers proposed novel transistor structures, but they are considered to be non-native and unpractical[1,2].However, the recent success of SOI in fabrication of microprocessor has given this technology credibility and attention it deserves. It is recognized to be viable and mature replacement to mainstream bulk-CMOS for the realization of high performance and ultra-low power digital as well as analog circuits.

SOI structure compared with bulk-CMOS possesses an extra oxide layer generally described as buried oxide (BOX) layer. Usually silicon dioxide is referred as BOX layer. However, the type of insulator used depends on the type of applications. The BOX layer is formed by allowing oxygen to flow on a plain silicon wafer and oxidize the wafer by supplying sufficient amount of heat. Thus, a uniform buried oxide layer is formed.

SOI technology is divided into two groups. Primarily, the active semiconductor layer from the substrate is separated by using a thin insulating layer that comprises parting by implantation of oxygen (SIMOX), Full Isolation by Porous Oxidized Silicon (FIPOS), Wafer Bonding (WB) and Zone Melting Recrystallization (ZMR). Next, semiconductor film is deposited precisely onto an insulating substrate and this is also the case for Silicon On Sapphire (SOS) and Silicon On Zirconia (SOZ).

However, it provides many advantages on contrast with bulk-CMOS[3]. Structural advantages include exclusion of wells and trenches. Device performance has substantially expanded in terms of better radiation tolerance, enhanced dielectric isolation in both perpendicular and parallel directions. The presence of BOX layer lowers the parasitic capacitance and operating voltage is reduced. It is considered to be latch-up free CMOS technology which has the ability to operate in harsh environments.

SOI MOSFETS are of two types: one is called partially depleted SOI MOSFET and the other called as fully depleted SOI MOSFET. SOI MOSFET consists of thinner top silicon layer as well as a channel that is completely depleted of the majority charge carriers. In other words, the depletion width of the SOI MOSFET is larger than SOI layer. Its potential is strongly controlled by the gate

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potential. In these devices there is no neutral region of MOSFET body or floating body. FDSOI possess an extra added advantage of better short channel behavior and elimination of floating body effect[4].On contrary, PDSOI device consists of SOI layer with thickness that is thicker than the maximum depletion width of the gate. PDSOI device is preferred to FDSOI device for applications where maximum clock rates are required and is recognized for its very high performance in terms of speed. However, floating body effect becomes the dominant issue for partially depleted device.

Many parameters are taken into consideration for modelling a MOS device operation. One such important parameters is threshold voltage (V_t)[5].Multiple methods have been proposed and developed to define threshold voltage in the literature. Every method has its pros and cons.

In this research paper, on the basis of extensive research results on process, device and circuit properties, we target to manifest the results of threshold voltage of device with properties by extrapolation process and V-I characteristics of SOI MOSFET.Section2explains structure of the proposed FDSOI device. Section 3 presents results and discusses threshold voltage extraction methods. The paper is concluded in Section 4.

2. Structure of Proposed FDSOI Device

To design any device, the main constraint is that it should possess enhanced performance in one or other way compared to the previous modelled device. One such constraint includes the voltage at which the device start responding to the given input. So that the power consumed by the device for its operation remains within acceptable limit. Another constraint of device design is its dimensions. To keep pace with current market demands in terms of speed, power and area, dimensions of transistors are scaled down every two years.

Considering the above two requirements, a device is modelled with the following specifications. Channel doping concentration of the device is kept low at (1×10^{17} cm^{-3}) to avoid threshold voltage variations and carrier mobility degrading. The doping concentration of source/drain region is maintained at 1×10^{20} cm^{-3}. The thickness of buried oxide layer which plays a vital role in improving the characteristics of FDSOI device is maintained at 100 nm. Gate length is retained at 220 nm. Silicon film layer thickness is maintained at 10 nm. Oxide thickness (t_{OX}) under the gate is selected to be 17 nm. By varying the drain voltage, the drain current characteristics are seen by maintaining constant different gate voltages. Gate voltage is varied from 0.2 V to 0.6 V and drain voltage from 0.1 V to 1.5 V. Substrate is grounded to maintain voltage at 0 V. The thermal voltage is 0.025852 V and gate work function is 4.8 eV. We designed an n-channel SOI device and simulated the device to obtain the resultant threshold voltage (Figure 1).

3. Results and Discussion

The threshold voltage of the MOS transistor is a very important parameter used in all circuit design. The aim of this paper is to calculate threshold voltage of the proposed FDSOI MOSFET using extrapolation method. For an nMOS device at gate-to-source voltages overhead the threshold voltage ($V_{GS} > V_t$) but then still below saturation ($V_{GS} - V_t$) > V_{DS})[6], the transistor is in its linear region, also called as ohmic mode, where it acts like a voltage-controlled variable resistor. The least possible gate-to source voltage differential that is vital to initiate a conducting path between source and drain terminals usually abbreviated as V_t(known as threshold voltage).

Experimentally, the critical point (threshold point) of a device is termed as the critical voltage value in the current-voltage transfer characteristics at which the device is turned on. On other hand, it can be also approximated as the gate to source voltage (V_{GS}) below which the drain current (I_D) is approximately zero. As subthreshold leakage current exits for V_{GS} below V_t, it becomes challenging to precisely find the threshold of the device. Although two distinct conduction regimes (the exponential which is weak inversion region and linear which is strong inversion region) exists in the device, still it is difficult to predict the

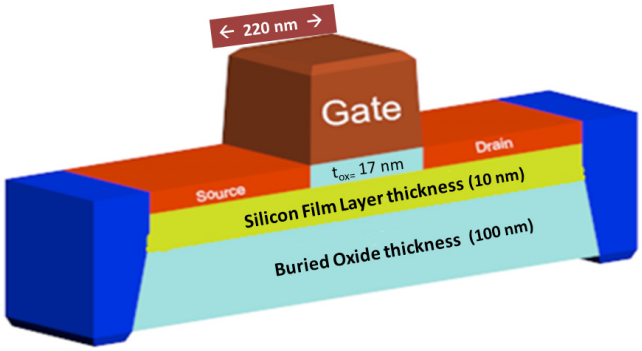

Figure 1. Modeled structure of FDSOI (NMOS) device (drawn not to scale).

critical switching point of the device as the transition is not abrupt.

A number of methods to extract threshold voltage are being used these days, namely Constant Current (CC) technique, Extrapolation in Linear Region (ELR) technique, transconductance linear extrapolation (GMLE) technique, Second Derivative (SD) technique, Ratio Method (RM), transition technique, integral method, corsi function method, Second Derivative Logarithmic (SDL) method, Linear Co-factor Difference Operator (LCDO) method, non-linear optimization[7], quasi-constant-current method etc. In addition to these various extractor circuits have also been designed which calculate threshold voltage automatically[8]. In this paper, a FDSOI MOSFET is modelled and its threshold voltage is measured using linear extrapolation method.

Extrapolation is a process of finding value of a variable beyond its original observation range. The estimate of the observation is provided above or below the given values[9]. In this technique a line is tangentially created at the completion of the assumed data and is prolonged outside that limit. The solutions of linear extrapolation technique are decent when used to extend the graph of an approximately linear function or not too far beyond the known data. To find threshold voltage, firstly, drain current (I_D) is calculated for a range of values of gate voltage (V_G) keeping the drain voltage (V_D) constant at smaller values to ensure the operation in the linear region. An I_D versus V_G graph is plotted. Due to the subthreshold conductance at low V_G values and the drop in effective mobility athigh electric fields, the actual curve is not a straight line[10].

Transconductance (g_m) is given by the ratio of drain current to gate voltage. Its maximum value i.e., the maximum slope of the curve is found at which a tangent is drawn to the curve. On extrapolating the tangent the intercept on x-axis (X) is found. By subtracting half the drain voltage value from the intercept gives threshold voltage (V_t).

$$V_t = X - (V_D/2)$$

The peak-g_m condition is not fundamental but chosen simply to obtain a unique intercept given a gradual cutoff-to-linear subthreshold transition while minimizing series resistance effects[11]. Since this method uses above-threshold data it could be more sensitive to mobility and series resistance variability and lacks accuracy[12]. However, the method is simple.

To find out the value of threshold voltage a plot is drawn between gate voltages on X-axis with drain current on Y-axis. For the given values of gate voltages and drain currents as reported in Table 1, I_D–V_{GS} transconductance characteristics curve is plotted in Figure 2.

Thus for calculating the value of threshold voltage from Figure 2, by considering maximum slope that meets X-axis and the value of V_{DS} as 0.1 V, we get the value as 0.21 V. Figure 3 shows output characteristics of the proposed FDSOI device. For different constant gate voltages, the behavior of drain current for a considered drain voltage is shown.

Table 1. Drain current versus gate voltage of the proposed FDSOI device

GateVoltage	Drain Current
–0.125	7.86996e–11
–0.05	8.30437e–10
0.1	9.24215e–08
0.2	1.54898e–06
0.3	1.09951e–05
0.4	2.95256e–05
0.5	4.92316e–05
0.6	6.73285e–05
0.7	8.36621e–05
0.8	9.8478e–05
0.9	0.000112023
1	0.000124496
1.1	0.000136055
1.2	0.000146823
1.3	0.000156899
1.4	0.000166366
1.5	0.000175289

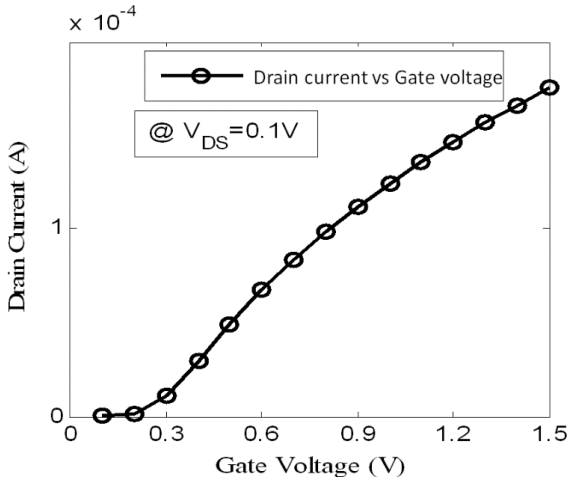

Figure 2. Transconductance characteristic of the proposed FDSOI device.

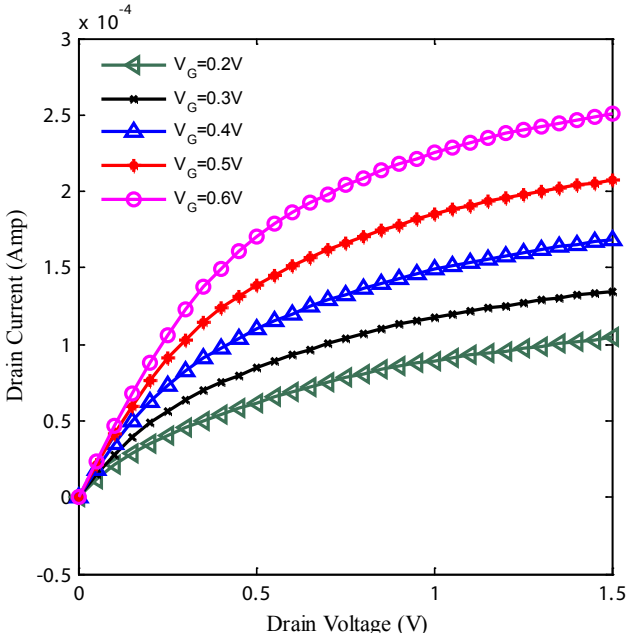

Figure3. Plot of drain current versus drain voltage at different constant gate voltages.

4. Conclusion

This paper models an FDSOI device, which has220 nm channel length. Critical device parameters such as buried oxide layer (BOX), gate oxide thickness (t_{OX}), channel doping concentration (NCH) are precisely adjusted to achieve optimum device threshold voltage (V_t) for low power applications. Deciding appropriate threshold voltage is one of the significant design aspects of the device in realizing ultra-low power consumption. This research work simulated the modeled FDSOI device for obtaining its output characteristics. This modeled n-channel FDSOI device exhibits superior electrical characteristics for ultra low power operations. These characteristics make it ideal for ultra-low applications. Thismodeled n-channel FDSOI device can also be used in internet of thing (IoT)technology, where ultra low power consumption is an absolute necessity.

5. References

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