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Low Power and High Variation Tolerant 9T-SRAM Cell at 16-nm Technology Node

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Abstract

Objectives: The objective of this paper is to design a threshold voltage (V_t) variation tolerant low leakage low power SRAM cell. **Methods/Analysis:** The proposed cell has the same architecture as that of read decoupled 7T SRAM cell (RD7T) with an exception of TG instead of access NMOS transistors. This cell is operated in super-threshold region at power supply varying from 0.62V to 0.77V. **Findings:** Various design metrics of the proposed cell are estimated and compared with RD7T. The proposed cell offers robustness against the process induced variations by providing a 1.1 × narrower spread in read time (T_{RA}) distribution at a cost of 1.23 × penalty in T_{RA}. It also provides 2.06 × narrower spread in read current (I_{READ}) distribution at the price of 1.13 × penalty in I_{READ}. It offers 1.42 × lower leakage current and also a 1.06 × lower hold power as compared to that of RD7T. Moreover, it also provides 1.13 × narrower spread in hold power with same read static noise margin (185 mV). **Novelty /Improvement:** The Monte Carlo based comparative analysis proves that the suggested cell is tolerant to the V_t fluctuations to a great extent.

Keywords: Leakage Current, Leakage Power Dissipation, Read Current, Read Delay, RSNM, Transmission Gate, WSNM

1. Introduction

SRAM is a bistable circuitry, which is used as data storage elements with microprocessors. With the evolution of technology, the operating speed of microprocessors has increased considerably. However, there is no appreciable improvement in the speed of memory. Therefore, cache memories are introduced to synchronize the speed of the processor and memory. The main applications of SRAM include RAM or cache memories in microprocessors, application specific ICs, in FPGAs and CPLDs etc. Some other prominent applications include implanted medical instruments, wireless body sensing network etc. SRAM significantly influences the performance and power efficiency of device, as it occupies 90% of the system-on-chip (SoC) area[1]. Down scaling of the memory cells is, thus, an important factor to achieve significant improvement in the density of integration. However, the leakage current proportionally increases as the number of transistors increases. Therefore, the standby leakage current of an SRAM cell needs to be reduced to achieve a higher density of integration. Additionally, such rapid scaling gives rise to variation in important parameters of MOSFETs (such as threshold voltage) utilized in an SRAM cell due to RDF. These variations cause fluctuations in the performance of an SRAM cell[2]. These include unfavorable effects on the write-ability, read stability and reliability of the cell. Further, the SRAM cell stability is also adversely affected. These variations make conventional 6-Transistor SRAM cell (CON6T) unpredictable and less reliable.

Therefore, cell design techniques to improve read stability, write-ability, power reduction, variation tolerance need to be investigated. In[3], an SRAM cell is proposed which achieves 50% reduction in access delay and 10% reduction in power consumption. However, these improvements are achieved at the cost of poor noise margin. A 7T SRAM cell is proposed in[4], which presents an improved performance at low supply voltage (V_{DD}). However, the WSNM and RSNM of the cell are reduced. Another, 7T SRAM cell[5], achieved an improvement in the read noise margin by disconnecting the pull down path to lowest available voltage (i.e. ground) during read

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transition. However, it endures a low write-ability due to single ended write operation. Many other cells are proposed to improve the read stability[6–9]. But these cells require larger area and/or require extra peripherals to support their operation.

For achieving better performance, reliability and tolerance to process induced variations, an optimal trade-off in respect to cell area must be made. This article suggests a read decoupled 9T SRAM cell, which utilizes transmission gate (TG) (TG9T), which performs single ended read operation. This circuit is compared with the similar circuits proposed in[10] and[11]. This cell eliminates the problem of read upset (as seen in CON6T), as read decoupled technique is used. Additionally, it also offers improvement in terms of leakage current and thus, higher integration density is achieved. It also offers an improvement in variability of various design parameters of an SRAM cell as compared to its conventional counterpart[10,11].

The remaining portion of the article is arranged as following. Section 2 presents the proposed work and device sizing. Section 3 replicates the characterization of SRAM cells and comparisons and finally, the conclusion in Section 4.

2. Proposed Work and Device Sizing

The main goal behind rapid scaling of device size is to achieve better performance as well as increased integration density. However, aggressive scaling makes the device more prone to PVT variations. It is observed that V_t fluctuations due to RDF is inversely proportional to square root of area of the device[12]. Therefore, by increasing the area, the variability problem can be compensated. In this work, an effort is made to alleviate the problems in traditional SRAM cell design like reliability, read stability and leakage current. This article offers a read decoupled TG9T cell (Figure 1) and a comparison with the read decoupled 7T SRAM cell (RD7T)[10,11] (Figure 2) is presented in terms of important design metrics of SRAM cell like RSNM, variability etc. A TG9T-based SRAM consisting of 16 SRAM cells in a row and 256 SRAM cells in a column is simulated. TG9T utilizes separate read and write port. The proposed circuit has a similar architecture as that of RD7T, except addition of two pMOSFETs (MP3/4) in parallel with the access nMOSFETs (MN3/4), forming a TG. The length for all the transistors is selected as 16 nm. Since, by increasing the area V_t fluctuations

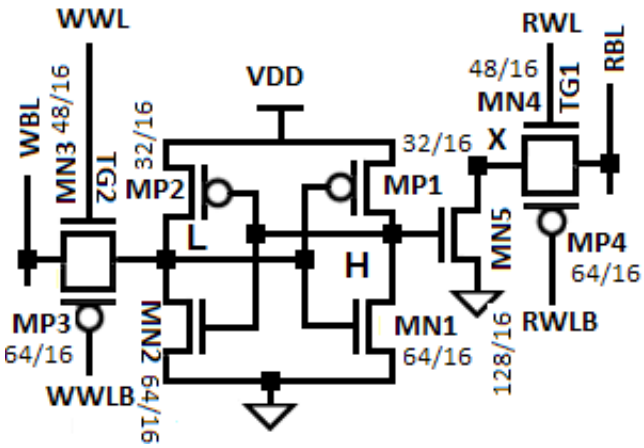

Figure 1. Proposed read decoupled TG based 9T SRAM cell (TG9T).

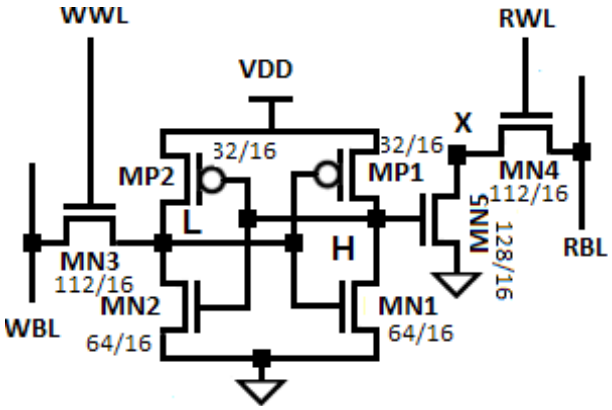

Figure 2. Read decoupled 7T SRAM cell (RD7T).

can be reduced, therefore, the widths of the transistors MN1/2, MN3/4, MN5 are kept at 64 nm, 112 nm and 128 nm respectively (see Figure 2). As the circuit, RD7T, is read decoupled, it is not influenced by the cell ratio or βratio (ratio of driver transistor size to the access transistor size, i.e., $\beta_{driver}/\beta_{access}$). Further, to maintain the write ability, γ_{ratio} (= $\beta_{pull\ up}/\ \beta_{access}$) should be ≤ 1.8[13]. γ_{ratio} for the RD7T is maintained at 0.28 (width of MP2/width of MN3=32/112) for successful write operation. As TG9T has the same architecture and the aggregate width of the TG (see Figure 1) is kept same as that of access transistor in RD7T, therefore, equal γ_{ratio} is maintained.

3. Characterization of SRAM Cells

The aim of this article is to address the problems associated an SRAM cell, designed in nanometer technology (below 65- nm technology), where the device is more prone to PVT variations. The variability (which is

defined as the ratio of the standard deviation (σ) to mean (μ) of a particular design parameter) problem arises more crucial as the miniaturization increases. Therefore, it is essential to investigate it further and take corrective measures.

The parameters like effective length (L), channel-doping concentration (NDEP), oxide thickness (t_{ox}), threshold voltage (V_{tn}, V_{tp}) are assumed to have Gaussian distributions with 3σ variation of 10%[1]. For achieving better precision in result the design metrics are estimated with 5000 Monte Carlo run[14].

3.1 Read Current (I_{READ}) Estimation and its Variability Analysis

I_{READ} is the total current flows through MN4 and MP4 of the TG1. Due to the presence of TG, there is a substantial improvement in the variability of I_{READ}. This is justified because V_t for MN4 decreases due to RDF. However, V_t of MP4 remains unaltered. This results in an increase in the current flowing through MN4, increasing the I_{READ} flowing through TG. Thus, VX increases and VRBL discharges swiftly. This increase in VX and decrease in VRBL causes the threshold voltages of both MN4 and MP4 to increase respectively due to body effect. Because of that, I_{READ} decreases. Therefore, this stabilizes the I_{READ} flowing through TG1. Similarly, the total I_{READ} is stabilized when the V_t of MN4 increases due to RDF.

A similar explanation can be presented when the V_t of MP4 varies with RDF. Hence, it can be concluded that the I_{READ} is more stable when TG is present unlike when only nMOSFET access transistor is used. Therefore, TG-based SRAM cell has lower value of variability due to the presence of TG when compared with RD7T. A 2.06× improvement in variability of I_{READ} with respect to RD7T is observed @ V_{DD} = 0.77 V. This improvement in variability of I_{READ} also ensures a tighter spread in other design metrics such as read delay.

Improvement in I_{READ} variability is obtained at a cost of 1.13 × penalty in I_{READ} (Figure 3). This happens because drive current of an nMOS is larger than that of pMOS. Therefore, even if the aggregate width of MN4 and MP4 (48 nm and 64 nm respectively) is 112 nm, i.e., width of access transistor of RD7T, MN4 (see Figure 2), their total drive currents are not equal. Nevertheless, because of the averaging effect of transmission gate, an improved variability of I_{READ} is observed (Figures 4 and 5).

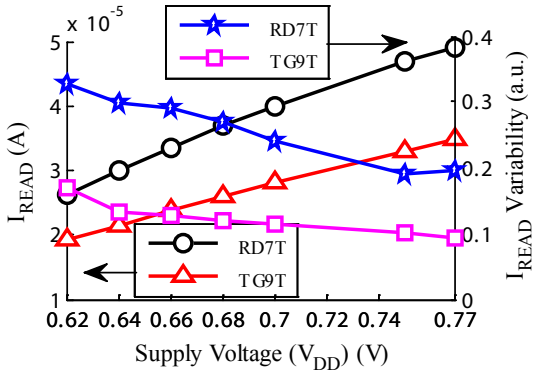

Figure 3. Read current versus supply voltage, V_{DD}.

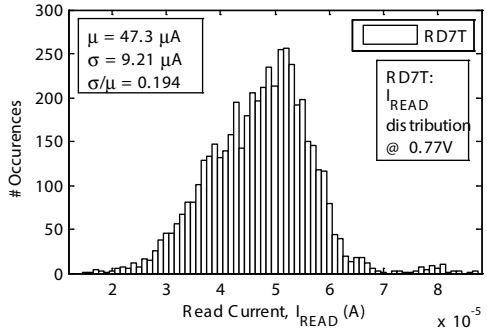

Figure 4. Read current distribution for RD7T @ V_{DD} = 0.77 V.

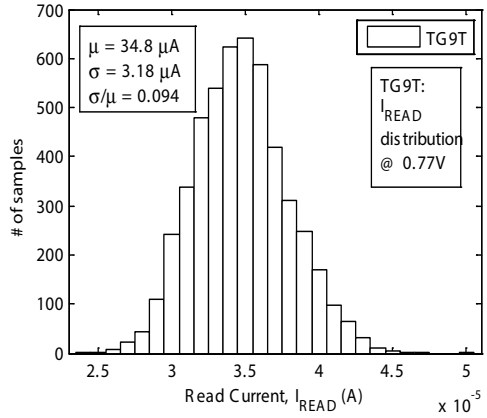

Figure 5. Read current distribution for TG9T.

3.2 Read Access Time Estimation and its Variability Analysis

Read operation is initiated by pulling up RWL to V_{DD} and as RWLB is complimentary to RWL, it is grounded. Therefore, both the transistors of the TG1 conduct. During read operation, WWL is grounded and its complimentary WWLB becomes high. Therefore, both the transistors of the TG2 are disabled. RBL is precharged before reading. Therefore, during read mode RBL discharges through

TG1 and MN5 if H node holds '1'. Read access time (T_{RA}) is estimated from the position when RWL increases from the beginning low value to the position when RBL is discharged to 50% of its initial high value[15]. The estimated value is reported in Table 1.

The read delay and its variability are plotted with respect to V_{DD} in Figure 6. As observed from figure, TG9T provides 1.1 × shorter distribution in T_{RA} as compared to RD7T at an expense of 1.23 × longer T_{RA} (Figures 7 and 8). This penalty occurs because, RBL discharges through nMOSFET in RD7T whereas RBL discharges through a combination of nMOSFET and pMOSFET in TG9T. The carrier of pMOSFET (hole) has almost two times lower mobility than that of nMOSFET (electron). This results in smaller read current/ longer read delay in TG9T. However, an improvement in variability is reached due to use of TG rather than pass transistors in read buffer.

Table 1. Read access time and its spread @ 0.77 V

SRAM	Std. Dev. (ps)	Mean (ps)	Std.Dev./Mean
TG9T	14.4	163	0.089
RD7T	11.4	121	0.097

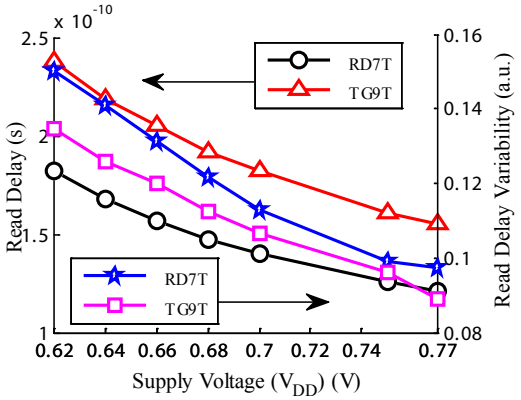

Figure 6. Read access time versus V_{DD}.

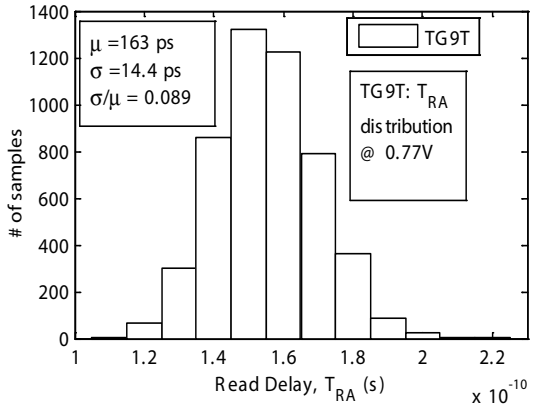

Figure 7. Read delay distribution for TG9T @ V_{DD} = 0.77 V.

3.3 Write Access Time Estimation

Write mechanism is initiated by pulling up WWL to V_{DD} and as WWLB is compliment of WWL, it is grounded. Therefore, both the transistors of the TG2 conduct. During write operation, RWL is grounded and RWLB, which is complimentary to RWL, becomes high. Therefore, both the transistors of the TG1 are disabled. The desired data to be written is transferred at write bit line (WBL). An opposite data is written in node H automatically (due to cross coupling inverters). Write access time (T_{WA}) to write '0' at node L is estimated from the position when WWL increases from its beginning low value to the position when L falls to 10% of its beginning high value. Due to presence of nMOSFET, which provides lower resistance path for the discharging current in RD7T, T_{WA} has a shorter value as compared to TG9T, which uses TG (Figure 5). Therefore, a 1.14 × penalty (@V_{DD} = 0.77 V) is observed as compared to RD7T (Figure 9).

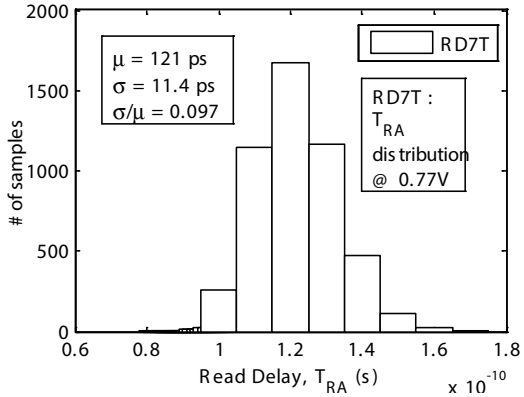

Figure 8. Read delay distribution for RD7T @ V_{DD} = 0.77 V.

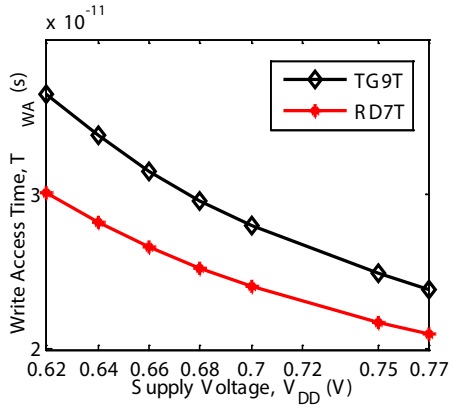

Figure 9. Write access time versus V_{DD}.

3.4 Read Stability

SRAM is mostly susceptible to noise when it is operating in read mode. According to Seevinck's seminal work, read stability is quantified in terms of RSNM, and is defined as[16]. Its estimation is carried out by operating SRAM cell in the read mode. The RSNM is obtained graphically with the help of Voltage Transfer Curves (VTCs) which forms a butterfly curve. The butterfly curve for both the cells is shown in Figure 10. RSNM value is obtained as given in[17,18] and as shown in the figure. It is observed that RSNM of RD7T and TG9T are identical and are same as the hold static noise margin (HSNM) of conventional 6T cell because they are both read decoupled.

3.5 Write - ability

Write-ability can be measured in terms of WSNM. WSNM is defined as given in[17]. Graphically it can be measured as given in[18–28] and shown in Figure 11. It can be observed from the figure, WSNM of RD7T and TG9T are 295 mV and 245 mV respectively @ V_{DD} = 0.77 V. This degradation in WSNM (1.2 ×) of TG9T is due to the use of TG which has a lower drive current as compared to that of nMOSFET used in RD7T.

As it is observed from the graphs (see Figures 10 and 11), the RSNM (185 mV) value is less than the WSNM (245 mV) value, therefore the proposed cell is a RSNM limited cell[12].

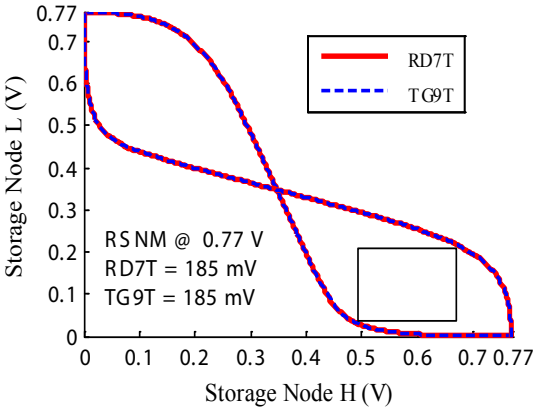

Figure 10. Read Static Noise Margin of TG9T and RD7T @ V_{DD} = 0.77 V.

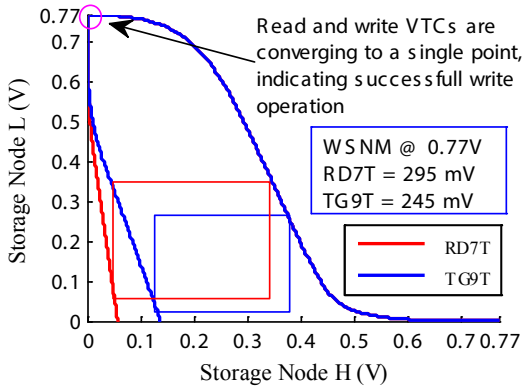

Figure 11. Write static noise margin of TG9T and RD7T @ V_{DD} =0.77 V.

3.6 Leakage Current (I_{LEAK}) Measurement

Suggested SRAM cell shows a lower I_{LEAK}, compared to RD7T. The leakage current depends upon the width of the device. Due to the presence of pMOSFETs in TG the cell offers a lower leakage. The reason for such behavior is the hot carrier injection in short channel devices. The hot carrier injection takes place when the holes or electrons cross the potential barrier at the Si/SiO2 interface and enter the oxide layer due to the presence of high electric field near the Si/SiO2 layer, providing holes or electrons the required amount of energy to do so.

The probability of electron injection is more than that of hole because electron has a lower effective mass than that of a hole. Thus, presence of more pMOSFETs reduces the leakage current in case of TG9T. It can be observed from the Figure 12 that it achieves a 1.42 × improvement in the I_{LEAK} @ V_{DD} = 0.77 V.

The I_{READ} to I_{LEAK} ratio is directly related to sense margin and column height of SRAM. Therefore, to achieve a higher sense margin and column height I_{READ} to I_{LEAK} ratio should be higher. A higher value of I_{READ}/I_{LEAK} is shown by the proposed cell, TG9T, compared to that of

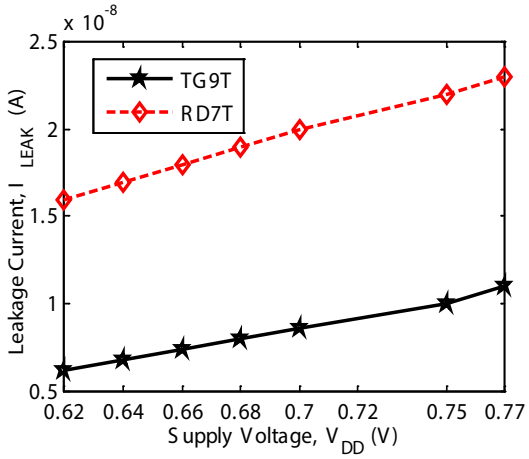

Figure 12. Leakage Current, I_{LEAK} versus V_{DD}.

RD7T (see Figure 13). Therefore, more cells can be allied to a column, resulting in a higher integration density.

3.7 Leakage Power Dissipation

The standby power of an SRAM cell is an important factor as most of the cells remains in the standby mode other than the row being accessed[29]. It is estimated when the cell is in the hold mode[30]. As observed form the plot, shown in Figure 14, TG9T consumes 1.06× lower power during hold mode as compared to RD7T at V_{DD} = 0.77 V. This happens because of low I_{LEAK} due to the presence of TG (both the cells operate at the same V_{DD} and power is proportional to current, i.e., I_{LEAK}) Therefore, in the standby mode TG9T consumes lower power (Figure 14). The distribution of hold power for both the cells is plotted in Figure 15. It can also be observed that the TG9T shows 1.13 × narrower spread in hold power at V_{DD} = 0.77 V compared to RD7T.

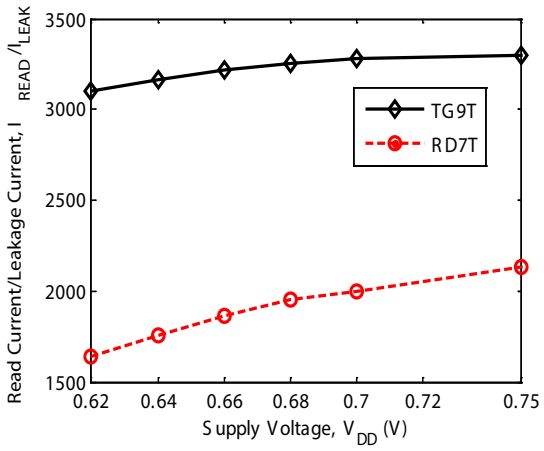

Figure 13. I_{READ}/I_{LEAK} versus V_{DD}.

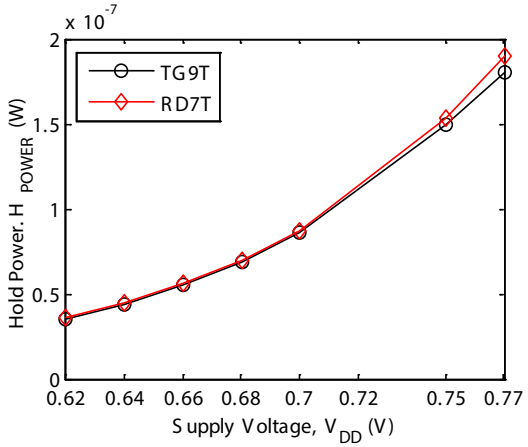

Figure 14. Hold power versus V_{DD}.

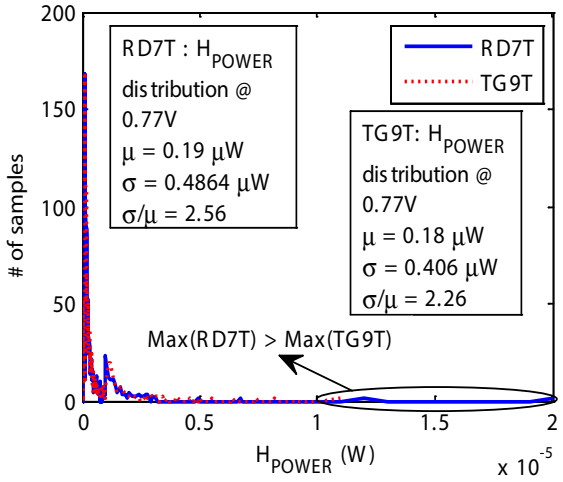

Figure 15. Hold power distribution for RD7T and TG9T @ V_{DD} = 0.77V.

4. Conclusion

With the aggressive scaling of device dimension for achieving higher integration and speed, the problem of variability and leakage current has become more severe. This article suggests a TG-based threshold voltage variation tolerant low leakage low power 9T SRAM. A study of influence of process induced variations on I_{READ}, T_{RA} and standby power is conducted. Substantial improvement in mostly all design parameters are observed as compared to those of read decoupled 7T SRAM cell. A significant improvement in the leakage current was also observed in the proposed cell. Its tolerance in variation and improvement in leakage current can be attributed to the use of access TGs. Hence, the proposed cell is a viable choice where improved stability and low power dissipation are major concern.

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