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A Novel Cubic Generator Realised by CCIII-based Four Quadrant Analog Multiplier and Divider

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Abstract

The objective of this paper is to present a novel cubic generator circuit using four quadrant analog multiplier and divider based on third generation current conveyor. A well-established approach has been utilized to implement the new four-quadrant analog multiplier and divider using CCIII exhibiting a larger usable bandwidth. Some additional, relevant, non-linear applications of CCIII-based four-quadrant analog multiplier and divider have also been worked out to demonstrate its usefulness. PSPICE simulations have been carried out to validate the theoretical findings of the proposed novel cubic generator and other presented circuit configurations. Applications of the new CCIII-based multiplier and divider circuits of this paper have been shown to realize amplitude modulation, squarer and finally the novel cubic generator.

Keywords: Non-Linear circuits, Analog Multiplier, Analog Divider, Third generation current conveyor, Cubic generator

1. Introduction

A large number of established research sub-domains of analog signal generation and processing are; continuous-time filters, analog to digital convertors, digital to analog convertors, continuous-time precision rectifiers, inductor realizations, sinusoidal oscillators etc. Further, to realize the desired functionality[1-3] depending upon the specific needs of linear and non-linear application situations, variety of semiconductor devices and integrated circuit Active Building Blocks (ABB) have been employed.

After overwhelming rule of over four decades by operational amplifiers in the design and innovations of linear and non-linear, voltage-mode circuits the current-mode circuits also have taken over. Largely this shift towards current-mode is, arguably, due to the advantages such as; low power consumption, larger dynamic range, greater bandwidth etc[4]. A literature survey reveals that the most popular active building block of this current-mode signal processing has been the Current Conveyor (CC). Till now three generations of CCs and their variants have been available in the literature. For a detailed account on the wide variety of linear and non-linear applications using devices from these current conveyor family readers may refer, for instance[5,6].

Third generation current conveyor (CCIII) is one of ABBs that has not been explored much for continuous-time signal processing. Although CCIII was introduced long back in 1995 by Fabre[7], yet very few applications employing CCIII on filters, oscillators, inductor simulation etc[8-12], have seen day of publication since then.

Four quadrant analog multiplier [FQAM] and divider has historically played a very important role in the area of continuous time signal processing[13,14]. Consequently, a large variety of such circuits were developed employing various ABBs[15-33] such as;operational amplifier[15-17], operational transconductance amplifier[18], current conveyor and its variant[19-23], differential difference amplifer[24], current feedback operational amplifier[25], current differencing buffered amplifier[26-27], current controlled current differencing buffered amplifier[28-29], current differencing transconducatance amplifier[30-31], current controllable current conveyor transconductance amplifier[32], operational trans-resistance amplifier[33] etc.

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This literature survey indicates that no published work of any non-linear application using CCIII can be found in the open literature.

This paper, therefore, attempts to present a novel cubic generator circuit as a non-linear application of third generation current conveyor (CCIII) using a four quadrant analog multiplier and divider. To accomplish this we have considered to use an all CCIII-based analog multiplier and divider in the cubic circuit configuration. The analog multiplier and divider, which works well in all four quadrants, can work without altering the hardware configuration. In order to ensure the effectiveness of this CCIII-based analog multiplier and divider, we have tested it for squarer and amplitude modulator before using them in the new cubic circuit of this paper.

The next section provides the introduction of the used active device i.e CCIII and section 3elaborates the circuit diagram of the new proposed cubic circuit generator along with a detailed approach to design the analog multiplier and dividerand its relevant mathematical development. Section 4 presents the simulation results of all the relevant configuartions and the proposed new cubic circuit. At the end concluding remarks have been given in Section 5.

2. Introduction to CCIII

The current conveyor is an active device which can convey the current form one port to another. The third generation current conveyor's port relationship is represented by (1) and its symbollic notation is given in Figure 1.

$$\begin{bmatrix} I_y \\ V_x \\ I_{z\pm} \end{bmatrix} = \begin{bmatrix} 0 & -\alpha & 0 \\ \beta & 0 & 0 \\ 0 & \pm\gamma & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z\pm} \end{bmatrix} \quad (1)$$

where α, β and γ represent non-ideal port transfer ratios of X, Y and Z terminals respectively and ideally α = β = γ = 1. From (1) we can observe that terminal X and Y are vitually shorted and the current entering through port X will be conveyed to the port Y as well as port Z.

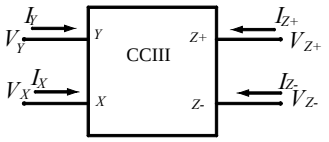


Figure 1. Symbolic Notation of CCIII.

3. Cubic Generator Circuit

Our innovative approach to the realization of a cubic circuit using the four quadrant analog multiplier and divider (FQAMD) is shown in Figure 2 which is a complete CCIII-based cubic circuit generator. The detailed description comprising of mathematical development of the FQAMD block has been given in next subsection.

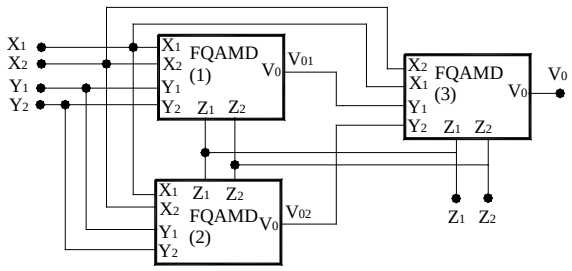


Figure 2. Cubic circuit realization using four quadrant analog multiplier/divider.

The outputs of the three FQAMD blocks are V_{01}, V_{02} and V_0 respectively given in (2)-(4) and the final output of the cubic circuit is represented by (5)-(6).

$$V_{01} = \frac{(W_A/L_A)\,(X_1 - X_2)(Y_1 - Y_2)}{(W_B/L_B)(Z_1 - Z_2)} \quad (2)$$

$$V_{02} = \frac{(W_A/L_A)\,(X_1 - X_2)(Y_2 - Y_1)}{(W_B/L_B)(Z_1 - Z_2)} \quad (3)$$

$$V_0 = \frac{(W_A/L_A)\,(X_1 - X_2)^2(Y_1 - Y_2)}{(W_B/L_B)(Z_1 - Z_2)} \quad (4)$$

If $X_1 = Y_1$ and $X_2 = Y_2$ then

$$V_0 = \frac{(W_A/L_A)\,(X_1 - X_2)^3}{(W_B/L_B)(Z_1 - Z_2)^2} \quad (5)$$

If the aspect ratios of the MOSFETs employed in FQAMD are kept same, the circuit acts as cubic circuit and the output is given as.

$$V_0 = \frac{(X_1 - X_2)^3}{(Z_1 - Z_2)^2} \quad (6)$$

3.1 Four Quadrant Analog Multiplier and Divider employing CCIII

The complete circuit diagram of FQAMD block used in the proposed cubic circuit of Figure 2, which is

simultaneously a multiplier and a divider is shown in Figure 3.

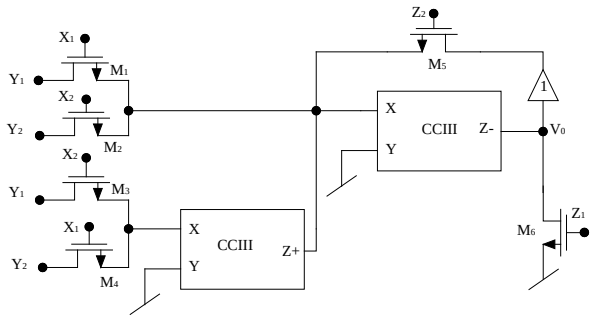


Figure 3. Four Quadrant Analog Multiplier/Divider employing CCIII.

Here, a well-established approach[14] has been considered to deduce the FQAMD of Figure 3 using CCIII where all MOS transistors are operating in triode region. The drain current equation for the MOS transistor, working in triode region, is given by (7).

$$I_D = K\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{7}$$

Where K= μ.Cox (W/L)

Let the current flowing from M_1 and M_2 is I_{D1}, given in (8), the current flowing from M_3 and M_4 is I_{D2}, represented in (9) and the current flowing through M_5 and M_6 is I_{D3} and $I_{D4,}$ expressed by (10) and (11) respectively.

$$I_{D1} = K\left[(X_1 - V_{TH})Y_1 - \frac{Y_1^2}{2}\right] + K\left[(X_2 - V_{TH})Y_2 - \frac{Y_2^2}{2}\right] \tag{8}$$

$$I_{D2} = K\left[(X_2 - V_{TH})Y_1 - \frac{Y_1^2}{2}\right] + K\left[(X_1 - V_{TH})Y_2 - \frac{Y_2^2}{2}\right] \tag{9}$$

$$I_{D3} = K\left[(Z_2 - V_{TH})V_0 - \frac{V_0^2}{2}\right] \tag{10}$$

$$I_{D4} = K\left[(Z_1 - V_{TH})V_0 - \frac{V_0^2}{2}\right] \tag{11}$$

Now considering the aspect ratios of MOS transistors M_1 to M_4 as (W_A/L_A) and that of M_5 and M_6 as (W_B/L_B), by routine analysis, the output voltage (V_0) can be written as given in (12), where, again, all the utilized NMOS transistors are assumed to be operating in the triode region.

$$V_0 = \frac{(W_A/L_A)\,(X_1 - X_2)(Y_1 - Y_2)}{(W_B/L_B)(Z_1 - Z_2)} \tag{12a}$$

or

$$V_0 = \frac{(W_A/L_A)\,\Delta X.\Delta Y}{(W_B/L_B)\Delta Z} \tag{12b}$$

where $\Delta X= X_1-X_2$ and $\Delta Y=Y_1-Y_2$ and $\Delta Z=Z_1-Z_2$.

Now, again, if the aspect ratios, of all the used MOS transistors, are considered to have the same value, then the expression for the output voltage is independent of the MOS transistor parameters. Thus, for V_T being the threshold voltage of the MOSFETs, following conditions needs to be satisfied for them to operate in triode region.

$$Y_1, Y_2 \le \min\,[(X_1 - V_T),(X_2 - V_T)] \quad \text{for } M_1 \text{ to } M_4 \tag{13}$$

$$\text{and} \quad V_0 \le \min\,[(Z_1 - V_T),(Z_2 - V_T)] \text{ for } M_5 \& M_6 \tag{14}$$

The FQAMD circuit of Figure 3 works as a four quadrant multiplier when, X and Y terminal acts as input terminals and at Z terminal some controlled voltage is applied. In such a case, V_0 is the result of multiplication of potential difference $(X_1 - X_2)$, $(Y_1 - Y_2)$ with some constant gain. If X_1 and X_2 are of the form (X + x) and (X - x) respectively, where X is the DC component while x is the signal component and if Y1 and Y2 are defined by the relation i.e. $Y_1=-Y_2= y$ again being another signal component with Z terminal having $Z_1=V_{z1}$ and $Z_2=V_{z2}$, both being DC control voltages then

$$V_0 = \frac{4.\,(W_A/L_A)\,x.y}{(W_B/L_B)(V_{z1}\text{-}V_{z2})} \tag{15}$$

Additionally, (12a) represents a divider when either of the potential differences $(X_1\text{-}X_2)$ or $(Y_1\text{-}Y_2)$ is kept constant, say $(X_1\text{-}X_2)$ in this case. This $(X_1\text{-}X_2)$ acts as constant gain along with the gain provided by transistor aspect ratios. Now, V_0 is the result of the divider with some constant gain.

This FQAMD, the multiplier and divider configuration, has been utilized in Figure 2 to build the cubic circuit.

4. Simulation Results

We present now, in the following, the SPICE simulation validations for the multiplier, divider and the cubic circuit. Additionally, we have also shown SPICE simulations for

squarer and an amplitude modulator to further establish the working of the FQAMD realization of the Figure 3. The CMOS CCIII structure of[34] used here is redrawn in Figure 4. The aspect ratios of these MOS transistors are given in Table 1. We have used 0.35μm, level 3 CMOS model parameter for the testing the above mentioned configurations which are given in Table 2. The supply voltage considered is V_{DD}= -V_{SS}=1.6V and values of the bias voltages are V_{BIAS1}= -0.38V and V_{BIAS2}=-0.9V.

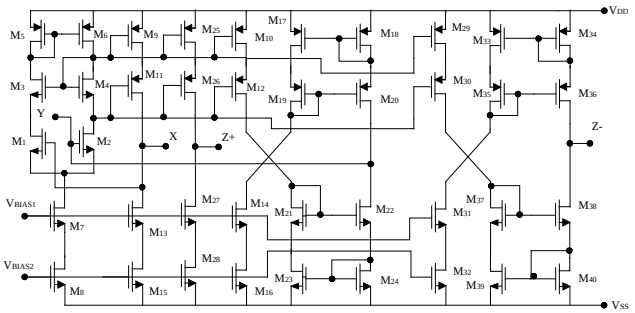


Figure 4. Third generation current conveyor (CCIII)[34].

Table 1. Aspect ratios of the MOSFETs of CCIII of Figure 4

CMOS transistors	W/L (in μ/m)
M1-M4	10/0.35
M5,M6	16/0.35
M7, M8, M13-M16, M21-M24, M27,M28, M31, M32, M37-M40	16/0.35
M9-M12,M17-M20, M25, M26, M29, M30, M33-M36	30/0.35

In the following we give separately the detailed account of the simulations of various tested configurations namely; multiplier, divider, squarer, amplitude modulator and cubic circuit. We have also given in the end a frequency response characteristic of the FQAMD.

4.1 Multiplier

For the simulation purpose value of X was taken to be 3V while x was varied from -300mV to +300mV. The potential difference (Y_1 - Y_2) was varied from -200mV to +200mV. V_{Z1} and V_{Z2} were kept constant at 4.1V and 2.85V respectively, maintaining a constant potential difference of 1.25V. All transistor aspect rations were kept same as W/L = 1.05μm /0.35μm. Now the output potential was plotted for different values of (Y_1 – Y_2). The output waveform of the, circuit given in Figure 3 when acts as a four-quadrant multiplier, is shown in Figure 5. In Figure 5 'cross marked' sign shows the theoretical output whereas continuous line represents simulated output. As can be seen in the Figure 5, the results are in agreement with the theoretical results to a high degree.

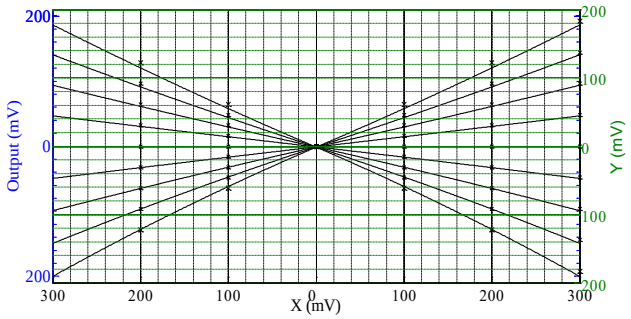


Figure 5. DC transfer characteristics of the designed circuit as a FQAM.

Table 2. 0.35 *μm*CMOS process parameters utilized in simulation

.MODEL NMOS1 NMOS (LEVEL = 3
+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871
+ PHI = 0.7 VTO = 0.5445549 DELTA =0 UO = 436.256147 ETA = 0
+THETA = 0.1749684 KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081
+ RSH =0.0559398 NFS = 1E12 TPG = 1 XJ = 3E-7 LD = 3.162278E-11
+WD = 7.046724E-8 CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO= 1E-10
+CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504 CJSW = 3.777852E-10 MJSW = 0.3508721)
.MODEL PMOS1 PMOS (LEVEL = 3
+ TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894
+ PHI = 0.7 VTO = -0.7140674 DELTA =0 UO = 212.2319801 ETA = 9.999762E-4
+THETA = 0.2020774 KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5
+RSH =30.0712458 NFS = 1E12 TPG = -1 XJ = 2E-7 LD = 5.000001E-13
+WD = 1.249872E-7 CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10
+CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5 CJSW = 4.813504E-10 MJSW = 0.5)

4.2 Divider

For the purpose of simulation, the values taken were X_1 = 3V, X_2 = 2.95V (making the potential difference (X_1-X_2) = 50mV). All transistor aspect rations were kept same as W/L = 1.05µm /0.35µm. Now the output potential was plotted for five different values of (Y_1 – Y_2). The SPICE plot showing the division output using the above values is given in Figure 6.

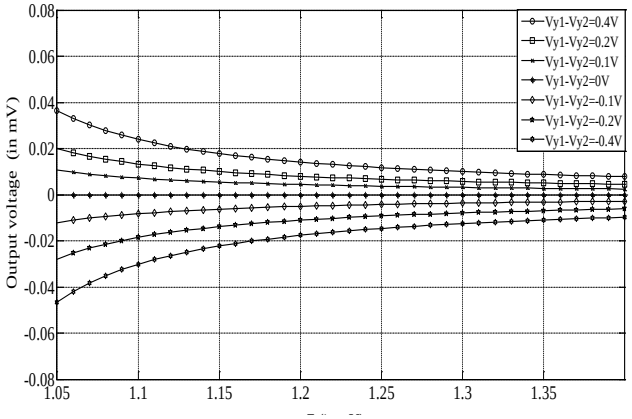


Figure 6. DC transfer characteristics of the designed circuit as a Four Quadrant Analog Divider.

4.3 Squarer

In order for the circuit to act as a squarer, the potential difference (Z_1-Z_2) must be kept constant, while the potential difference (X_1-X_2) and (Y_1-Y_2) must be kept same and equal to the required squarer input. During the simulation the values of these potentials were V_{Z1} = 2.5V, V_{Z2} = 1.25V (thus making the potential difference (Z_1-Z_2) = 1.25V). X_1 and X_2 were taken to be of the form (X+x) and (X-x) respectively where X was taken as a constant DC voltage (2.5V) while x was taken to be a sinusoidal wave of 100mV and 100 KHz frequency. Similarly, Y_1 and Y_2 were taken to be of the form (y) and (-y) respectively where y was taken as a sinusoidal wave of 100mV amplitude and 100 KHz frequency. Thus, both the potential differences (X_1-X_2) and (Y_1-Y_2) were sinusoidal waves of 200mV amplitude and 100 KHz frequency which acted as the input to squarer. The transistor aspect rations were same as used in previous case. The simulation result is shown in Figure 7 which resembles the theoretical result to a high degree.

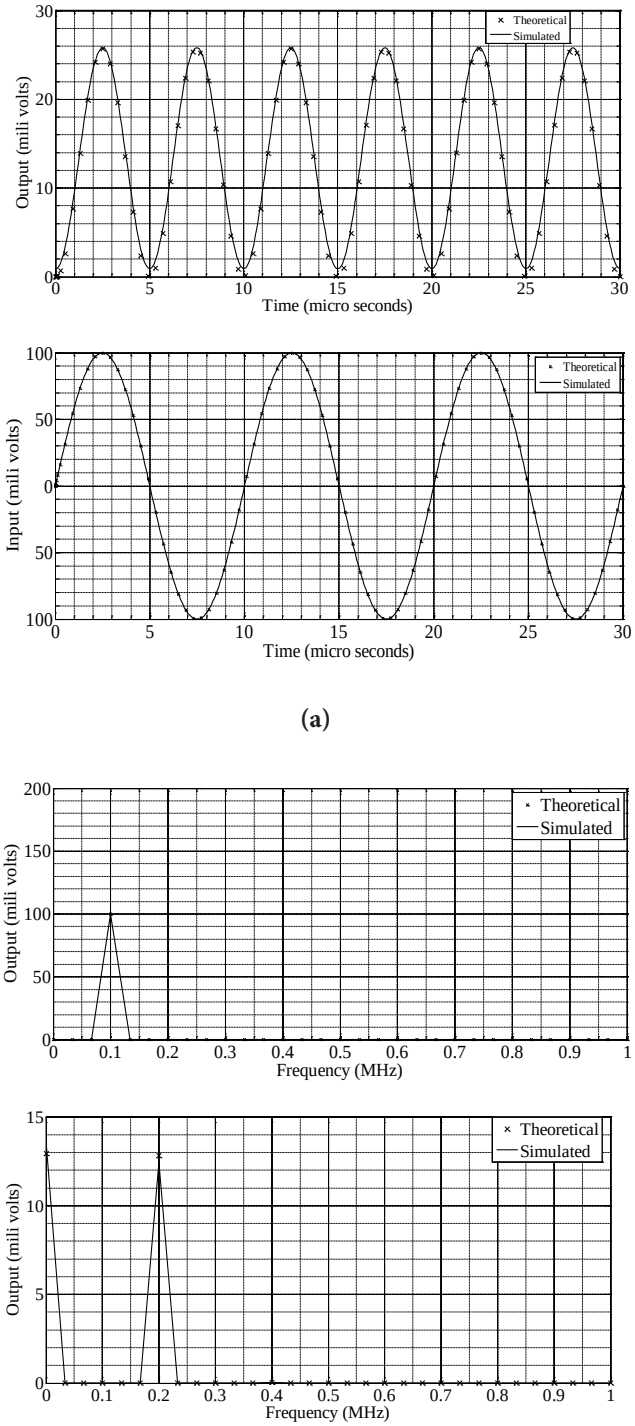
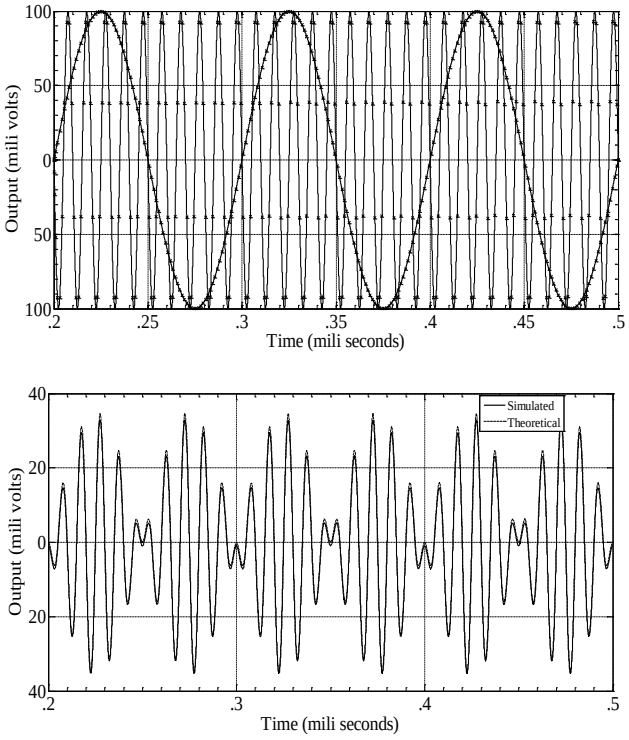


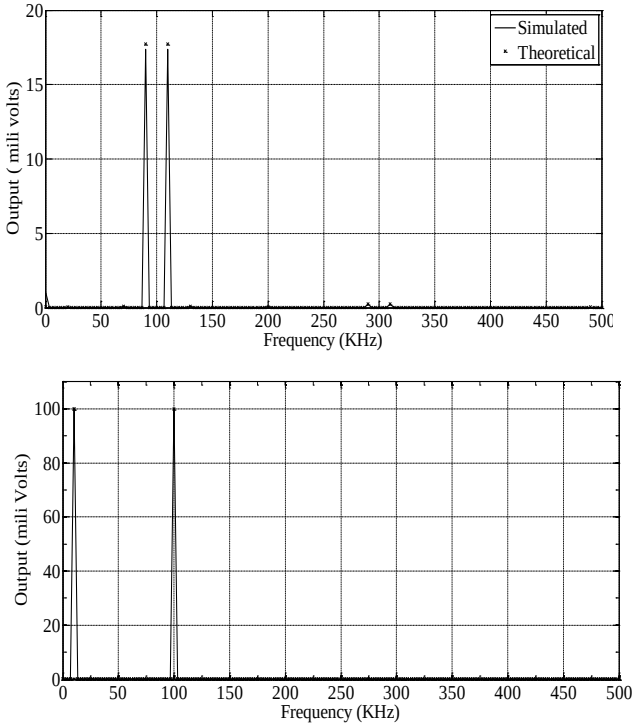
Figure 7. DC transfer characteristics of the designed circuit as a Four Quadrant Analog Divider.

4.4 Amplitude Modulator

In order for the circuit to act as an amplitude modulator, the potential difference (Z_1-Z_2) must be kept constant, while the carrier signal and modulating signal must be applied at (X_1-X_2) and (Y_1-Y_2). During the simulation, the values of these potentials were Z_1 = 2.5V, Z_2 = 1.25V (thus making the potential difference (Z_1-Z_2) = 1.25V). X_1 and X_2 were taken to be of the form (X+x) and (X-x) respectively where X was taken as a constant DC voltage (1.25V) while x was taken to be a sinusoidal wave of 100mV amplitude and 100KHz frequency. Thus the potential difference (X_1-X_2) acted as a carrier wave of 200mV, 10KHz frequency. Similarly, Y_1 and Y_2 were taken to be of the form y and –y respectively where y was taken as a sinusoidal wave of amplitude 100mV and 100 KHz frequency. Thus, the potential differences (Y_1-Y_2) acted as a modulating wave of 200mV and 100 KHz frequency. The transistor aspect rations were same as used in previous case. The simulation result is shown in Figure 8, which match the theoretical results.



(a)



(b)

Figure 8. Simulation results of the proposed circuit as an amplitude modulator (AM) circuit (a) time –domain response (b) frequency domain response.

4.5 Frequency response characteristic of the FQAMD

In order to obtain the frequency response of the FQAMD circuit, the values of the input potentials were chosen to be V_{Z1} = 4.1V, V_{Z2}= 2.85V (making Z_1-Z_2 = 1.25V), Y_1 = 250mV, Y_2 = -250mV (making Y_1-Y_2 = 500mV). X_1 and X_2 were taken to be of the form (X+x) and (X-x) respectively where X was taken as a constant DC voltage (0.25V) while x was taken to be a sinusoidal wave of 0.5mV and varying frequency (making X_1-X_2 to be sinusoidal wave of amplitude 1mV and varying frequency). The output potential was plotted against the frequency to obtain the frequency response shown in Figure 9. By simulation we have obtained the bandwidth to be 112.63MHz.

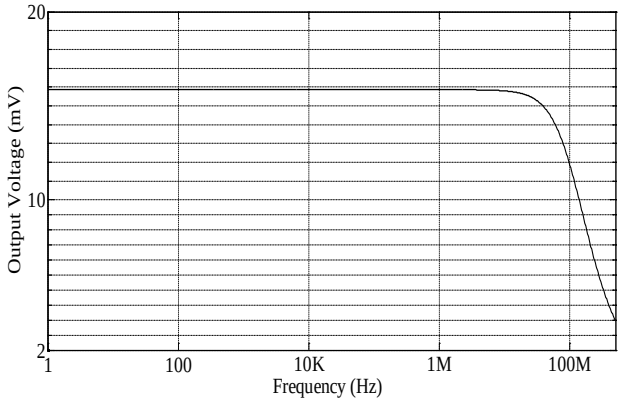
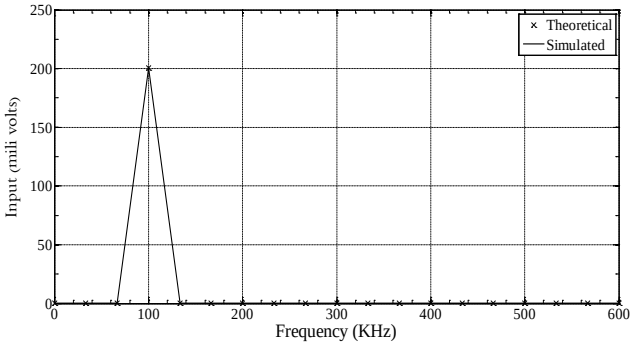


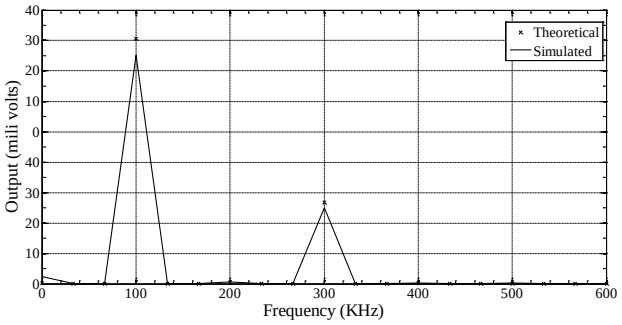
Figure 9. Frequency response of the proposed FQAMD circuit.

4.6 Cubic Circuit

For testing the functionality of the cubic circuit generator, three FQAMD blocks have been employed as shown in Figure 2. The outputs of the FQAMD circuits have been used as an input to the 3rd block of FQAMD. The final output is the output of the 3rd block of FQAMD. For simulation purposes, X_1 and X_2 were taken to be of the form (X+x) and (X-x) respectively where X was taken as a constant DC voltage (2.5V) while x was taken to be a sinusoidal wave of 100mV and 100 KHz frequency. Thus, both the potential differences (X_1-X_2) was sinusoidal waves of 200mV amplitude and 100 KHz frequency which acted as the input to cubic circuit. During the simulation the values of these potentials were V_{Z1} = 2.5V, V_{Z2} = 1.25V. The transistor aspect rations were constant as used in previous case. The simulation result is shown in Figure 10, which validates the working of the circuit as a cubic generator.



(a)



(b)

Figure 10. Frequency domain response of the proposed circuit as a cubic circuit (a) input waveform (b) output waveform.

The above simulation results demonstrate the validity of the theoretical assertions of the realized new cubic circuit. The simulations also justify the results of multiplier, divider, squarer and the amplitude modulator. The frequency response of our FQAMD shown in Figure 9 demonstrates improvement with respect to the frequency response one recent related work[27].

5. Conclusion

A complete CCIII-based new cubic circuit has been presented which fills to some extent the void of a CCIII-based non-linear applications. The cubic circuit presented utilized our CCIII-based FQAMD circuit derived from that of[14]. Other non-linear applications of the presented CCIII-based FQAMD namely; multiplier, divider, squarer and amplitude modulator were also tested and found to be working as expected. All worked out PSPICE simulations validate the theoretical results of the proposed configurations.

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