Indian Journal of Science and Technology, Vol 9(38), DOI: 10.17485/ijst/2016/v9i38/101940, October 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Implementation of FPGA based DPWM-Digital PI Closed Loop Controller for Voltage Regulation

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Abstract

Objectives: In this paper, a Field Programmable Gate Array (FPGA) based real time implementation of a closed loop controller for regulating the load voltage under line and load disturbances by generating Digital Pulse Width Modulation (DPWM) is developed. Digital Proportional Integral (DPI) controller is designed to generate the DPWM. **Methods**: DPWM are developed by two methods: Counter based and Delay line based. The closed loop DPWM activated DC-DC buck converter is simulated using MODELSIM and tested in real time using Xilinx Spartan 3A DSP FPGA. **Findings:** Hardware results show the regulated load voltage by updating the DPWM control signal duty cycle to compensate the line and load disturbances. FPGA based DPWM provides less complexity in design. **Improvements:** Hybrid based DPWM method with closed loop control for DC-DC Buck converter could be used for voltage regulation.

Keywords: Closed Loop Controller, Digital PI, DPWM, FPGA

List of Abbreviations

ADC	Analog to Digital Converter
CSV	Comma Separated Values
CMOS	Complementary Metal Oxide Semiconductor
DPI	Digital Proportional Integral
DPWM	Digital Pulse Width Modulation
DSP	Digital Signal Processing
DC	Direct Current
DVM	DC Value Match
FPGA	Field Programmable Gate Array
LCD	Liquid Crystal Display
NEV	Negative Error Value
PEV	Positive Error Value
PI	Proportional Integral
PID	Proportional Integral Derivative
PWM	Pulse Width Modulation
SR	Set Reset
VHDL	Very High Speed Integrated Circuit Hardware Description Language
ZEV	Zero Error Value
ZVM	Zero Value Match

1. Introduction

The converter is a device which converts the unregulated DC voltage into a regulated DC voltage. DC-DC Converters are of different types, namely buck converter, boost converter, buck-boost converter, cuk converter, and full-bridge converter. The buck converter is used in many real time applications like control of rotor induction generator[1], on-board battery charger[2] and electric vehicles batteries[3]. The buck converter has low input ripple when connected in the current-sourced and voltage-sourced dc-to-dc converter topologies[4]. For the DC-DC converters, development of feedback controller enhances its performance. The one cycle control method for line and load disturbances is very simple[5].

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The real time implementation of digital PID controller is simplified with the help of FPGA[6]. The time domain analysis with sampling effects leads to the estimation of voltage regulation error and its compensation for the DPWM in dc-to-dc converter[7]. The smooth controller transition was achieved by FPGA based unified multi-mode DPWM controller[8]. The low cost FPGA implementation is suitable for high frequency and high resolution DPWM[9].

In our work, we have concentrated on the FPGA based control of DC-DC converter where simple buck DC-DC converter is selected as test bed. A digital PI controller and digital pulse width modulation are developed in to regulate the load voltage under line and load disturbances.

1.1 Buck Converter

The buck converter is a DC-DC converter which accepts a DC voltage signal and produces a reduced regulated voltage signal by a switching control. This switching control is analog in most of the applications. The digital switching control has more advantages than the analog switching control like easy designing, high manipulation power, easy up gradation, immune to environmental changes, easy debugging.

The operation of the buck converter is related to the duty cycle as

$$Vout = d.Vin$$

Where "Vin" is the input voltage of the buck Converter
"Vout" is the load voltage of the buck Converter
"d" is the duty cycle.

The duty cycle "d" is the ratio of the ON period and the period of the controlling square pulse.

$$d = \frac{Ton}{T}$$

Where "Ton" refers to the ON period
"T" refers to the time period of the cycle

2. Digital Pulse Width Modulation Techniques

The simulation block set model of buck converter with the DPWM technique is shown in the Figure1. In general, the PWM is generated by comparing the DC signal with the high frequency saw tooth carrier wave. In this work, the Digital Pulse Width Modulated (DPWM) signal is generated using logical design. The DPWM is generated by the following methods. They are

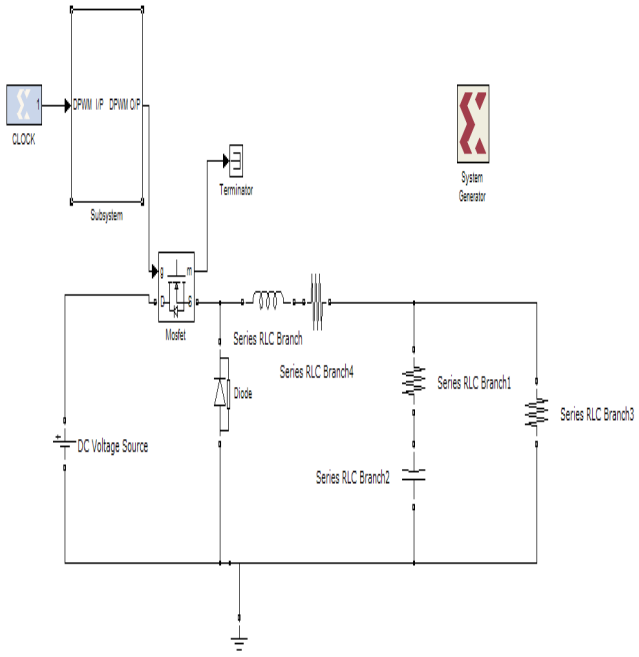

Figure 1. SIMULINK-MATLAB blockset model of DC to DC buck converter with DPWM control.

2.1 Counter based DPWM Method

In counter based DPWM generation method, an asymmetric carrier wave is generated by the counter. The counter based DPWM method can be designed in three ways depending on the triggering direction of the counter circuit. If the direction of the counter is in increasing value (UP COUNTER), then it is called as leading edge counter based DPWM. If the direction of the counter is in decreasing order (DOWN COUNTER), then it is called as trailing edge counter based DPWM. If the direction of the counter is increasing and decreasing (UP/DOWN COUNTER), then it is called as triangular counter based DPWM. Switching period value is equivalent to the highest count value. The block diagram of the counter based DPWM is given in Figure 2. The first comparator block finds the initial value match (namely zero "0") of the counter. This is referred as "Zero Value Match" (ZVM). The second comparator block finds the match value between the counter and the digitized DC input value. This is

referred as "DC Value Match" (DCVM). The ZVM is the input to the SET and DCVM is the input to the RESET of the SR-flip flop. The SR-flip flop is triggered by these two signals namely SET and RESET to generate the DPWM.

In this paper, the 11-bit resolution counter based DPWM is used. That is the counter circuits generate the asymmetric carrier for the period value of 2047 and therefore a DC value is converted to 11-bits to obtain the matched values ZVM and DCVM. The ZVM and DCVM are utilized by the SR-flip flop to generate the DPWM signal.

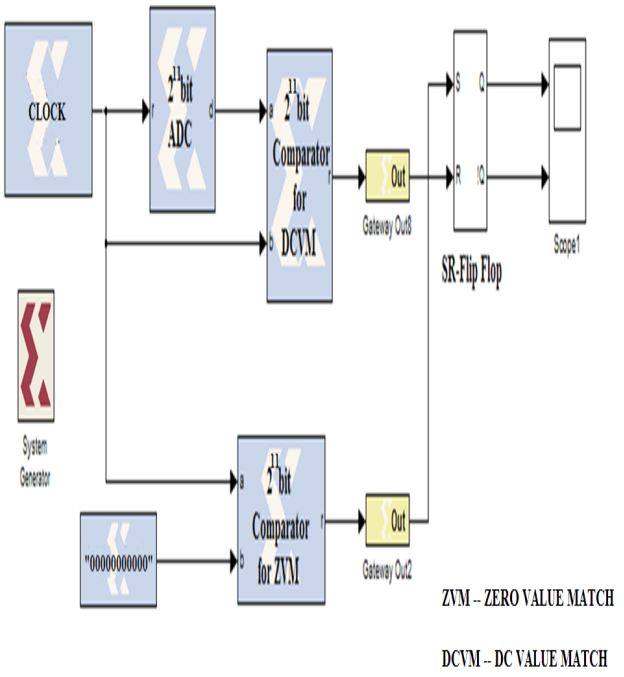

Figure 2. SIMULINK-MATLAB blockset of Counter based DPWM.

2.2 Delay Line based DPWM Method

Figure 3 shows the SIMULINK-Xilinx block set for the 11-bit resolution delay line based DPWM method. Delay line based DPWM generation method involves the 211 ring counter, 2048:1 multiplexer and SR-flip flop. The converted 11-bit DC value is fed as select line for the 2048:1 multiplexer. 211 Ring counter is connected to the input side of the 2048:1 multiplexer through 2048 D-flip flops as shown in Figure 4. The SET signal of SR-flip flop is enabled by the 2047th pin of the ring counter through its corresponding D-flip flop. The RESET signal of SR-flip flop is enabled by the 2048:1 multiplexer output. Thus the DPWM is generated by the SR-flip flop to operate the DC-DC buck converter. For Real time implementation, a closed loop PI controller is developed for load voltage regulation. The output of the PI controller is the 11-bit DC value used in the above methods.

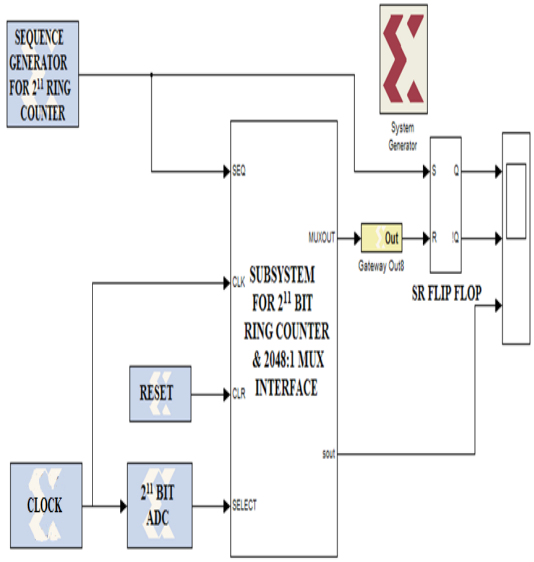

Figure 3. SIMULINK-MATLAB blockset model of Delay line based DPWM.

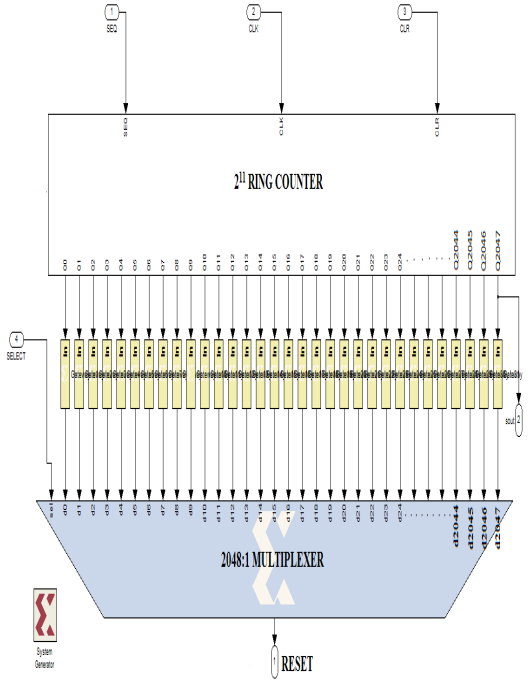

Figure 4. SIMULINK-MATLAB blockset for 211 Ring Counter and 2048:1 Multiplexer Subsystem.

2.3 Real Time Digital PI Controller

Digital Proportional and Integral controller (DPI) is used for controlling/regulating the load voltage of the buck DC-DC system. The DPI controller is designed in the Z-domain. The general PID controller is given by

$$u(t) = k_p e(t) + k_i \int e(t)dt + k_d \frac{de(t)}{dx} \quad (1)$$

The value for k_d is '0', as the PI controller is used.

$$u(t) = k_p e(t) + k_i \int e(t)dt \quad (2)$$

Taking Laplace Transform

$$U(s) = K_p + \frac{K_i}{s} \quad (3)$$

Using Bilinear Transformation,

Consider

$$s = \frac{(1 - z^{-1})}{T} \quad (4)$$

Now

$$U(Z) = K_p + \frac{K_i}{(1 - z^{-1})} \quad (5)$$

Solving the equation (4) gives

$$U(Z) = \frac{(K_p + K_i) - K_p Z^{-1}}{(1 - Z^{-1})} \quad (6)$$

Let $K_1 = K_p + K_i$ and $K_2 = -K_p$ in the equation (6),

$$U(Z) = \left[\frac{K_1 + K_2 Z^{-1}}{(1 - Z^{-1})}\right] E(Z) \quad (7)$$

The discrete Z-domain equation is

$$U(Z) = K_1 E(Z) + K_2 Z^{-1} E(Z) + Z^{-1} U(Z) \quad (8)$$

Taking Inverse Z-Transform of the equation (8) gives

$$u(k) = k_1 e(k) + k_2 e(k-1) + u(k-1) \quad (9)$$

The equation (9) is designed using VHDL coding and used in the Spartan Xilinx 3A DSP FPGA kit. The K_p and K_i values are obtained by Ziegler and Nichols tuning method.

Specifications for the buck converter used in our work are shown in Table 1.

The developed DPI controller manipulates the DC value for the difference in the error.

3. Field Programmable Gate Array

The Xilinx Spartan 3A DSP FPGA is used in the implementation of the designed controller for the DC-DC buck converter. The Xilinx Spartan 3A has inbuilt ADC. The set point variations are provided by the VHDL code and can be viewed in the LCD display by developing an activation code in VHDL. The feedback load voltages are fed to the Xilinx Spartan 3A DSP FPGA as input via a signal conditioning circuit of range 0-5V. The input values to the FPGA are amplified 10 times more than the actual input values in our work . This scaling is done to the fractional input values of the ADC and PI considered in the design, as the Xilinx Spartan 3A DSP kit do not support the floating value.

Table 1. Specification of Buck Converter in Matlab-Simulink Model

V_{in}	V_{out}	L	C	Load
21V	9.4V	1μH	22μF	10 ohms

3.1 Analog to Digital Converter

AD7266 is the analog to digital converter used in the Xilinx Spartan 3A DSP kit.AD7266 is a dual, 12-bit, high speed, low power device. This ADC device accepts the Analog data through the channel and its equivalent is coded in multiples of 100. If the value is 10, then the ADC recognises it as 100. These values are easy to manipulate within the FPGA, as the float values are not supportive when implemented using Xilinx Spartan 3A DSP FPGA. The 11-bit ADC is used in this design.

The AD 7266 used in the kit is in the range of 0 to 5V. In closed loop system, the value of the feedback is easily more than the range of the ADC. For the sake of stability, the VHDL code is utilised to down scale the feedback value to match within the preferred range of the AD7266. The VHDL coding is designed in behavioural modelling taking into consideration of the logical operation of the AD7266 along with its triggering signals.

3.2 Resolution

Resolution refers to the number of bits used in the design. In this work, the two DPWM methods are designed using 211 bit resolution. The counter based DPWM method uses a 211 bit (2047 count) counter. The delay line based DPWM method uses the 2048:1 multiplexer. In our

Figure 5. Counter based DPWM generated in Model Sim.

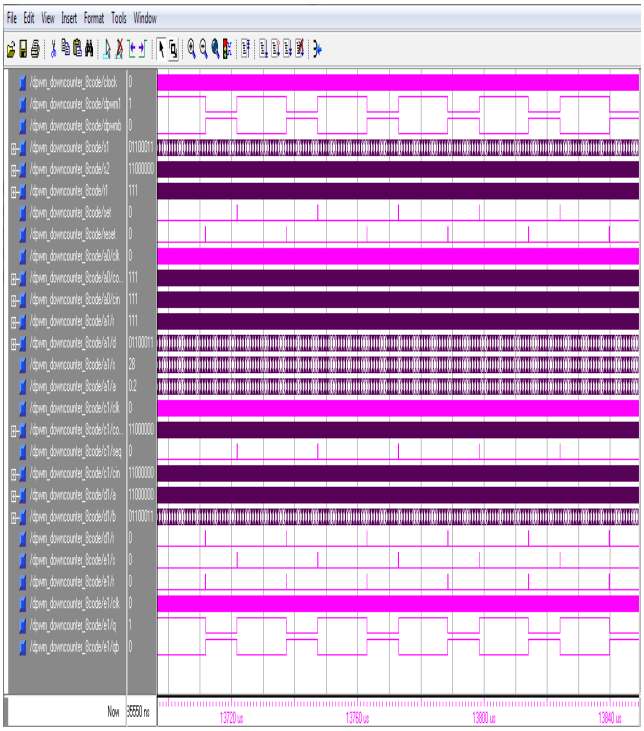

Figure 6. Delayline based DPWM generated in Model Sim.

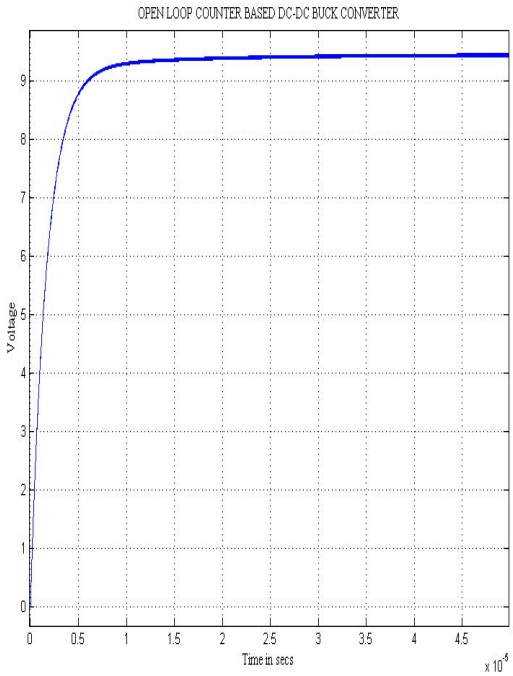

Figure 7. Simulation open-loop output of counter based DPWM dc-dc buck converter under line disturbance.

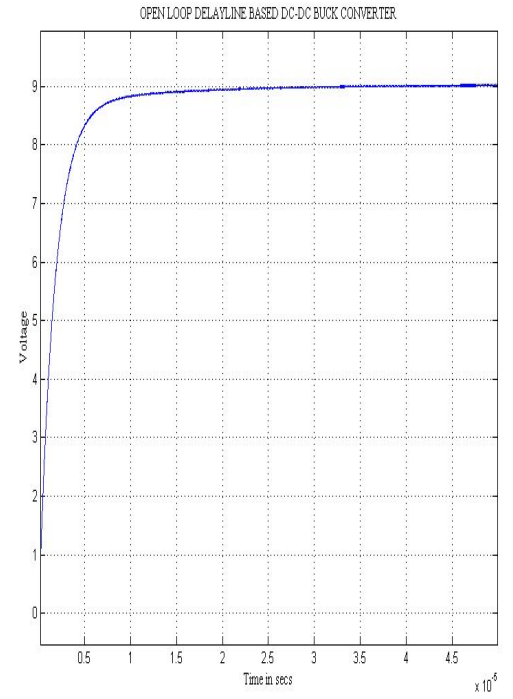

Figure 8. Simulation open-loop output of delayline based PWM dc-dc buck converter under line disturbance.

work, the switching frequency of the DPWM generated by the above methods is 12.5 KHz to match the hardware requirement. To achieve this frequency, the DPWM switch patterns are to be adjusted as per the scaled value given by the formula.

$$\text{Scaled}_{\text{value}} = \frac{1}{2^n \text{ X Output frequency X Clock period}}$$

Where clock period is 100ns

4 Results

4.1 Simulated Results

The simulation outputs of the DPWM generation using the two techniques are given Figure 5 & 6. Model Sim software was used for the simulation of DPWM generation. The open loop step variation for the DC-DC buck converter is given for the two DPWM techniques in Figure 7 & 8.

4.2 Experimental Results

The hardware output of load disturbances (positive and negative) for closed loop dc-dc buck converter with digital PI controller using three DPWM generation techniques are shown in Figure 9-12. Figure 13 & 14 depicts the load disturbances imported from the CSV format file. The experimental setup for the closed loop dc-dc buck converter analysis is shown in Figure 15.

Table 2 and Table 3 details about the positive and negative load disturbance for the closed loop dc-dc buck converter. The delay line based DPWM is best suit for the positive load disturbance and counter based DPWM is best for the negative load disturbance. Table 4 depicts no change in either of the DPWM methods for both positive and negative load disturbances.

Table 2. Hardware Closed Loop Transient Time Performance Indices of Positive Line Disturbance of Dc-Dc Buck Converter for the DPWM Techniques

Methods	**Counter based DPWM**	**Delay Line based DPWM**
Rise Time (t_r)	0.1	0.24
Time Delay (t_p)	0.05	0.12
Settling Time (t_s)	3.3	2.84
Percentage Overshoot (% MP)	14.2857%	14.0%
Steady State Voltage Ripple	0.0357	0.0204
Normal Value	11 V	9.8 V
Disturbance Value	12.8 V	11.4 V

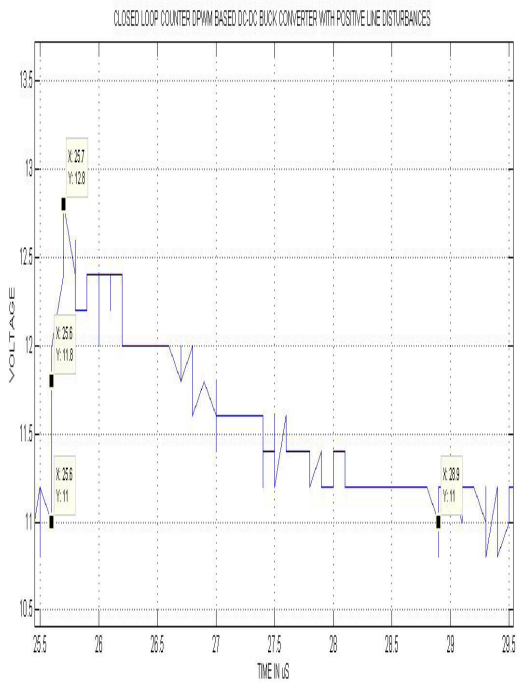

Figure 9. Counter DPWM PI control based DC-DC buck Converter with positive line disturbance from 11V to 12.8V.

Table 3. Hardware Closed Loop Transient Time Performance Indices of Negative Line Disturbance of Dc-Dc Buck Converter for the DPWM Techniques

Methods	**Counter based DPWM**	**Delay Line based DPWM**
Rise Time (t_r)	0.2	0.3
Time Delay (t_p)	0.1	0.15
Settling Time (t_s)	3.8	5.2
Percentage Overshoot (% MP)	14.2857%	14.2857%
Steady State Voltage Ripple	0.035714	0.0204
Normal Value	11 V	9.8 V
Disturbance Value	9.6 V	8.4 V

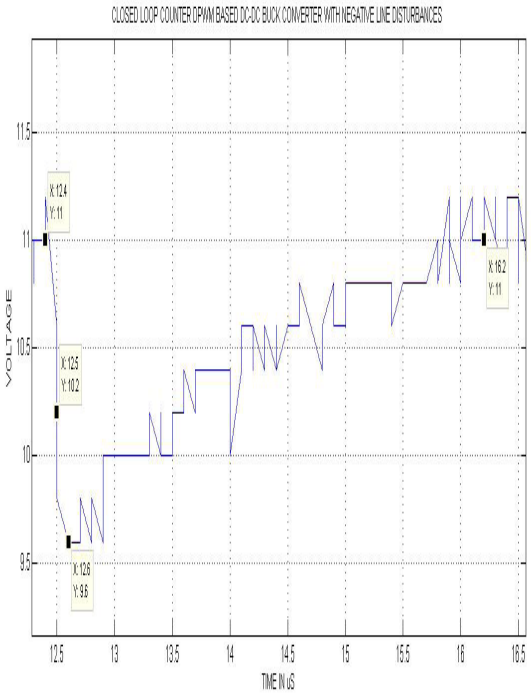

Figure 10. Counter DPWM PI control based DC-DC buck Converter with negative line disturbance from 11V to 9.6V.

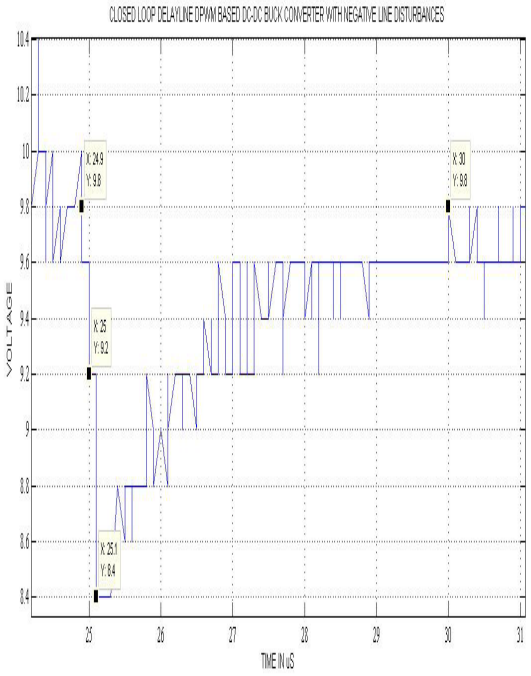

Figure 12. Delayline DPWM PI control based DC-DC buck Converter with negative line disturbance from 9.8V to 8.4V.

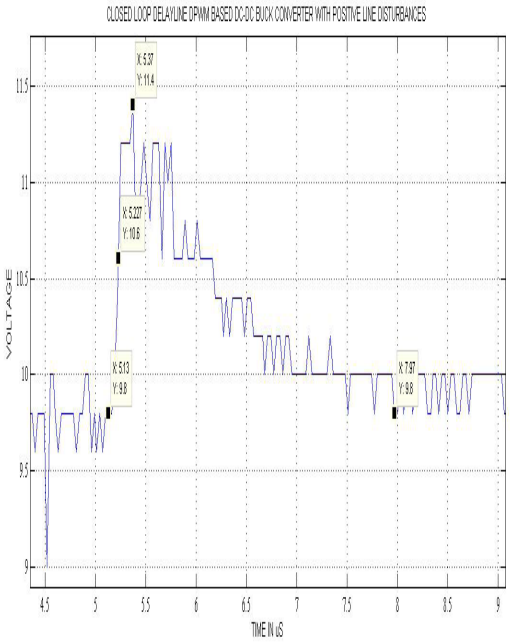

Figure 11. Delayline DPWM PI control based DC-DC buck Converter with positive line disturbance from 9.8V to 11.4V.

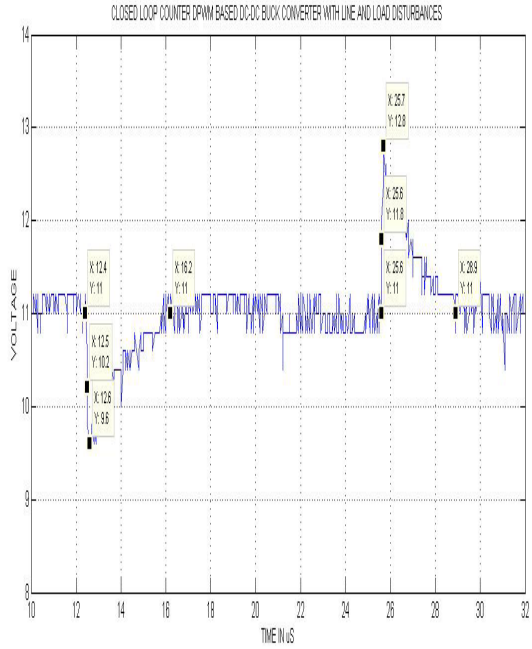

Figure 13. Closed loop Counter DPWM controlled dc-dc buck converter with Line Disturbances.

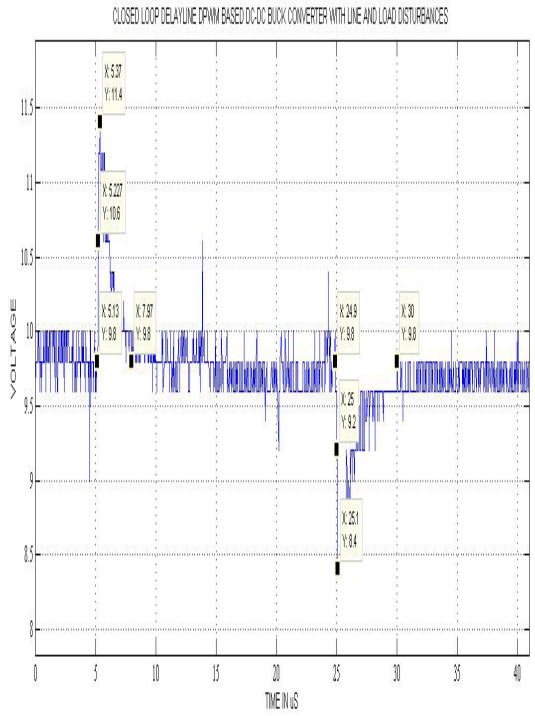

Figure 14. Closed loop Delayline DPWM controlled dc-dc buck converter with Line Disturbances.

Figure 15. Experimental Setup for the Digital PI based DC-DC Buck Converter.

Table 4. Hardware Closed Loop for positive and Negative Load Disturbance of Dc-Dc Buck Converter for the DPWM Techniques

Methods	Counter based DPWM	Delay Line based DPWM
Positive Load Disturbance 470 Ω to 495 Ω	NC	NC
Negative Load Disturbance 470 Ω to 445 Ω	NC	NC

5. Conclusion

Hardware results show that the Digital PI controller performance is satisfactory in regulating the load voltage of DC-DC buck converter under disturbances. Delay line based DPWM shows less steady state ripple compared to counter based DPWM. Counter based DPWM show less settling time. Output responses of FPGA based hardware implementation using Xilinx Spartan 3A DSP proves the reliability of the tool for power converter applications. Online updation of control duty cycle in response to the transients to regulate the output response shows the effectiveness and reliability of the FPGA tool.

6. Acknowledgement

The authors would like to thank the department of Electronics and Instrumentation Engineering, Annamalai University, Chidambaram, India for the facilities and assistance provided in the laboratory.

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