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Timing Aware IR Drop Analysis in Microprocessor without Interlocked Pipelined Stage (MIPS) Design using Power/Ground Padding

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Abstract

Objectives: In this paper, the authors perform the physical design flow of Microprocessor without Interlocked Pipelined Stage MIPS, which is register based architecture in detail which aims to minimize IR drop in pre-circuit stage. The intent of this work is to analyze the IR drop and to make sure that the power supply is delivered across the entire chip. Technology shrinking makes it difficult to deliver complete supplied voltage to all the placed standard cells. And it becomes difficult to meet the slack time. The placement algorithm has also been proposed in the work. **Methods/Statistical Analysis:** The switching activity of the clock signal dynamically varies the IR drop at each buffer. Hence, depending on the level of IR drop, the current delivered by the buffers will be varied. This has led to the fluctuation of the supply voltage, which in turn causes variations in the delay, skew and slew rates. These effects necessitate the detailed timing analysis of the circuit. It can be observed that 10% IR drop causes an increase in delay of about 5% to 10%. **Findings:** The Register Transistor Level of MIPS design has been converted into net-list using Cadence Encounter RTL Compiler. The net-list is imported in Encounter GDSII for the Physical Designing. The Cadence Encounter Digital Implementation (EDI) used in the paper is 90 nm technology. The floor plan results of the design shows that the cells utilization is 70% and rest of the 30% is left for routing the design. The fly-line analysis is done in floor-planning stage to estimate the placement of the logic cells. The core utilization is 69% while the distance between the core and die is10 µm. The circuit is operated with the supply voltage 1.628 V and the IR drop analysis has been performed to all the standard cells in the design. The design also meets Slack time, Setup time, Hold time. Thus the Timing Aware IR drop has been analyzed in the paper. The MIPS design operates at 100 MHz Frequency. The MIPS design shows an appreciable decrease in the turnaround time which is 2.38 ns. **Application/Improvements:** The physical design of MIPS gives better IR drop and turnaround time. Power consumption in pre-placement, post-placement of the design is reported to be 11.37 mW and 11.77 mW.

Keywords: Cadence Encounter, IR Drop Analysis, MIPS, Physical Design

1. Introduction

The VLSI design cycle includes specification of the required system, architecture of the system, behavior or functional design of the system, logic design, circuit design of the system, physical design, fabrication, packaging, testing and finally debugging. Thus, the above mentioned flow is universally accepted and is applicable in all aspects. The work follows the design steps reported in[1] to analyze and minimize the IR drop in the synthesis of MIPS. The area specification of IC-die is 228962 µm^2 and core area is 219492 µm^2. The supply voltage is 1.620 V. Using advanced process technology, transistor size is scaled down for high density design. Lower supply voltage permits lower noise margins and smaller IR drop on the power/ground network. The increase in the complexity of design leads to increases in area and power consumption. Narrow wires can be preferred for interconnectivity, but have high resistance, which leads to an increase in IR drop of the design. Hence, metal layers are more preferable for routing longer signal and power in the design of larger chips.

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An IR drop on-chip PDN in an array and in a wire-bond model has been analyzed in[1,2] illustrates that the IR drop greatly affects the performance of the design. The high speed requirements with a constraint of DSM make a compulsion to work on clock skew verification. Minimization of clock skew with minimization of IR drop becomes a very difficult task. This task has been implemented in the proposed paper. By the proper placement of P/G pads at the chip peripheral area, there is a considerable reduction in the IR drop on an entire chip. The number of package pins decides the number of P/G pads.

The proposed work mainly focuses on minimization of IR drop on MIPS design. The power/ground padding methodology has been used to minimize the IR drop across the chip.

2. Physical Design

The physical designing requires certain files as an inputs and it produces a respective outputs. Before going to PD, synthesis is one of the main steps. This step gives a logical functionality of the given RTL design. The input to the synthesis step is verilog files, constraint files and library files. The outputs are area, timing and power report. The inputs to PD are technology files which include the description of units, layer design rules, vias, drawing patterns, parasitic resistance and capacitance related to manufacturing process. Physical Libraries includes the description of complete layout information, abstract model for floor-planning, pin placement, design placement, routing strategies. Constraints file includes all design related constraints like Area, power, timing. The floor-planning is the first step in PD. This step includes core area estimation, die area estimation, estimation of placement of macro cells if any, input output pads placement, timing analysis along with congestion analysis should be done in this stage to avoid further violations. Placement of the standard cells plays an important role in all aspects of further violations, congestions. Thus for locating input and output always consider the surrounding environment within which the block or chip is interacting. Pin assignment is placed in accordance with interfacing of the particular module and pins. Power planning is an important step in PD. The power planning is to be properly planned so that the standard cells placed in the chip completely receives the given supply voltage. This becomes difficult with the shrinking technology and also due to the resistivity of the wire. Which leads to a local hotspot named IR drop. Next, to minimise clock skew and insertion delay clock tree synthesis is done and it is given to the standard cells. Finally, routing is done globally and detailed routing has been performed as illustrated in Figure 1.

2.1 IR Drop Analysis

Due to technology scaling and higher design frequencies, minimization of IR drop in the design is a challenging task. Through the metal layers, the power supply Vdd/Vss is distributed uniformly across the design. Actually the metal layers have a finite amount of resistance, due to which when a voltage is applied, there is a voltage drop (IR drop). As mentioned earlier, IR drop analysis plays vital role in determining the performance and reliability of the design. IR drop can be minimized by using Power/Ground network. When the technology has been scaling done, it reduces the width of interconnects but increases the resistance of the wire. By the increase in the resistance of the wire, there is an increase in the IR drop across the wire. As a result, the supplied voltage is not sufficiently delivered to all the logic cells in the design. This affects the speed that is nothing but performance of the circuit and also functionality of the same. Thus the IR drop is a serious and problematic concern in the industry. IR drop analysis is performed on the power supply networks to reduce the voltage drop. Due to the existence of non-ideal elements in the network, the IR drop may be static or dynamic. Average currents in the network contributes static voltage drop whereas dynamic voltage drop is due to the transient behavior of the current waveforms within clock cycles. A similar effect is found in ground wiring also which leads to ground bounce. Both static and dynamic effects contributes lower operating voltages within the devices, results in increase of overall time response of a device. The current spikes cause noise on wires, which in turn induce abrupt voltage changes on these wires and their neighboring wires, due to inductance coupling. This paper mainly deals with the static IR drop.

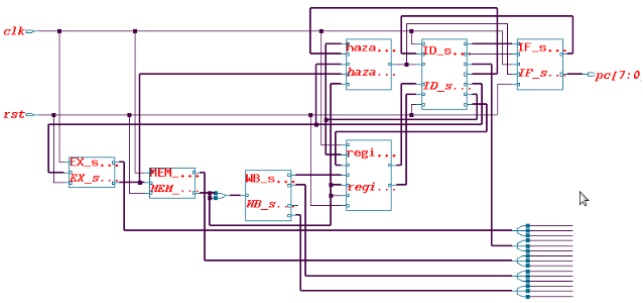

Figure 1. Schematic of MIPS design.

Since IR drop effectively reduces the supply voltage, it is important to understand the impact of IR drop on propagation delay of the design. Two small clock circuits presented in[2] are considered for simulation. The circuit consists of a five stage clock tree with 23 inverters interconnected using distributed RC network and is connected to the power grid. The clock circuit[2] is of H-tree configuration which evenly distributes the clock to all parts of a chip. The power grids are represented as dotted lines, each of which consists of a mesh of nearly 10000 nodes, 20200 resistors and 10000 capacitors, which are lumped to the ground. Two 1.8 v sources are connected to the nodes of power grid and create a variable IR drop.

Switching activity of the clock signal dynamically varies the IR drop at each buffer and leads to the variation in the output current[3] and hence the supply voltage. This effect, affects the delay, skew and slew rates which can be captured using detailed timing analysis. From the simulation, it is observed that 10% IR drop causes a increase of 10% in delay.

2.2 Power/Ground Padding

The power/ground padding is purely a grid structure and is a resistive model. Based on design density, IR drop is computed. The analysis of the model should include device parasitic capacitances, network capacitances, decoupling capacitors and the inductances[3]. Thus, power is one of the most important design criteria today. Deep sub-micron technologies enable high packing density on a small chip, but it leads to power density limits packaging, cooling and other supporting structures[4]. Power density also causes reliability issues. The source voltage coming from a corner of the chip should be delivered completely to the entire placed cells on the chip. This becomes difficult due the presence of resistivity of the connecting wire. This phenomenon leads to an IR drop on the chip.

To avoid this, mesh structure has been created known as power/ground padding[5]. The net list of MIPS design has been floor planned, the power planning is done secondly. In the power planning step creation of power distribution network is performed. An algorithm has been written for the placement of a particular module of the MIPS design.

2.3 Algorithm Placement of Particular Cells/Macros

- Floor Plan - site core_2400 -r 0.999121865548 0.699997 5.0 5.0 5.0 5.0
- Edit Pin - side Left –f ixed Pin 1 –fix Overlap 1 - layer 3 - spreadType start - spacing 0.2 - start 0.0 0.0 -pin {pin_names }
- Add Stripe - extend_to design_boundary block_ring_top_layer_limit ME5 - max_same_layer_jog_length 0.8 - padcore_ring_bottom_layer_limit ME3 - number_of_sets 7 -stacked_via_top_layer ME6 - padcore_ring_top_layer_limit ME5 - spacing 1 - xleft_offset 10 -xright_offset 10 - merge_stripes_value 0.1 - layer ME4 - block_ring_bottom_layer_limit ME3 -width 3 - nets {GND VCC} - stacked_via_bottom_layer ME1
- sroute - connect { block Pinpad Pinpad Ring core Pin } – layer Change Range {ME1 ME4} –block Pin Target {nearest Ring Stripe nearest Target } – pad Pin Port Connect { all Port one Geom } – check Aligned Secondary Pin 1 – block Pin use Lef – allow Jogging 1 –crossover Via Bottom Layer ME1 – allow Layer Change 1 – target Via Top Layer ME6 –crossover Via Top Layer ME6 – target Via Bottom Layer ME1 - nets {GND VCC}
- create Place Blockage - box 100 100 180 180 - ype soft
- set cell_list {cells/marcos}
- set lx 50
- set ly 50
- for each instplace $cell_list {
- set lx [expr $lx +2]
- echo “place Instance $ instplace $lx $ly -fixed” >> file }

This algorithm will help to place the standard cells and also to place the macro cells. Here in the proposed paper a module named EX-stage has been placed of MIPS design using the above algorithm. Similarly the structures in[7,8] can be taken for analysis for IR drop analysis.

3. Implementation Results

To illustrate and for a demonstration in the P/G Padding methodology, a MIPS RTL has been synthesized to a net-list Encounter® RTL Compiler. The net-list is thus imported in Cadence EDI in 90 nm technology. Figure 2 shows the floor plan of the design. The core and die area is 478 μm^2 and 469 μm^2 respectively. The cell utilization is 70%. Remaining 30% is utilized for routing in the design.

Figure 3 shows Pin assignment of MIPS design and the design has 10 internal pins. Amongst them two pin are the input pin and other eight pins are output pins. All the pins are placed on the left side of the die area and are placed on the metal layer 3.

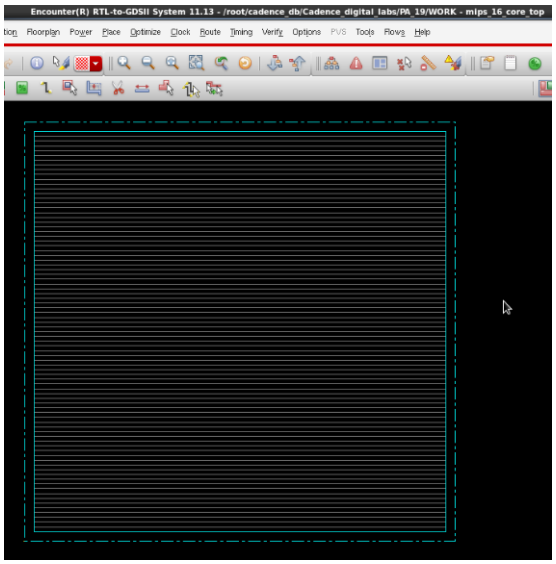

Figure 2. Floor plan of MIPS design.

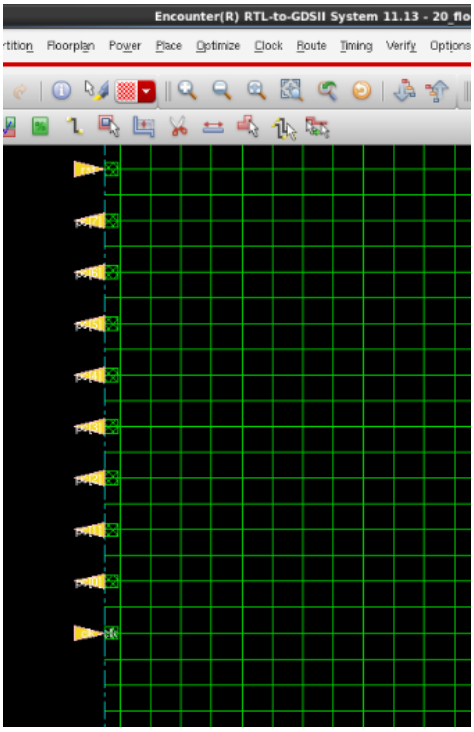

Figure 3. Floor plan of MIPS design with pins.

Figure 4 shows placement of soft blockages. The soft blockage specifies a region where only buffer can be placed. Which indicates standard cells cannot be placed in this region. In other words, it blocks the placement tool from placing non-buffer cells such as standard cell in this region. The dimensions in which the blockage is placed is 100 100 180 180.

Power planning is shown in Figure 5 the metal power stripes are added in MIPS design. The number sets of power stripes added are 5. Metal 4 has been used to trap the supply voltage. The width of the metal layer is 4 μm while the spacing between the power stripes is 1 μm. Two iterations are proposed in the paper for IR drop analysis.

The IR drop for Case 1 is shown in Figure 6. IR drop can be performed on legally placed cells. The histogram

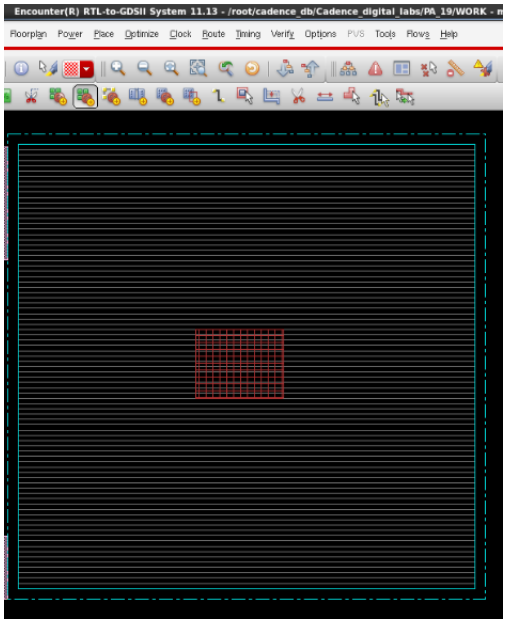

Figure 4. Addition of placement soft blockage.

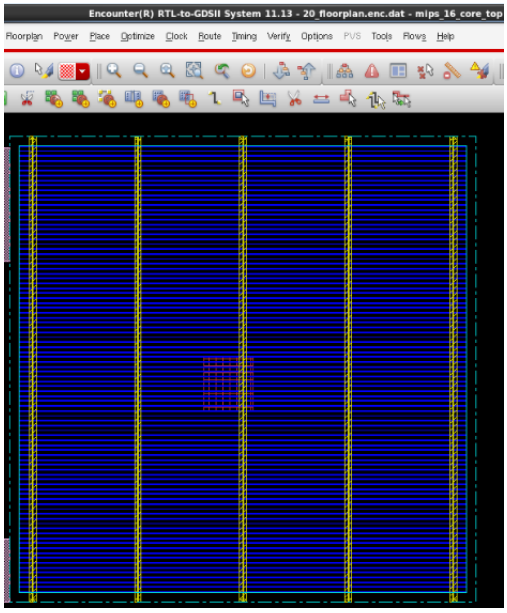

Figure 5. Power-planning of MIPS design.

representation is shown in Figure 7. 2317 standard cells are receiving 1.458 V, 670 standard cells are receiving 1.619 V and 141 standard cells are receiving 1.620 V which is the supplied voltage.

The power stripes are added in MIPS design. The number sets of power stripes added are 10. As mentioned earlier metal 4 has been used to trap the supply voltage. The width of the metal layer is 4 μm while the spacing between the power stripes is 1 μm. Figure 8 shows the addition of power strips.

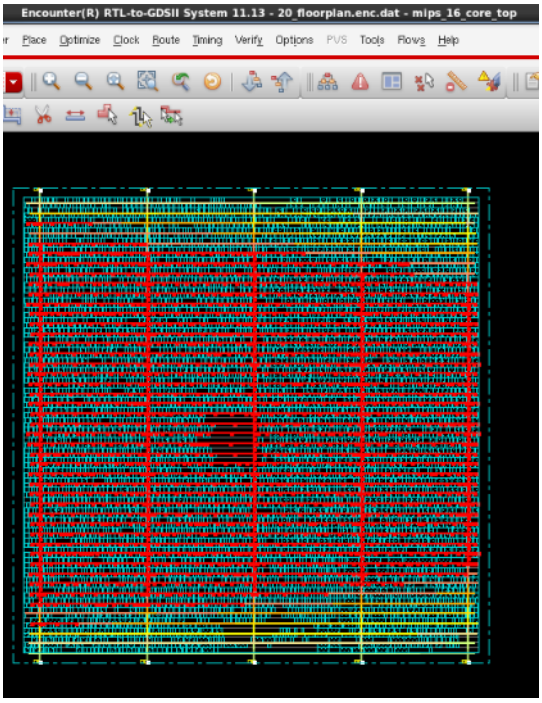

Figure 6. IR drop analysis for MIPS design.

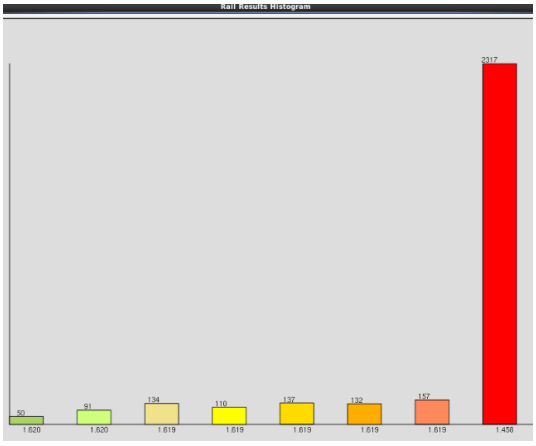

Figure 7. Histogram representation of IR drop analysis for MIPS design.

Figure 9 shows IR drop analysis for Case 2. The histogram representation is shown in Figure 10. Nearly 3597 standard cells are receiving 1.619 V, 946 standard cells are receiving 1.620 V which is the supplied voltage.

Using the algorithm the placement of EX-stage module gas been shown in Figure 11. The enlarged placed cells are also shown in the same Figure 12. The proposed algorithm plays an important role in special placement of the modules. The routing of the design is shown in Figure 13.

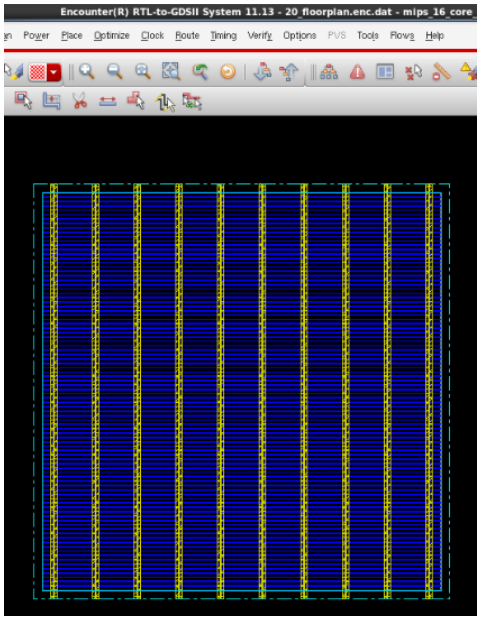

Figure 8. Power-planning of MIPS design.

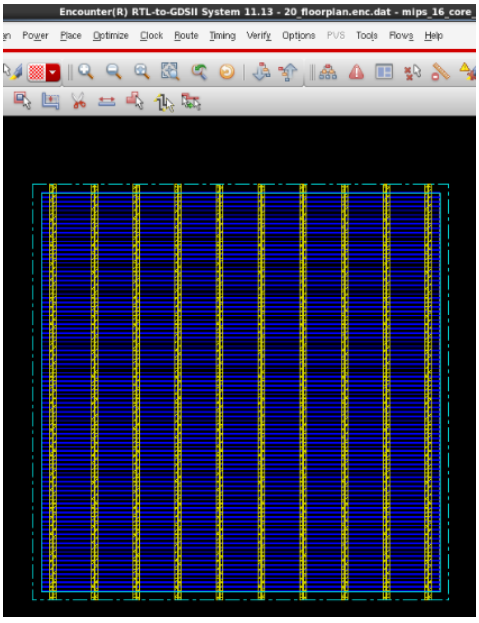

Figure 8. Power-planning of MIPS design.

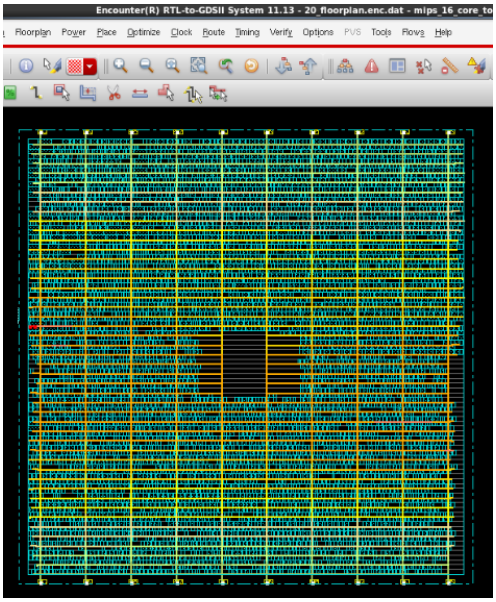

Figure 9. IR drop analysis for MIPS design.

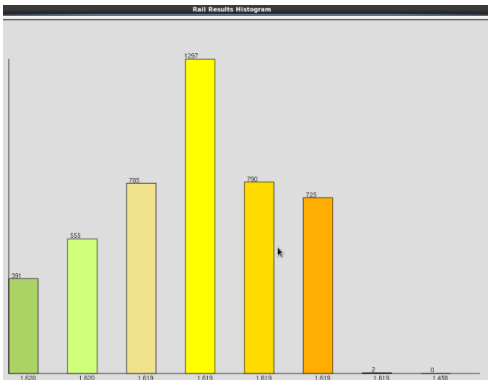

Figure 10. Histogram representation of IR drop analysis for MIPS design.

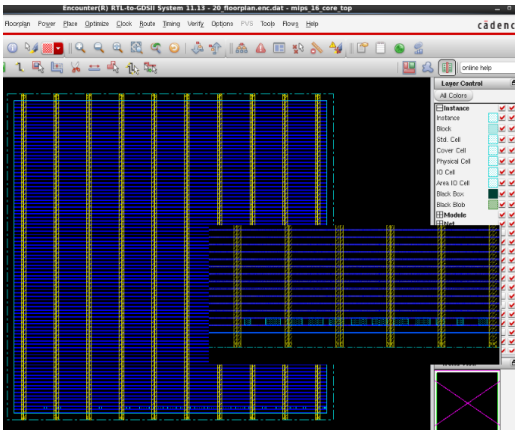

Figure 11. Placement of EX_stage module of MIPS design using algorithm.

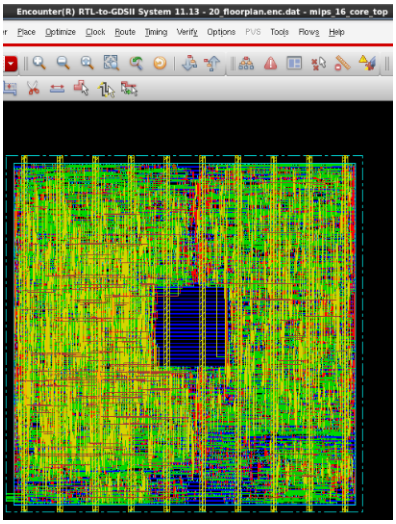

Figure 12. Routing of MIPS design using top metal layer 4.

Table 1. Slack timing of MIPS design at all stages of a PD

Case study	Pre-placement (ps)	Pre-CTS (ps)	Pre-Route (ps)	Post-route (ps)	Total power (mA)
Case:1	5.840	−1.623	−1.648	−1.879	11.87
Case:2	5.840	−1.663	−1.696	−1.908	11.63

The top layer is metal 6 and all the metal layers are utilized for routing. The global and detailed routing has been performed in Cadence EDI in 90 nm technology.

Timing reports for setup and hold mode has been reported as follows:

4. Conclusion

In this work, the RTL of MIPS has been synthesized in Cadenced RTL Compiler, the layout of MIPS design has been created in Cadence Encounter Digital Implementation EDI tool in 90 nm technology. The Power/Ground Padding Methodology has been created for trapping the supplied voltage. Thus two cases have been proposed for minimization of IR drop hot spots. Thus Figure 6 shows only 15% of the standard cells receives the supply voltage. Also Figure 6 shows that 98% of the placed standard cells receive the supply voltage. An algorithm for placement of EX-stage is proposed in the paper. The slack time in pre-placement stage is met while in the further steps of PD the slack time is not met. The reason behind this is

the CTS stage introduces buffers. Which in turn leads to insertion delay and clock skew routing all the modules also introduces interconnect delay as there is an increase in resistivity of the interconnecting wire. Thus Table 1 shows the Timing Analysis at each stage of PD.

The future work becomes more complicated as there can be a shrink in the technology. Thus meeting timing constraints becomes difficult as the technology shrink. After the sign off, extraction and verification of the design, it can be moved for base layer tape-out and later metal layer tape-out.

5. Acknowledgement

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