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Optimizing Power in Sequential Circuits by Reducing Leakage Current using Enhanced Multi Threshold CMOS

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Abstract

Technical thirst of man is in exponential rise and posing critical challenges in using this technology. This is much evident in the design of VLSI circuits. Sequential circuit designing demands lesser energy consumption, smartness and increased functional density. In this domain, every development in the recent past has energy as the focal point. MTCMOS exactly serves the purpose of reduced power consumption in digital circuits. This technique provides lower leakage current and offers enhanced speed. It uses low threshold voltage devices for low leakage and high threshold voltage components as sleep transistors. These sleep transistors are good enough to isolate the logic modules from the supply, ground in order to reduce the leakage current. Care is ensured particularly in the mode transition and also the least possible time for turn ON state in a circuit, as these are the primary concerns for power consumption and thereby for the performance degradation of integrated circuits. In this paper, a successful attempt was made in enhancing the advantage of employing MTCMOS technique towards lesser power consumption in sequential circuit designing.

Keywords: Leakage Current and Sequential Circuit, MTCMOS, Power or Energy Consumption

1. Introduction

In modern electronic devices, Power consumption is the bottleneck for system performance. Reducing power consumption has become an important issue, especially for high performance portable devices like Mobile phones, laptops, tablet PCs etc. Low power design can be exploited at various levels such as at system level, architecture level, circuit level, and component level.

There are various classifications for the reasons behind power consumption in a circuit. One popular way of classifying is as static and dynamic. Apart from this short circuit and leakage also plays a vital role in fixing the overall energy consumption in a circuit.

Static power is due to the number of logical components used in the design and dynamic occurs as a result of [4]number of transient states in the logic[14]. Short circuit currents also occur in this scenario, particularly when both NMOS and PMOS transistors are in ON state[6,7]. Capacitive action leads to dynamic energy consumption, which is most challenging issue to deal with as switching activity is high in sequential circuits. The expression for this dynamic energy consumption is given in the equation 1.

$$P_{dynamic} = C_{switched} V_{CC}^2 f_{clk} \qquad (1)$$

Here $C_{switched}$ is the cumulative switched capacitance. V_{CC} is the power supply, and f_{clk} refers to frequency of switching. Next significant contributing parameter for power consumption is the leakage power. It is becoming increasingly important and challenging as the demands for scaling the devices is ever increasing[7]. These currents can be classified into PN junction reverse bias current, hot carrier injection and sub-threshold current etc. Here, sub-threshold current is considered as the major contributing factor, so the expression for the sub-threshold current is given in the equation 2.

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$$I_{subth} = A \times e^{\frac{1}{nV_T}(V_G - V_S - V_{TH0} - \gamma' \times V_S + \eta \times V_{DS})} \times \left[1 - e^{\frac{-V_{DS}}{v_T}}\right] \quad (2)$$

Where

$$A = \mu_0 C'_{OX} \frac{W}{L_{eff}} (v_T)^2 e^{1.8} e^{\frac{-\Delta V_{TH}}{\eta v_T}} \quad (3)$$

VTH0 is the zero bias threshold voltage, vT = kT/q is the thermal voltage. The body effect for small values of source to bulk voltages is very nearly linear and is represented by the term g□ VS, where g□ is the linearized body effect coefficient. η is the DIBL coefficient, COX is the gate oxide capacitance, m0 is the zero bias mobility, and n is the sub threshold swing coefficient for the transistor.)VTH is a term introduced to account for transistor-to-transistor leakage variations.

The expression for the sub-threshold current can be modified into the simplest form by not considering the DIBL and the body effect factor. In addition to these assumptions, consider that $V_{ds} >> V_T$. The expression after these assumptions is reduced to:

$$I_{Subth} = \frac{A}{W_0} W_{10}^{\frac{V_{GS} - V_t}{S}}$$

Here an important observation is for every 100 mv decremented value in the threshold voltage; there will an increase in leakage current. S is the slope, whose value is $S = nV_T$[10].

Another inference is for the very less values of threshold voltage and supply voltage, these leakage power values are more intensely significant than dynamic energy consumption. The influence of this sub-threshold region and associated leakage currents will become predominant factors in the next generation innovations[3,11]

2. Impact of Technology Scaling

Scaling has become the rudimentary aspect for the evolution of technology in the recent past. Scaling also poses challenges to the technological performance parameters evaluation[5]. There are various scaling methods and constant field scaling is one prominent method. Here physical dimension such as width, length are scaled by a factor of 1/S, supply voltage and threshold voltages by a factor of 1/S and substrate doping by a factor of S. All other depended parameters such as delay, capacitance etc is scaled down by a factor of 1/S. The proportionate development in the frequency of operation is much clear with the proportionate improvement in the scaling technology[8]. As the operating frequency rises in general with scaling the switching power dissipation in this case also rises by $1/S^2$.

The scenario is different in the case of constant die size. This is because the energy consumption due to dynamic switching current is almost constant with scaling as the number of switching elements enhanced by a factor of S^2.

There is another observation that leakage currents generally get enhanced with reduced threshold voltages[9]. A typical interesting observation for a threshold voltage of 400 mv suggests that if the dynamic power consumption gets scaled by 1 then the leakage current gets enhanced by a factor of forty five.

But the impact of scaling on future technology is not good enough, due to increase of sub threshold leakage current. There is a high degree of demand for finding ways to contain the power consumption at reduced levels even under the conditions of improved leakage current and reduced threshold voltage due to scaling. The needed gain or performance from the design is possible only when these aspects are taken into consideration, while performing scaling.

3. Reduction Techniques

Many power reduction techniques have also been proposed from the system level down to the circuit level. In this paper, some of these techniques will be presented.

3.1 Dual V_T Methods for Sub threshold Leakage Control

Using high and low threshold voltages will be an influential solution to reduce the impact of sub-threshold leakage current[10]. This is in general known as dual threshold voltage technique. This diverse configuration allows both the advantages of speed and reduction in leakage current as a result of low and high threshold voltages respectively.

Suppose if S is of 100 milli volts per Decade and the shift in threshold voltage is of 300 milli volts then it also induces three times impact on the sub-threshold leakage current values. Here comes the exact usage of dual threshold voltage technique as it offers more than one advantage towards better performance of the circuits.

The usage of source biasing effect cannot be ignored for this application, but it is less effective when compared to dual threshold voltage method under the condition of increased scaling. The advantages offered by the later technique are many such as non leaky and very high speed components. The intended performance can be easily achieved with these techniques. All these reasons make this technique as the prime choice for the designers in the recent developments of CMOS technology. Using another threshold voltage also would not affect the overall cost of the design. Active and standby operational leakage currents can be effectively reduced by using this technique. These reasons make this technique as an attractive choice for the design engineers of sequential circuits for reducing the leakage current and to deal with many other energy consumption related challenges.

3.1.1 Dual V_t Gate Partitioning

The implementation of dual threshold voltage technique is simple. It divides the circuit into critical and non-critical sections. It makes use of lesser threshold voltage devices, where speed is the concern and similarly for energy consumption related areas, it uses higher threshold voltages. This is a wonderful approach of reducing the sub-threshold leakage currents in standby and also in the active mode of operation[12].

The common perspective is that high speed and lesser leakage are independent as threshold voltages vary in different directions. Suppose, in the case of speed as a concern i.e in the active mode, we make use of only lower threshold voltage devices although there is leakage current invariably. It is altogether a different need, when it comes to usage of high threshold voltage devices for peripheral circuits. In the case of intensely performance oriented designs of the circuit, the components cannot be operated at reduced speed, here there is a chance of achieving lesser leakage current reduction. Amidst of this scenario, implementing the dual threshold voltage logic is a challenge.

At first, a circuit to be partitioned, dual threshold voltage logic can be applied in stage-wise manner. Initially, all the components are given with lesser threshold voltage and later identify the non-critical regions or components and then rise them to higher values of threshold voltage. This surprisingly pushes into a situation, where now these non-critical regions become critical.

3.2 Multi-threshold CMOS (MTCMOS)

MTCMOS is very popular technique for the reduction of leakage current in standby condition[1]. This is achieved by employing higher threshold voltage transistor to isolate the logic from the supply or the ground, particularly in the inactive phase of the circuit operation.

The circuit shown in the Figure 1 is a good example of the implementation of this technique. Lesser threshold voltage transistors are used in the logic and higher threshold voltages towards supply and ground ensures lesser sub-threshold leakage. This is done through header and footer switches as shown in the Figure 1.

The reduced logic performance can be seen as in the active mode, the power interrupt switch is ON by SLEEP signal and current is drawn through this switch. This ensures that the reduction in the voltage drawn and thereby reducing the overall performance. There are various methods to encounter this effect. They are,

- Increase power supply
- Increased width of the power interrupt switch
- Increased area as well as power for sleep mode of operation
- Altering component implants towards achieving higher threshold voltage

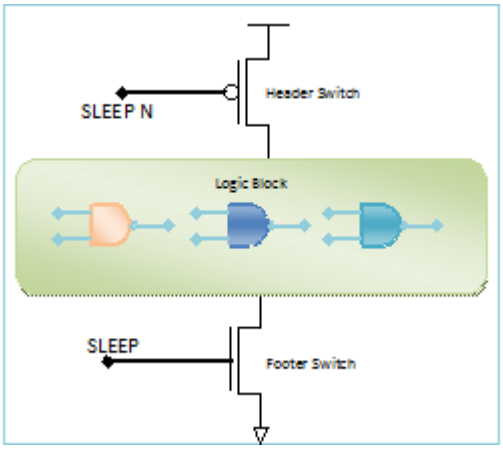

Figure 1. An example of an MTCMOS circuit.

In combinational logic blocks, MTCMOS techniques will effectively reduces the standby sub-threshold leakage currents. However, during the standby modes, these techniques cannot be applied to the sequential circuits because the high threshold power switches will disconnect the internal nodes from power supplies which cause them float.

This is not true in the case of single polarity component. Here the output nodes of the same gate will be generally driven to a differential rail, whereas the other nodes will be still in the float state. This scenario sometimes poses greater challenge in employing dual threshold voltage techniques for leakage current reduction. This is also because of the predetermined designs and in particular to sequential circuits with predefined conditions in the standby state data handling mechanism.

4. MTCMOS Sequential Circuits

Several MTCMOS sequential circuits that can preserve state during the standby mode has been discussed in this paper.

4.1 Conventional MTCMOS Latch

The Mutoh-Flip Flop is the conventional MTCMOS flip flop provides a low-leakage sleep mode where the data is maintained in the master latch shown in Figure 2. The best way to protect the state of the circuit is to make use of parallel high threshold voltage complementary metal oxide semiconductor inverters. This will ensure static recirculation path during the standby state[2,13].

During the active period, the operation of this latch is similar to conventional CMOS latch circuit. This latch works as transparent when a lower value of clock is encountered and behaves as opaque when higher clock signal appears. Whereas in the standby mode, the clock is low and higher threshold voltage inverters are used to hold the latch state. This occur even I_1 and I_3 are isolated from the supply power.

Distributed and localized header and footer sleep transistors are utilized in the master and slave latches to eliminate the sneak leakage current paths. Although the Mutoh-FF is capable of maintaining the data while lowering the leakage power consumption, the circuit suffers from high area and active power consumption overheads as compared to the standard single low V_t flip flop.

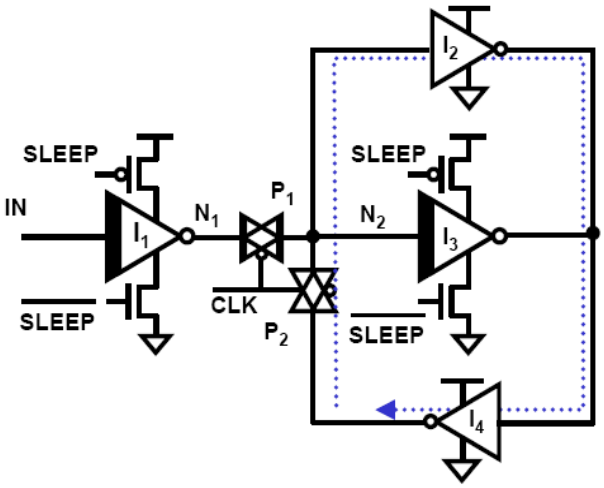

Figure 2. Conventional MTCMOS latch.

5. Enhanced MTCMOS LATCH

Figure 3 represents the Enhanced MTCMOS latch with P_1 pass gate is of low threshold voltage and P_2 pass gate is of high threshold voltage. This is different from the earlier discussed design in terms of selection of devices for distinct values of the threshold voltage. Higher threshold voltages are necessary for the reduction of leakage currents is the established fact. So, the inverters in the design I_2 and I_4 holds the latch state in standby mode of operation. Similarly, I_1 and I_3 are isolated then from the supply. The interface to the external connections is given by I_1besides acting as buffer to drive the latch input. This arrangement is crucial to avoid data feed through problem that occurs when no proper synchronization is met in giving input signals. Table 1 shows Comparison of MTCMOS_ LATCH AND EMTCMOS _LATCH using 180nm Technology.

Even though MTCMOS latch works like a conventional latch during the active mode, care should be taken in transistor sizing. This sizing is very crucial when a lower threshold voltage component is used in combination with the higher threshold voltage component. In this case larger leakage currents are possible. So sizing of the transistors should be effectively carried out in such a way

Table 1. Comparison of MTCMOS_ LATCH AND EMTCMOS _LATCH using 180nm Technology

Name of the circuit	Avg. power(Watts)	Delay	Power delay product(PDP)=avg. power*delay
MTCMOS_LATCH	45.74E-3	15.62	45.74E-3 *15.62
EMTCMOS_LATCH	146.6E-6	240.5E-3	146.6E-6*240.5E-3

that weak devices are protected and not contributing to the rise in leakage current.

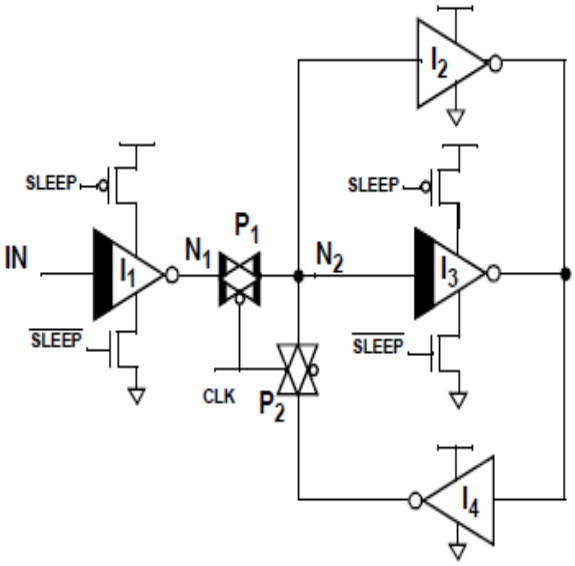

Figure 3. Enhanced MTCMOS Latch.

The operation of the above circuit in the transparent latch mode is as follows: Higher threshold voltage switches are ON, when the lower clock is appears. Better performance is achieved by making most crucial transitions to occur via lower threshold voltage components, namely, I_1, P_1, and I_3.

Next, P_2 is designed with higher threshold voltage components, so I_4 is isolated from I_1 for better performance of the latch. Suppose, if P_2 is chosen with lower threshold voltage components then it results in the slowing down of the data feed through associated delay value. This occurs because I_1 has to deal with the leakage of this gate till I_4 also get flipped in the period of switching transition.

During active state of the latch the following transitions occur:

- P_1 is turned OFF, whereas P_2 is in hold state
- N_1 and N_2 are pushed to opposite rails and gets isolated by P_1

This design also may end up in making N_1 and N_2 as contributors of leakage currents, if P_1 is not switched OFF properly. But leakage currents are far better than the conventional MTCMOS designs.

In other case, when N_1 and N_2 are in opposite rails, the role of P_1 becomes crucial to reduce the noise margin. This can be achieved by proper transistor sizing. This also arises as N_2 is driven through P_2 which has feeble threshold voltage (relatively).

This may not be a major issue if only lower threshold voltages are being used in the design. As in this particular case, enhanced OFF currents are balanced by enhanced ON currents. In the case of dual threshold voltage latch, care should be taken such that N_2 is at correct logic level. This can be done by properly sizing the higher threshold voltage P_2 and also I_4.

When it comes to the standby mode of operation, important aspect is the clock state. It should be high to keep the latch in the hold state. Higher threshold voltage components or transistors are to be in the OFF state to isolate the lower threshold voltage components or transistors from the supply power.

In the idle state, the recirculation path of I_2, I_4 and P_2 will be in active condition, which makes the latch to be in the hold state for this complete phase. Another point is this recirculation path can also be realized using higher threshold voltage components as it is not the prime reason for the switching and also it can be of lower speed.

Higher threshold voltage OFF component can be observed in the standby mode i.e in all the paths from supply to ground. As a result of isolation of I_2 from supply through these higher threshold voltage components, during the sleep state the excessive leakage encountered in the hold state can be avoided.

From this it can be inferred that usage of local sleep components of dual polarities is useful to eliminate or to reduce the sneak leakage. But this becomes very expensive. Unlike conventional MTCMOS circuits, MTCMOS in this design cannot hold higher threshold voltage sleep components, whereas here both the polarities are also required.

6. Conclusion

In combinational logic blocks, MTCMOS techniques will effectively reduces the standby sub-threshold leakage currents. However, during the standby modes, these techniques cannot be applied to the sequential circuits because the high threshold power switches will disconnect the internal nodes from power supplies which cause them float. In this paper we presented an enhanced MTCMOS latch that minimize the sneak leakage paths which draws high currents relative to a cutoff paths that flows from the power supply to ground through "ON" and "OFF" pass gates. By using local sleep devices of both polarities, all sneak leakage paths, can be eliminated in the sequential circuits. In this paper we compare the power and delay

values of MTCMOS latch and EMTCMOS latch using 180nm technology. The comparative analysis of this work at 180nm projected the pitfalls in the performance of the circuit with respect to technology scaling in terms of power consumption and delay.

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