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Low Power High Speed based Various Adder Architectures using SPST

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Abstract

Adder is a circuit that is combinational andcalculates the sum of three (full adder) or two (half adder) inputs. Full adder can be cascaded to produce n-stages of adder. This cascaded adder structure is called as parallel adder. The sum and carry outputs of any stage cannot be calculated until the input carry occurs, this leads to a delay in the addition process. In order to overcome the delay, carry look ahead adder is proposed which is said to be a fast adder. To improve the speed of vary look ahead adder, Spurious Power Suppression Technique (SPST) is used. This paper discusses 8-bit adder consisting of three architectures parallel adder, normal carry look ahead adder and SPST carry look ahead adder. The results were simulated using Xilinx tools and as shown, the power has decreased for both the SPST carry look ahead adder and the SPST ripple carry adder. The code was written in Verilog HDL and tested on a Xilinx FPGA test board as a part of a velocity measurement circuit for an Electromagnetic Projectile Launcher.

Keywords: Adder, Full Adder, Power, Parallel Adder, SPST

1. Introduction

Adders are an integral part of digital circuits, used almost everywhere from basic operations to complex digital signal processing applications. Adders can be constructed for any numerical base is it binary, decimal, hexadecimal or others. The most common form of adder is the ones that work with binary numbers. In places where one's or two's complement notation is used for negative numbers, it is very easy to modify the adder as a subtractor. Other signed number formats such as floating point, require extra hardware around the adder[1].

Adders can have multiple architectures, but basically they are of 2 kinds. Half adder adds two binary digits and gives output sum and carry. Full adder adds two numbers and also accounts for the value carried in as well as out. Architectures can be many types, the most widely used ones being carry look-ahead adder, Ripple carry adder and carry save adder.

The paper is organized as follows: The paper starts off with parallel adder, carry look ahead adder and then finally SPST carry look ahead adder[2]. Then the results for each circuit are compared and the advantages of SPST are shown.

2. Parallel Adder

We have taken a parallel adder with 4 inputs, so 4 full adders are used to generate the sum and carry for 4-bit adder. Architecture of parallel adder is as shown in Figure 1.

The Parallel adder works on the very basic principle of addition. Addition start from the LSB and proceeds to the MSB while gathering the carry. For the first stage, the carry in added with the LSB's of the two inputs and the sum is generated. The carry of this stage is given to the next bit and so on. Finally, we get a sum and a final carry output. This form of adder is also known as a ripple

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carry adder, as the carry travels as ripples from one stage to another.

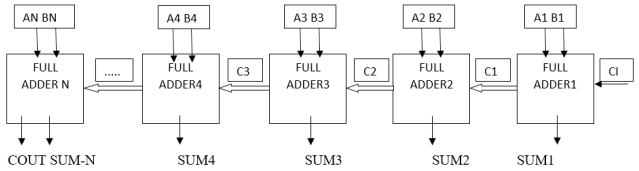

Figure 1. Parallel adder.

The Verilog code for the above architecture was written using structural modelling. The reports for the speed are and power was generated using Cadence and Xilinx tools.

3. Carry Look Ahead Adder

Carry look ahead adder is a fast adder in which operation of addition is speeded up. It generates two blocks for addition. Blocks are carry propagation and carry generation which has mathematical equations for manipulation.

Carry propagation $P_i = A_i$ xor B_i

Carry generation $G_i = A_i$ and B_i

To reduce computation time, two signals are generated for each bit position Propagate and Generate. They are generated based on whether the carry will be generated or propagated from that stage. Since P and G depend on the bits in that position, they can be generated independently and the adder doesn't have to wait for the previous stage. This reduces computation delay and makes the adder faster. The adder has full adders and a carry look ahead unit that computes the P and G values and makes the adder work.

The block diagram is shown in Figure 2.

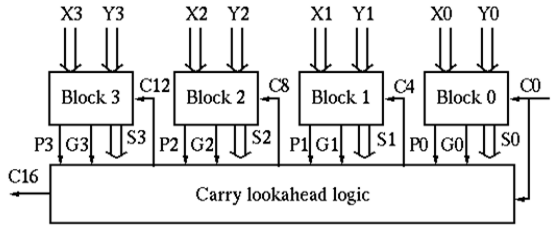

Figure 2. Carry look ahead adder.

4. Spurious Power

Spurious Transitions are unwanted transitions in a digital circuit that occur even though they are not expected and desired. They generally occur due to timing mismatches and unwanted redundant hardware in the circuit. These unwanted transitions are basically switching activity taking place in the circuit. As we know switching dissipates power and the power due to these transitions are known as Spurious power[3].

4.1 Spurious Power Suppression Technique

The SPST has a detection logic circuit find out if a transition in data bits of the result will occur in circuits, e.g., multipliers or adders. When a part of the data doesn't cause any change in the final result of the circuit, that portion of the data is latched to avoid unwanted transitions inside the processing units. Thereby the speed will be achieved[4,5]

4.2 SPST in Carry Look Ahead Adder

The architecture of SPST is shown using a low power design of an adder circuit[6]. The adder shown consists of two structures, one is the Most Significant Part (MSP) and the other is the Least Significant Part (LSP). The MSP is different from the original adder and is modified with the help of data controlling circuits, detection logic circuits, logic for finding carry both in and out beforehand and sign extension circuits. The LSP of the adder is implemented like in a normal adder. If a portion of the data does not affect any part of the final outcome, the data control circuit of the SPST stores (latches) this part to avoid unwanted transitions in the arithmetic unit data. The detection unit uses detection logic circuit to figure out the unwanted activity from the MSP bits of the input and the required carry output from the LSP stage of the modified adder. The circuit with detection logic gives close, carry_ctrl and sign outputs.

The block diagram for the SPST CLA is shown in Figure 3

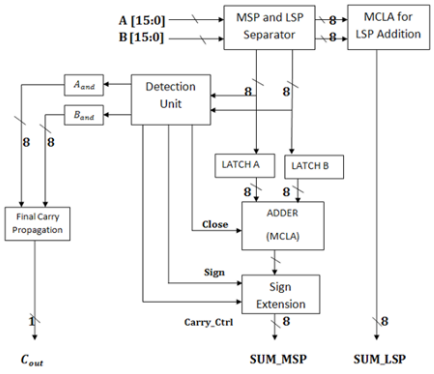

Figure 3. SPST CLA.

The block diagram of the detection unit is as shown in Figure 4

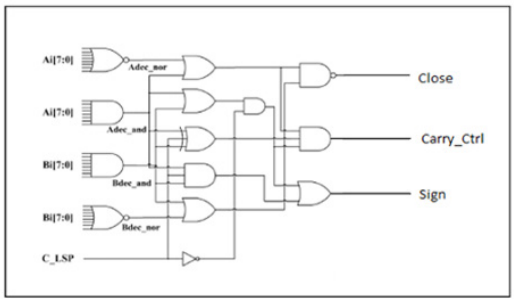

Figure 4. Block diagram of detection unit.

5. Results

The results obtained are shown in Table 1

6. Conclusion

In this paper, the proposed low power high speed VLSI Structure for Carry Look Ahead Adder with SPST is seen. The adder with SPST using AND gates tested hasvery high autonomy on changing the data assertion time. This helpsthe SPST circuit in being robust and helps it achieve up to 30% speed improvements. The proposed architecture was synthesized using Xilinx EDA tool with the logic family of Xilinx virtex 5. 8-bit adder architecture is synthesized and timing reports shows that SPST CLA adder is superior in the case of speed and power usage compared with parallel adder and normal carry look ahead adder.

7. References

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Table 1. Comparison various structures

Parameter	Carry look ahead adder	Ripple carry adder	SPST carry look ahead adder	SPST ripple carry adder
Power Leakage Dynamic Total	(nw) 546.013 11529.728 12075.741	(nw) 963.990 12283.870 13247.860	(nw) 313.683 9934.177 10247.860	(nw) 846.872 10001.307 10848.179
Area Cell Cell area	33 127	45 144	8 71	24 94
Timing (in – out)	696 (ps)	786 (ps)	648 (ps)	742 (ps)