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Design of Gain Enhanced and Power Efficient Op-Amp for ADC/DAC and Medical Applications

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Abstract

In this paper, low power low voltage Op-amp which forms the basic building block for various devices is designed by making the transistors of the Op-amp to operate in sub-threshold region. Now-a-days portable electronic devices are of great demand which thereby increases the demand for low power and low voltage design of devices. Conventionally, two stage op-amps are used which requires higher power with comparatively low gain. In order to overcome this, operation of devices in sub-threshold region is carried out which requires low power comparatively. Initially, the design of conventional Op-amp is designed using CADENCE Virtuoso tool GPDK 180nm with a supply voltage of 1.8V and the corresponding gain, phase margin, power of the conventional Op-amp is observed and then, Op-amp with transistors operating in sub threshold region is designed using CADENCE Virtuoso tool GPDK 180nm with a supply voltage of 1.8V and the corresponding gain, phase margin, power is observed. The comparison between these two observations are made and presented. These low power high gain devices are used in various applications like ADC/DAC devices and many medical applications.

Keywords: Op-amp, Phase Margin, Gain, Sub-Threshold Region

1. Introduction

Size of transistors are decreasing exponentially as predicted by Moore and thereby the size of devices is also decreasing correspondingly. However, power requirement for these devices still exists in the higher range. In order to overcome this difficulty many approaches were framed earlier.

In this paper, power requirement of the device is reduced by modifying the basic building structure of the devices. The operational amplifier (Op-amp) is a basic building block for many analog and mixed signal circuit designs like ADC, DAC, regulators, etc. As Op-amp forms the basic building block, its performance affects the overall performance of the system.

Here Op-amp is considered and modifications are made in them to reduce the power requirement of the devices. Conventional Op-amps have transistors which consume more power which thereby increases the power consumption of the devices which are using it.

2. Conventional Op-Amps

Op-amp are basically an amplifier, but can be differentiated from other amplifiers by its property that it can be able to use in the application of addition, subtraction, differentiation, integration. Op-amp has high forward open loop gain, thereby when they are applied in negative FB, so that close loop TF (Transfer Function) does not depend upon Op-amps forward path gain[1,2]. Mostly conventional Op-amps are made up of two stages[3], where first stage comprises of differential amplifier followed by common source amplifier.

It consists of two terminals, one is the inverting terminal and other is the non-inverting terminal. Input to the Op-amp is the differential signal and it is applied to the differential amplifier of the Op-amp, and output stage is the single ended output. Output will be equal to difference of signals applied at the input. In conventional op-amp, all the transistors present in them are operated in saturation region. In these transistors gate to source

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voltage should be greater than threshold voltage for the proper operation of the devices being considered. In addition to the transistors present in the op-amp, there will be a Miller capacitor which is added to increase the phase margin.

Conventional op-amp is initially designed by considering some initial specifications which is followed by certain calculations to come out with a desired design.

2.1 Specifications of Conventional Op-Amp

Initial specifications are as follows, and are given in Table 1.

Table 1. Specification of conventional op-amps

SPECIFICATIONS	VALUES
DC gain	60dB
Gain Bandwidth	30MHz
Phase Margin	60^0
Slew rate	20V/usec
ICMR(+)	1.6V
ICMR(-)	0.8V
C_L	2pF
P	<=300uW
V_{DD}	1.8V
Process	180nm
L_{min}	500nm

<Insert table 1. Here >

2.2 Formula Used

For the initial specifications, calculations are made using the following formulas as follows,

- As we are using cadence GPDK 180nm, we fix the initial length of the channel in transistor=500nm
- In order to avoid oscillations, fix the phase margin=60^0
- Miller capacitance is added to move the pole and increase the phase margin and its value is given by

  $C_C = 0.22 * C_L$
- Current through M5 can be found from slew rate by

  $I = \text{Slew rate} \times C_C$
- Design of transistors M1,M2 in Op-amp is done using the formula

  $(W/L)_{1,2} = (g_m)^2 * (\mu_n C_{ox} * I_5)$

  Where,

  Gain Bandwidth= $(g_m)/C_C$

  From this g_m=Gain Bandwidth * * C_C
- Design of transistors M3, M4 in Op-amp is done using the formula

  $(W/L)_{3,4} = (I_5)/ [(\mu_p C_{ox}) (V_{dd} - ICMR(+) - V_{t3(max)} - V_{t1(min)})]^2$
- where,
- $\mu_p C_{ox}$, V_t are calculated from cadence
- Design of transistor M5 :

  $(W/L)_5 = (I_5)/ [\mu_n C_{ox} (V_{ds5sat})^2]$

  where,

  $V_{DS5sat} = (ICMR-) - \sqrt{(I_5 (\mu_n C_{ox} (W/L)_1]} - V_{t1max}$
- Design of transistor M6:

  $(W/L)_6 = [(g_{m6})/ (gm_4)](W/L)_4$

  where,

  $g_{m6} > g_{m1} * 10$
- Design of M7:

  $(W/L)_7 = (I_7/I_5) (W/L)_5$

2.3 Device Specifications

For the above specifications, using the above formulas, device parameters are made and tabulated as follows, and are given in Table 2.

Table 2. Device specification of conventional op-amps

DEVICE	W/L Ratio	W/L
M1	6	3u/.5u
M2	6	3u/.5u
M3	14	7u/.5u
M4	14	7u/0.5u
M5	12	6u/0.5u
M6	174	87u/.5u
M7	75	37.5u/.5u
M8	12	6u/.5u

2.4 Schematic of Conventional Op-Amp

Using the above device parameters, schematic of conventional op-amp is drawn using CADENCE Virtuoso tool GPDK 180nm with a supply voltage of 1.8V as shown in Figure 1.

2.5 Region of Operation of Devices

In cadence, region of operation of device in region 2 refers to operation of transistor in saturation. In the conventional op-amp above, all op-amps operate in region 2, which thereby implies that transistors present in the conventional op-amp operate in saturation region.

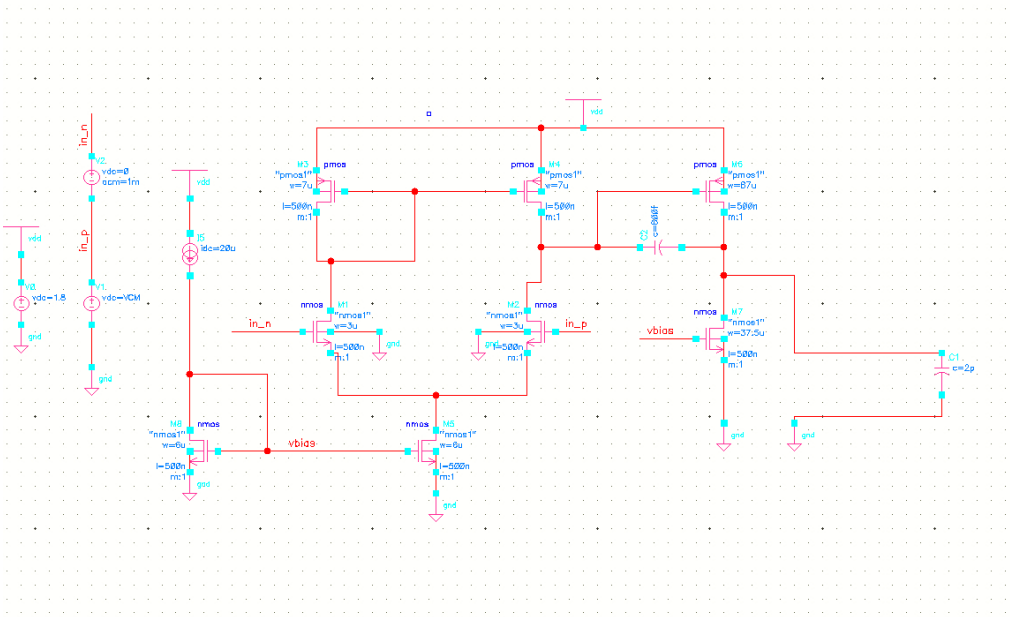

Figure 1. Schematic of conventional op-amp.

2.6 Magnitude and Phase Response

For the conventional op-amp designed using the above specifications, magnitude and phase response are obtained as follows and are shown in Figure 2.

Gain obtained for this conventional op-amp is 58.45^0.

2.7 Power Observation

For the conventional op-amp designed using the above specifications, power dissipation is obtained as follows and are shown in Figure 3.

As it was stated earlier gain, phase margin, power of conventional op-amp are obtained using cadence virtuoso and it does approximately met the desired specifications.

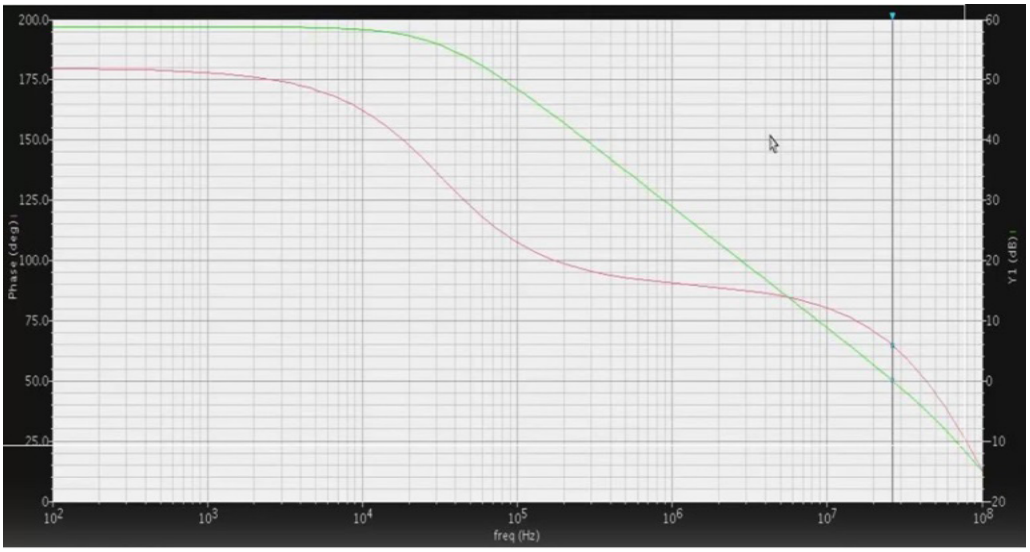

Figure 2. Magnitude and phase response conventional op-amp.

Figure 3. Power observation for conventional op-amp.

3. Proposed Subthreshold Operation of Op-Amp

We would have already learnt that the transistors would be operating in the cutoff or linear or saturation region. However, during the operation of transistors in the cutoff region, we will be considering that there would be no drain current, but there will be a negligible current present in the cutoff region. These negligible current was considered as a leakage current, but we would not have considered them as they are negligible[4,5].

Now, the size of transistors has scaled down, and thereby these leakages current comes into account[6]. As the current flow consideration is below the threshold voltage of transistors, this region of operation of device is called subthreshold operating region of transistors[7]. The current which is flowing in this region is called subthreshold current.

As far as conventional op-amp is considered, in which transistors are operating in saturation region, power requirement would be very high when compared to the op-amp in which transistors would be operating in subthreshold region. This reduction in power occurs because voltage requirement for the device to operate in sub-threshold region is low. So thereby operation of devices in subthreshold region would drastically decrease the power of the devices[8].

In Figure 4, the graph is drawn between V_{gs} and $\log I_d$. From the graph, it could be noted that below threshold voltage drain current increases exponentially with gate to source voltage, while above threshold voltage drains current increases linearly with gate to source voltage[9,10].

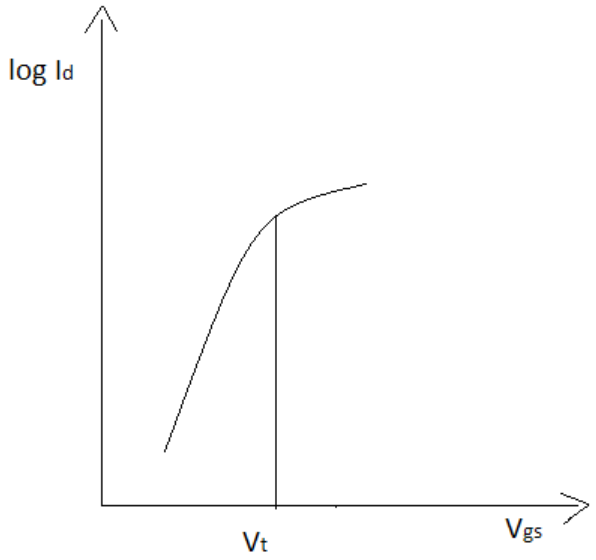

Figure 4. V_{gs} Vs Logi_d transistor in sub-threshold region.

In order to make the transistors to operate in subthreshold region, following specifications has to be met and are given in Table 3.

Table 3. Specifications for transistors in sub-threshold region

SPECIFICATIONS	VALUES
Gain	70dB
Gain Bandwidth	25KHz
Phase Margin	60
Slew Rate	2V/us

3.1 Formula Used

To meet the above specifications, following formula along with the earlier formula are used,

- 1) $I_D=(W/L)I_O e^{(Vgs-vth/mVt)} (1-e^{-Vds/Vt})$
  Which can be approximated as
  $I_D=(W/L)\ I_O e^{(Vgs-vth/mVt)}$
- $(W/L)M_{1,2}=(I_{D1,2}/I_O)e^{(Vth-Vgs/mVt)}$
  where,
  $I_{D1,2}=4q(m1,2Vt)^2/Svw$

3.2 Device Specification

From the above formulas, specifications are met by making the device specifications as follows and is given in Table 4.

Table 4. Device specification for transistors in sub-threshold region

DEVICE	W/L ratio	W/L
M1	80u	160u/2u
M2	80u	160u/2u
M3	250	100u/0.4u
M4	250	100u/0.4u
M5	50	50u/1u
M6	9.708	100u/10.3u
M7	5.6	5.6u/1u

3.3 Schematic of Op-Amp in Subthreshold Region

With the above device parameters, op-amp is drawn using CADENCE Virtuoso tool GPDK 180nm and the various observations are made as shown in Figure 5.

3.4 Region of Operation of Transistors in Op-Amp

In cadence, region of operation of device in region 3 refers to operation of transistor in subthreshold region. In this op-amp one can note that all transistors operate in region 3, which thereby implies that transistors present in this op-amp operate in sub-threshold region.

3.5 Magnitude and Phase Response

For the above op-amp designed using the above specifications, magnitude and phase response are obtained as follows as shown in Figure 6.

3.6 Power of Op-Amp in Subthreshold Region

For the above op-amp designed using the above specifications, power obtained is as follows as shown in Figure 7.

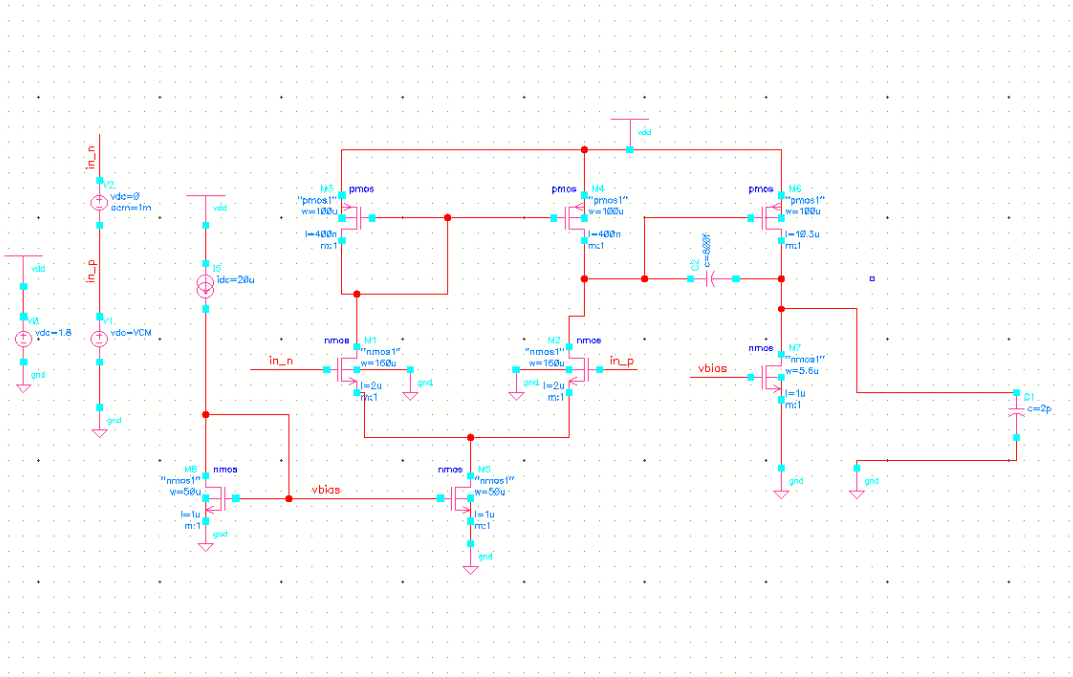

Figure 5. Schematic of op-amp in subthreshold region.

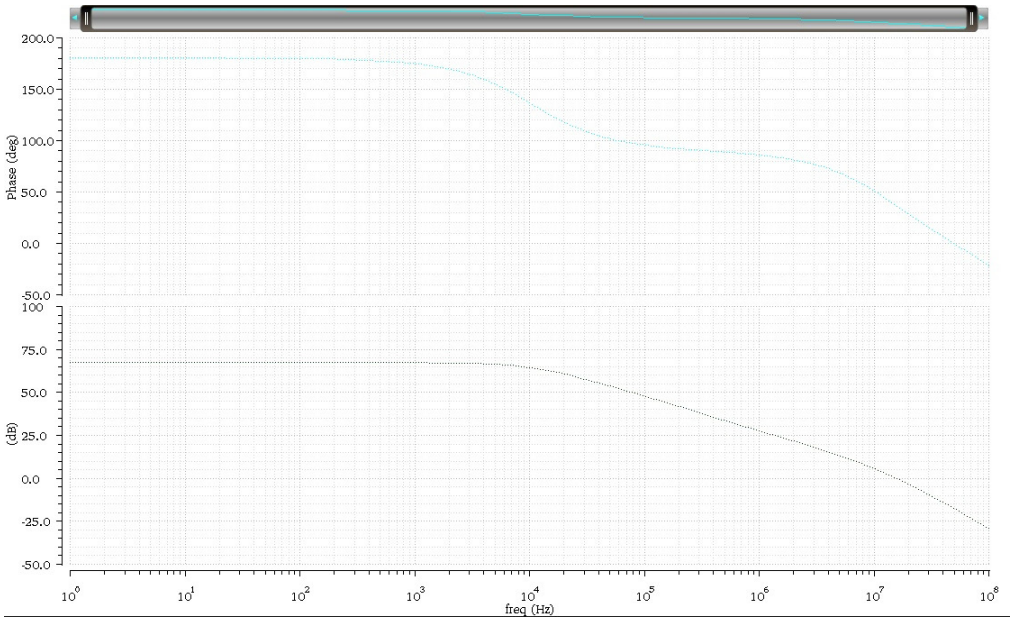

Figure 6. Magnitude and phase response.

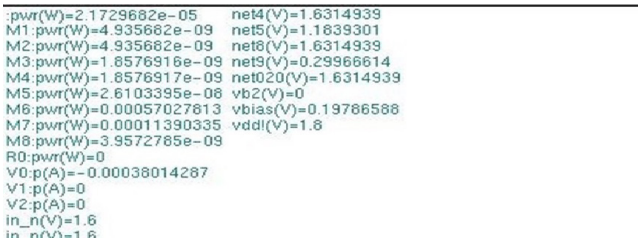

Figure 7. Power of op-amp in subthreshold region.

4. Comparison between Conventional Op-Amp and Proposed Op-Amp

Comparisons between conventional and proposed op-amps are made and their differences are stated here. Power requirement for the proposed op-amp has decreased several times when compared to conventional op-amp and their corresponding gain also increased by operating the device in the sub-threshold region and are given in Table 5.

Table 5. Comparison between conventional op-amp and proposed op-amp

PARAMETERS	CONVENTIONAL OP-AMP	PROPOSED OP-AMP
POWER	209 uW	21.7uW
GAIN	58.45^0	68.45^0

5. Conclusion

Conventional op-amp is designed using CADENCE Virtuoso tool GPDK 180nm with a supply voltage of 1.8V. Their corresponding power, gain, phase response are observed and compared with op-amp which operates in subthreshold region, from which one can observe that power has drastically reduced and their corresponding gain has been increased and this forms the basic application for many low power medical applications and other low power devices.

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