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Digital Infinite Impulse Response Filter with Floating Point Multiply Accumulate Circuit using Pipelining

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Abstract

A competent architecture for IIR filter is designed. It is configured and folded, which will be used in the real time applications like loud speaker and equalization of digital signal processing. A basic feature of digital signal processing is filtering. Filtering is a choosy system which passes an assured choice of frequency and attenuating the others frequency. Digital filtering is a prevailing sector of DSP allied works. A system of digital filter performs mathematical operations on a sampled or discrete time variant signal to contract or improve certain aspects of that signal. The configurable folded IIR filter for sixth order is designed using three series of second order IIR filter. This IIR filter architecture is used to carry out three second order or a one sixth order. It can be also used to execute one fourth order and one second order in parallel according to the requirement where, each second order IIR filter is designed using multiply accumulate circuit which as floating point. Here pipelining of IIR filter for second order is proposed to increase the throughput by reducing the critical path delay. The proposed sixth order IIR filter using three second order IIR filter with pipelining achieves 39.7% of increased throughput and it operates at high frequency of 85.068MHz compared with conventional MAC based architecture.

Keywords: IIR Filter, Multiply Accumulate Circuit (MAC), Pipeline

1. Introduction

In digital signal processing the filter circuits are widely used for many applications. The main purpose of this filter is to remove undesirable part of the signal, that is floating point series. IIR filter has been more effectual compare to FIR filter due to feedback system.

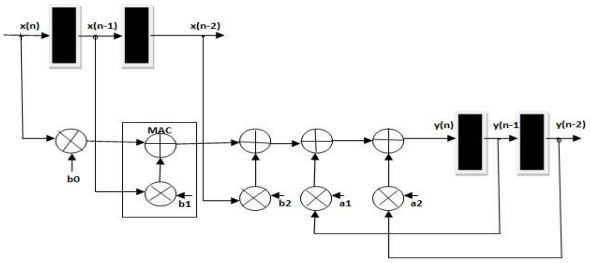

Figure 1. Design of IIR filter for second order.

The digital Infinite Impulse Response (IIR) filter[1] represented as Figure 1. Here input and output signal sequences are x(n) and y(n). IIR filter design for second order is detailed in [2]. The operation of multimode filtering is described in [3], here the cascaded second order FIR filter is applied to change the filter order depending on the constraint. Multiplier next to accumulator is used to design each second order FIR filter. The performance of the circuit is measured by using the parameters like Critical path delay, Power and Area. By providing appropriate optimization in these parameters, the performance of the circuit will be increased. The configurable design of IIR filter for sixth order is designed using three series of IIR filter which is second order, where each IIR filter for second order is designed by Multiply-Accumulate-unit (MAC)[4] which is floating point. Arithmetic and multiplier concept are detailed in [5,6]. The use of this filter is to execute single sixth order or three second order. It can also be used to perform one fourth order and one second order in parallel. This architecture for filter gives improved performance compared with existing design.

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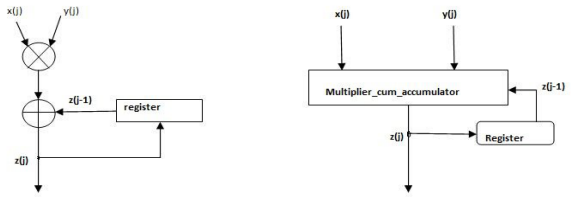
2. IIR Filter Design

IIR filter design uses a floating point as values. This filter design integrates two things. First thing is the design of IIR filter for second order using modified multiply-accumulate-circuit, here addition is performed using present multiplication so the depth of modified multiply-accumulate-circuit is reduced compared with conventional MAC design. Figure 2(a) shown is the design of usual multiply-accumulate-circuit.



(a) (b)

Figure 2. Multiply- accumulate- circuit (a) usual b) modified.

Here separate adder is used for adding the result of present multiplication with previous MAC result and this adder for addition is avoided in modified multiply-accumulate-circuit. Figure 2(b) shows the modified MAC circuit and it is called as multiplier-cum-accumulator. The Second thing is IIR filter performs the multimode operation it follows the series of second order IIR filter.

3. Multiply-Accumulate-Circuit (MAC)

Multiplier cum accumulator using floating point contains the sections of Mantissa alignment, Normalization and Multiplication-cum-accumulation. In floating point multiply-cum-accumulation operation the [As, Ae, A] is first input operand likewise [Bs, Be, B] is second input operand and the [Ps, Pe,P] is denoted as result of prior MAC. Here, As, Bs, Ps are denoted as sign bits respectively Ae, Be, Pe denoted as exponent bits and A, B, P are the normalized mantissas. The operation performed based on the select line when sel=0 then complete design is used to perform multiplication operation which is floating point. If sel=1 it performs MAC operation. The two nbit input numbers are multiplied and resulting value will be 2n or 2n-1 bit large. The multiplication result of most significant bit is Ri[msb] and the result of least significant bit is Ri [lsb]. n the same way most significant bit and least significant bit of preceding MAC result will be Ri-1 [msb] and Ri-1 [lsb]. In floating point MAC Operation Ri [msb] and Ri [lsb] will be aligned. Floating point MAC design is detailed in [7]. Where the mantissas are Ri, Ri-1, here the least significant bit is 0 and most significant bit is 47 or 46. In modified floating point multiply-accumulate-circuit the partial invention of current multiplication is added with the mantissa of preceding MAC result. The most significant bit of mantissa of preceding MAC result is align with result of msb bit of the current multiplication which is not attained. So the mantissa of P and B are single place shifted right ({0,P}, {0,B}) the corresponding exponent value will not change and the prevision of most significant bit of multiplication result is avoided. In following step, the result of unbiased exponent value of preceding MAC is related with the sum of balanced exponent. When (Ae + Be) > Pe, by using barrel shifter the mantissa of P is shifted right upto (Ae + Be) – Pe time using rounding process. Similarly, if (Ae + Be) is less than Pe, mantissa of A is shifted right upto Pe – (Ae + Be). Hence pe will be equal to (Ae + Be). The msb of current multiplication product of aligned A x B is equal to msb of P. Here three more bits for rounding process are (Guard bit (G), Sticky bit (S) and Round off bit (R)) are used right to the most significant bit of the mantissa. Then Wallace tree multiplier is used for multiplication of A and B, where the partial products values are added with P. After that, Normalization is processed in last step of floating point MAC.

4. IIR Filter Design Using Modified MAC

Design of IIR Filter for modified second order is shown in Figure 3.

Here the filter coefficients are bo, b1, b2 and a1, a2. Here y(n) denoted as output. x(n) is denoted as input signal sample value. The multiplexer used to select the filter coefficients and value of inputs, outputs for every clock cycle. Equation of IIR filter for second order is shown in (1)

$$Y(n) = a1\, y(n-1) + a2\, y(n-2) + bo\, x(n) + b1\, x(n-1) + b2\, x(n-2) \quad (1)$$

Design of IIR filter for configurable sixth order is shown in Figure 4. Here three 2-quad IIR filters are cascaded to achieve the IIR filter operations of three second

order or one sixth order. It can also be used to perform one fourth order and single second order. Figure 4 shows the mode of operation in IIR filter is performed by using the select line of the multiplexer. The IIR filter for sixth order is denoted as Y (n) = a1 y (n-1) + a2 y (n-2) + a3 y (n-3) + a4 y (n-4) + a5 y (n-5) + a6 y (n-6) + b0 x (n) + b1 x (n-1) + b2 x (n-2) + b3 x (n-3) + b4 x (n-4) + b5 x (n-5) + b6 x (n-6). Here the expressions a1 y (n-1), a2 y (n-2), b0 x(n), b1 x(n-1), b2 x(n-2) are establish by 2-quad F1. The terms a3y(n-3), a4y(n-4), b3y(n-3) and b4y(n-4) will find by 2-quad F2. In the same way a5y (n-5), a6y (n-6), b5y (n-5) and b6y (n-6) be taken from two quad F3. For IIR filter of sixth order , y(3) = a1y(2) + a2y(1) + a3y(0) + b0x(3) + b1x(2) + b2x(1) + b3x(0) .At clock cycle 2,5 and 10 the terms y(2) , y(1) and y(0) be established from 2-quad F1.then at the clock cycle 11,12 and13,14 ,15 the expressions b0x(3) ,b0x(3) +b1x(2) ,b0x(3) +b1x(2) +b2x(1) +a1y(2) +a2y(1) are establish from 2-quad F1.In parallel at clock cycle 11 and 12. 2-quad F2 contain the terms b3x(0) and b3x(0) +a3y(0).By making se22 = 6 the value of b3x(0) +a3y(0) is maintained in 2-quad F2 at clock cycle 13,14 and 15.

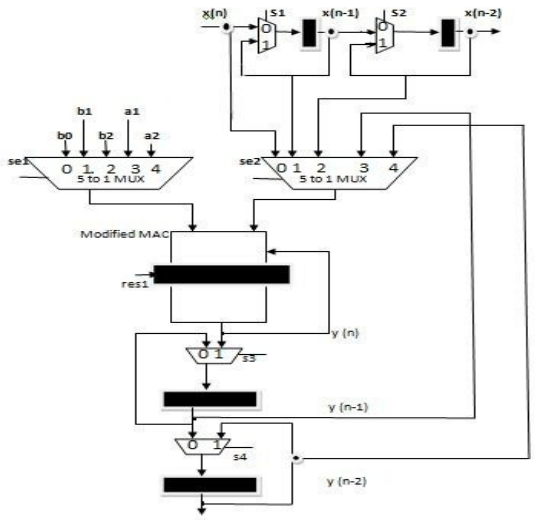


Figure 3. Design of IIR filter for modified second order.

Figure 5 shows the 2-quad IIR filter for sixth order design. se2=5 and se22=5, s7=1 the expressions from 2-quad F1 b0x(3)+b1x(2)+b2x(1)+a1y(2)+a2y(1) is add with b3x(0)+a3y(0).Now 2-quad F2 produce a result of y(3) at clock cycle 16.likewise all the output values are get from IIR filter for sixth order.

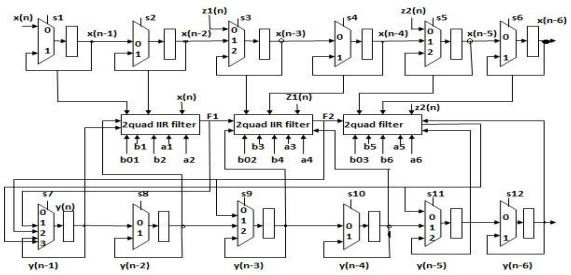
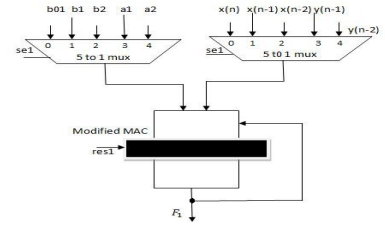
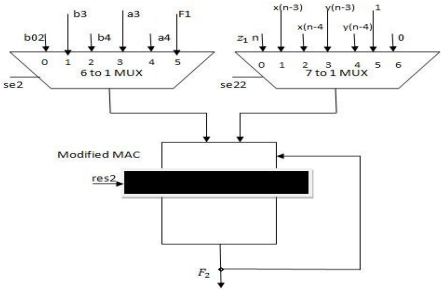


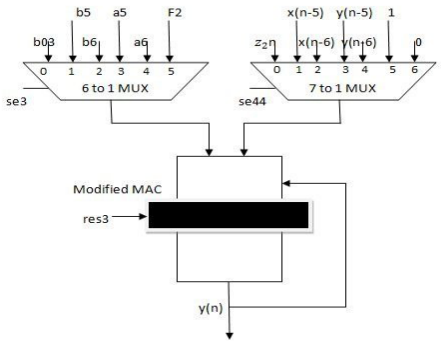
Figure 4. Design of IIR filter for configurable sixth order.



(a)



(b)



(c)

Figure 5. 2-quad IIR filter for sixth order design (a) 2-quad IIR filter (F1), (b) 2-quad IIR filter (F2), (c) 2-quad IIR filter (F3).

5. Pipelining

Pipelining concept in IIR filter is used to reduce the critical path in to small stages by adding register along the path, it may increase the sample speed or reduce the power consumption. Here eight tap second order IIR filter is pipelined so eight stages are used for pipelining to achieve the smaller critical path delay. Result of this will increase the operating frequency so the throughput of the filter is increased. Pipelining method for critical path reduction, it can be oppressed to either increase the sample speed or to reduce power consumption.

6. Results and Discussion

Configurable IIR filter for sixth order designed by three series of IIR filter, which is second order. Here pipelining is used to design IIR filter for second order. This method is used to reduce the critical path by placing latches along the critical path. So the total critical path delay is reduced and it achieves the high throughput. Simulation results shows the output of IIR filter for second order and fourth order as well as sixth order. Here Figure 6 shows the result of second order IIR filter without pipelining. Similarly, Figure 7 shows the result of second order IIR filter with pipelining and result of fourth order IIR filter is shown in Figure 8. Figure 9 shows the result of sixth order IIR filter**.** Table 1 gives the details about throughput and frequency value for proposed work.

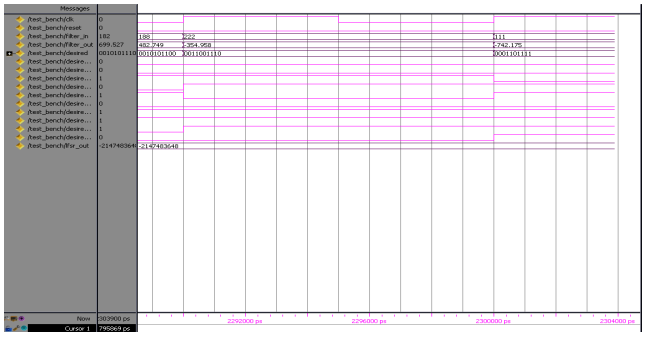


Figure 6. Result of second order IIR filter without pipelining.

Table 1. Tabulation of proposed work

Throughput	Timing (Max Frequency)
205 MBps (without pipelining)	63.037MHz
340.2MBps (with pipelining)	85.068MHz

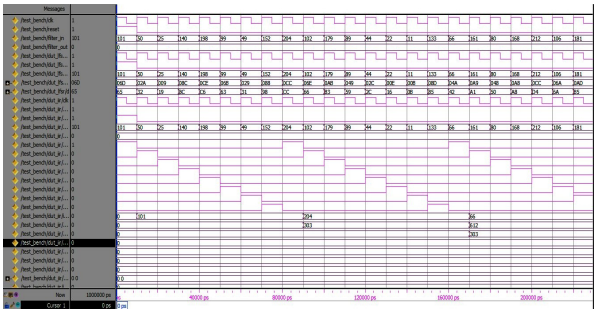


Figure 7. Result of second order IIR filter with pipelining.

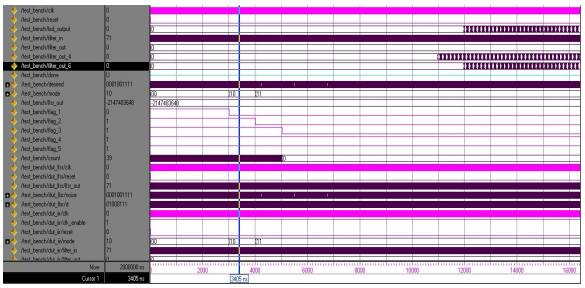


Figure 8. IIR filter for fourth order.

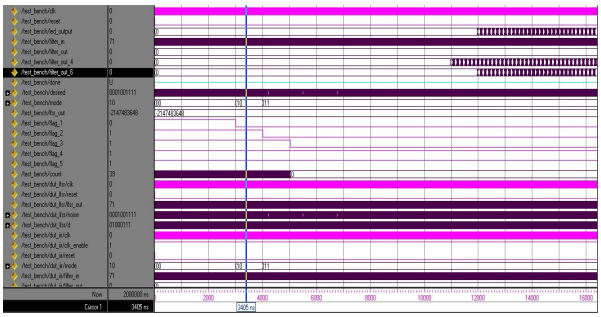


Figure 9. IIR filter for sixth order.

6. Conclusion

This paper proposes a pipelining concept in configurable folded IIR filter design to achieve high throughput. The design of IIR filter for sixth order with pipelining is used to carry out three second order or a one sixth order. It can also perform one fourth order and single second order in parallel. The proposed configurable design of IIR filter for second order using pipelining achieves high throughput of 205 MBps by reducing the critical path delay.

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