A New Approach for Low Power Decoder for Memory Array

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Abstract

SRAMs are important building blocks in many digital applications, such as microprocessors and cache memories. Decoders are the significant components in SRAMs. Address decoder is vital part of SRAM memory. Choice of capacity cell and read operation is relies on upon decoder. Henceforth, execution of SRAM is relies on upon these parts. This work studies the location decoder for SRAM memory, focusing on deferral streamlining and control effective circuit systems. We have focused on ideal decoder structure with slightest number of transistors to diminish range of SRAM. Usually, in Memory Chip, it consumes almost fifty percent of the total chip access time and power. Parameters which has to be considered while designing an address decoders are, first appropriate circuit technique has to be chosen and the second thing is sizing constrains of the transistors. Modified hybrid type of decoding topology is illustrated and it is compared with traditional type decoders which include both static and dynamic types using 180 nm CMOS technology in Cadence Virtuoso environment.

Keywords: Buffer Control, Cadence and Power Consumption, SRAM, Static Decoder

1. Introduction

SRAM modules are frequently employed as a cache which has high performance and usually employed to enhance the performance of the processor[1]. And in computer systems, it is used as registers. In the recent trends, processor speed has increased drastically[2], to subsist off the high-speed processor[3] i.e. need to provide instructions and data in high clock rates. Subsequently in VLSI technology the performance of functional gates has increased, but memory access time or speed is not enhanced because of high memory densities. Therefore for high computing machines or processors, memory elements are important to improve the performance. And can be used in microprocessor also. In this work, the design of low power and high-speed Decoders are implemented which can be used in high-speed memory computing systems.

Address decoders are the important module in all memory blocks which respond to very high frequency[3].

Chip access time and power consumption of the Address decoder directly influences on SRAM memory circuits.

Two types of decoders can be employed in SRAM Memories which are the Column decoder which passes the data into bit lines further into SRAM cells and Row decoder which enable the word line by the address input. Due to large densities of storage elements in memory arrays, the various types of address decoders can be implemented resulting in performance improvement and reduction in power consumption[4]. Design of dynamic and static decoders are complex and in high memory densities elements, the design of static and dynamic decoder are complex hence, there is a high possibility of sensing wrong elements. Traditional static Address decoder gives precise result but it built with a large number of transistors which results in large amount of delay[5].

In this work, Static CMOS type decoder with additional buffer control stage is presented which has optimal performance in power consumption.

2. Decoding Architecture

Considering Decoder performance, chip access time and power consumption are largely determined.SRAM cell is activated by row decoders having n to 2^n outputs. The general memory array Row decoder can be multi or single stage architecture. In multiple stages decoding, it uses several linked blocks[6]. Generally, MSB is pre-decoded in the first stage that triggers the relevant word line. Similarly in last decoding stage, number of outputs corresponds to a number of word lines. Yet, memory architecture used nowadays is based on dividing the whole module into several decoding stages. This type of method is proven to be faster for large memory arrays and also having less power consumption.

2.1 Traditional Decoder

Basic AND Logic gate conventional decoder is illustrated in Figure 1. The problem with these types are in CMOS Technology AND gate cannot be directly derived and when fan-in more than 4, it slows down decoding. Hence it occupies more area to decode the function. Since the area is increasing delay and power also increases drastically.

Hence, these type of decoders is realized using NAND, NOR, NOT gates only.

2.2 Universal Block Decoding Schemes

NAND gate produces Logic low outputs when both inputs are high and for other combinations, it gives high output. Similarly, NOR gate produces a high logic output when the inputs are low and produces high logic for other combination.
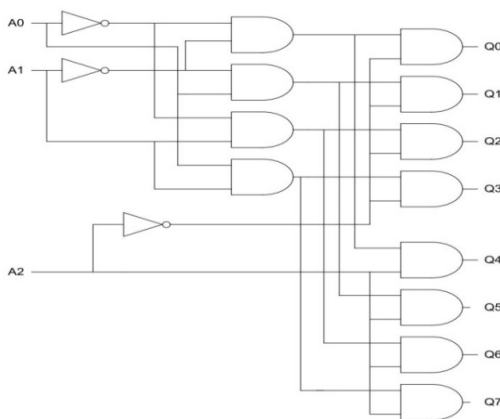
Gate with distinctive output is needed to design an address decoder. Using inverters, input logic can be varied and by using NAND and NOR gates we can get the unique combination of logics. By utilizing all these CMOS gates we can design address decoders, by using only NAND gates and inverter circuits and by using the combination of NAND–NOR circuit[4].

NAND gate produces distinctive low output for all high input, (2:4 NAND type Decoder is shown in Figure 2). [3]NOR produces distinctive high output for all high input, (2:4 NOR type Decoder is shown in Figure 3).

Using this criterion, design scheme is presented by using the combination of NOR and NAND gates. [7]NOR gates are used in thelast stage to provide high output and NAND gates are used in initial stages. The combination of these NAND-NOR stages gives the total number of stages
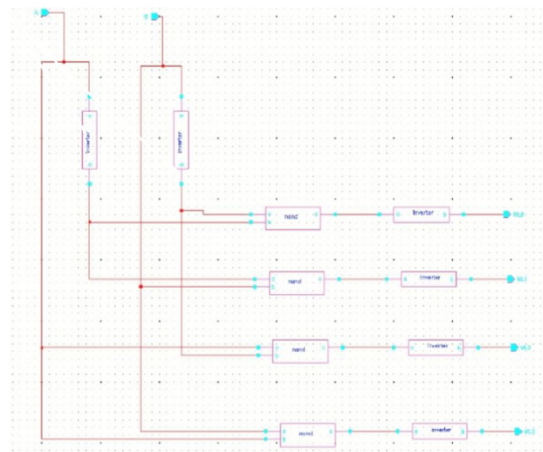

Figure 2. 2:4 NAND type decoder.

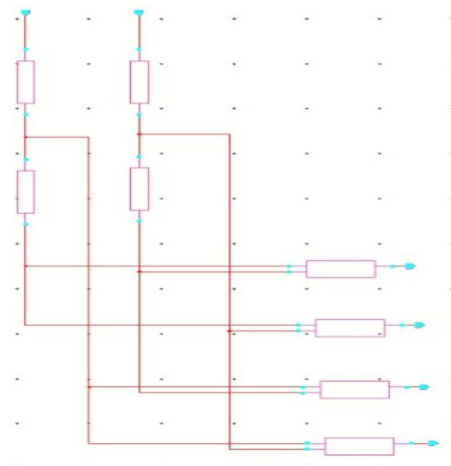

Figure 1. Traditional AND type decoders.

Figure 3. 2:4 NOR type decoder.

of the decoder. The initial stage can be designed either by NOR gate or NAND gate. NAND gates are used for an odd number of stages. Nor gates are used for even number of stages. Both architectures is shown in Figure 4 (NAND LOGIC) and Figure 5 (NAND–NOR Logic) respectively.

The only problem in this block type architecture is area wise it is not fully optimized i.e. transistor count will be high so does the power. Since there are many logic functional blocks there will be different path delays at the final output stage[3]. In this case, Least Significant Bits need to pass on every input and output pins in every stage whereas Most Significance Bits will operate only in final stage hence, there will be more glitches due to different delay path.

Consider an example where the address is 00000, the decoder output for line 15 (for some time) and 0 becomes high. This is due to different delay path at the final output stage. Hence, there will be false cell due to this unwanted

power will be dissipated. To eliminate the number of stages and to control the delay in path new decoding architecture is presented.

2.3 Proposed Hybrid type Decoder Technique

The proposed hybrid type is made using three components namely buffer control circuit as shown in Figure 6, pre-decoders, NAND-NOR stages based gates. Here pre-decoding circuit is used to minimize the transistor count, also, it reduces total input and output stages. By reducing these parameters power optimization can be achieved at a higher rate. The pre-decoding technique is made by 4 bits, 8 bits, 16 bits, 32 bits so on. In this hybrid approach, pre-decoding technique reduced 1 stage.

Proposed 5:32 hybrid decoder is illustrated on Figure 7. To get distinct output NOR and NAND based stages were
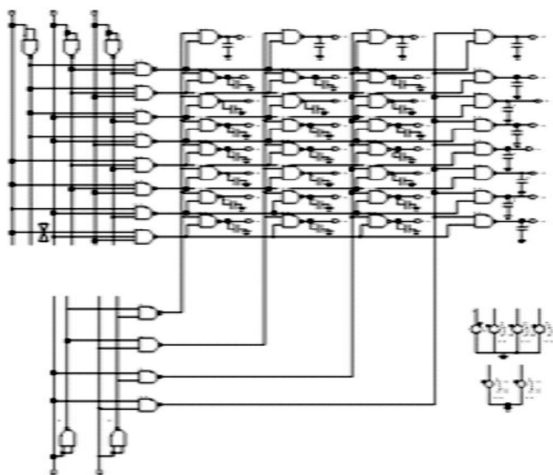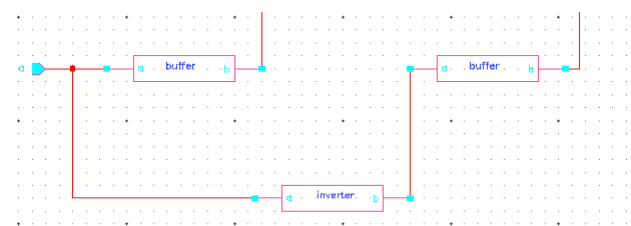

Figure 6. Buffer control circuit.

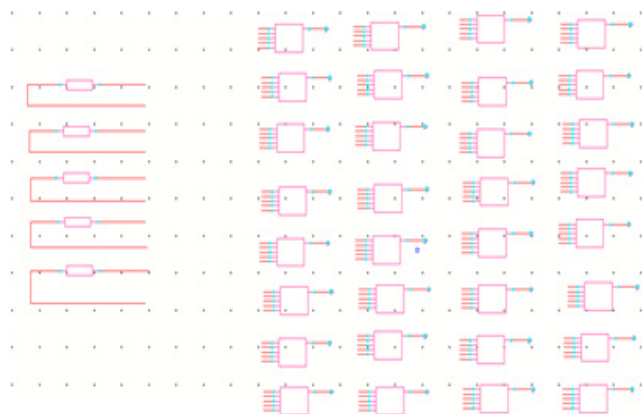**Figure 4.** 5:32 NAND based logic.
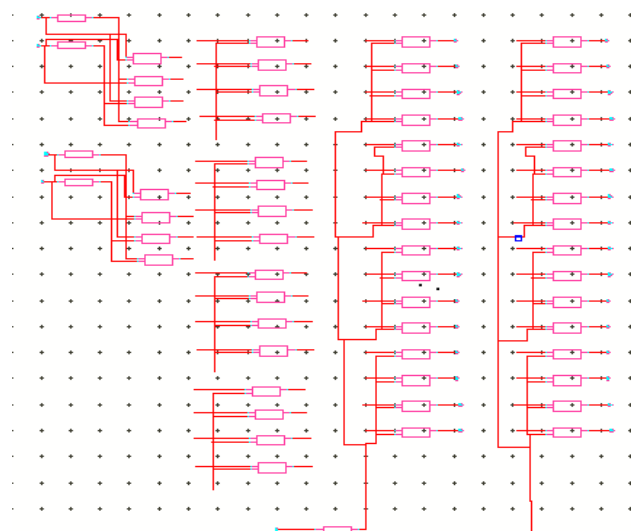

Figure 5. 5:32 NAND-NOR based logic.

Figure 7. Proposed 5:32 static decoder.

used. By using pre-decoding technique, here the count of gates are reduced when compared to the traditional type of decoding technique which uses NAND–NOR stages to implement the function. And consider delay also reduced when compared with traditional decoding scheme. Buffer control, clock skew or path delay is reduced by using buffer control circuit (Figure 7). It gives equal delay at all significant bits i.e. most significant and least significant. Hence, this buffer control circuit is made for all functional logic change.

The initial stage of the decoder is pre-decoding stage, which can be implemented using NAND or NOR gate scheme. In this case, NOR type scheme is used to get distant high output, the second stage is NAND type scheme which gives distant low outputs. Buffer control is employed at the final stage of the decoder, these reduces the different path delay in the whole circuit. These three combinational stages form the efficient decoding architecture.

3. Simulation Results

The various models are designed and implemented in cadence virtuoso environment using GPDK 180 nm library technology files. The resultant waveform for proposed decoder is illustrated in Figure 8.

The comparison is made between traditional decoding schemes and proposed scheme for 5:32 decoder. Table 1 clearly shows that power consumption of proposed decoder is considerably less when compared with traditional blocks.

The various results were tabulated, which shows that performance of the proposed decoder is efficient.
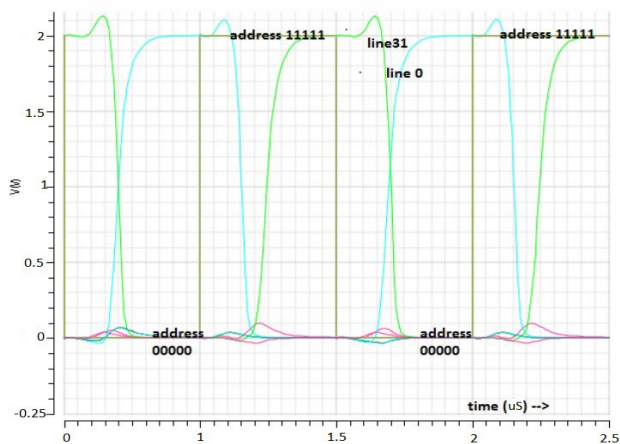

Figure 8. Waveform for proposed 5:32 decoder.

Table 1. Comparison between traditional schemes and proposed

TYPE	POWER	NO. OF TRANSISTORS
Traditional Static NAND	16 mW	370
Traditional Static NAND-NOR	12.6 mW	330
Proposed Static using Buffer Control	9 mW	238

4. Conclusion

Static type decoder is designed, which is capable of implementing 2^5 bit pattern. The proposed decoder is operated with 1.8 v, supply and consumes around 9 mW. Whereas traditional NAND-NOR, NAND implemented logic consumed 12.6 mW and 16 mW respectively.

Hence, it clearly shows that proposed decoding technique is 28.5% (when compared to NAND–OR) and 43% (when compared to NAND based logic) power efficient than the traditional blocks.

5. Reference

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