

Design and Implementation of Adders using Novel Reversible Gates in Quantum Cellular Automata

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Abstract

Background/Objectives: The objective is to reduce the Quantum Cost (QC), Garbage Output (GO) and Gate Counts in the design of the adder by incorporating the Novel Reversible Gates. **Methods/Statistical Analysis:** In recent day's energy dissipation is the major complex problem in circuit designing in order to recede this problem the reversible logic is employed, where the input vectors can be derived from the output vectors and from the output vectors the input vectors can be procured. Using this technique the Quantum Cost, Garbage Outputs and Gate Counts of the design is reduced. **Findings:** Based on the technique of reversible logic a novel reversible Gates is proposed from that the novel reversible adders have been designed. The novel reversible gates satisfy the property of reversibility and universality which shows the uniqueness of the proposed gates. The comparative analysis have been made with the existing work, the proposed work shows a significant improvement in the design optimization parameters. **Application/Improvements:** The proposed structures can be employed in the ALU design and in Floating Point Multiplier design. The comparative analysis shows that Number of Gates, Garbage Outputs and Quantum Cost is minimum for the proposed gate based structure rather than conventional one

Keywords: Garbage Outputs (GO), QCA, Quantum Cost (QC), Reversibility, Reversible Logic, Universality.

1. Introduction

The irreversible circuits which emits a tremendous amount of heat and results in an enormous emission of energy during computation. This contribution of heat and energy must be reduced in a huge amount. Hence in order to further proceed on this way reversible logic technique is used. The reversible logic circuits can also be named as the charge recovery circuits. Reversible logic has an ability to reduce power dissipation and its does not lose information during its information bit processing and it generates unique outputs. The gate is considered to be reversible if and only if every input has unique output vectors and input vectors can be derived from the output vectors. Researchers like Landauer computed

that each irreversible the heat generated will be in the order of KT , the power dissipation is mainly due to the erasure of the intermediate states that are been used in the computation process. When one bit of data gets erased means the energy dissipation will be in terms of $KT \ln 2$, where K is the Boltzmann's constant and T is the absolute temperature¹. Bennett proposes the concept of reversibility, thermodynamically the reversible computers can dissipate less amount of heat that is less than KT of energy per logical step and capable of producing useful computations at useful speed². Further the conservative logic is also employed to reduce the power dissipation³. Quantum cellular automata are the philosophical model of quantum computation, it should be made universal for quantum computation and QCA computation will be

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reversible.

2. Basics of Reversible Logic

The parameters that are considered for computing reversible logic is Quantum Cost, Garbage Outputs, Gate Counts.

2.1 Quantum Cost (QC)

Each reversible circuit has a cost associated with it called as the quantum cost it is defined to be the number of 1x1 and 2x2 primitive gates used in the quantum circuitry.

2.2 Garbage Outputs (GO)

Garbage outputs are defined to be the number of outputs left unused during the quantum computation.

2.3 Gate Counts

The number of gate used to compute the certain circuitry in quantum implementation.

3. Proposed Reversible Structure

This paper solicits the new reversible gate called Reversible Gate 1, Reversible Gate 2 and Reversible Gate 3 as shown in Figures 1, 2 and 3. The significant aspect of this gate is that it satisfies the property of Reversibility and Universality. The novel Reversible half adder, half subtractor, full adder, full subtractor and ripple carry adder is designed using this novel Reversible Gates.



Figure 1. Proposed Reversible Gate 1.

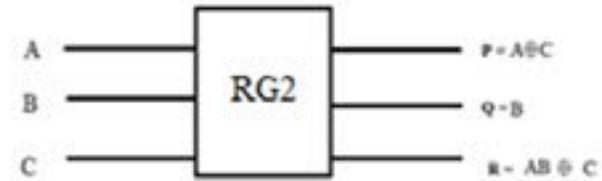


Figure 2. Proposed Reversible Gate 2

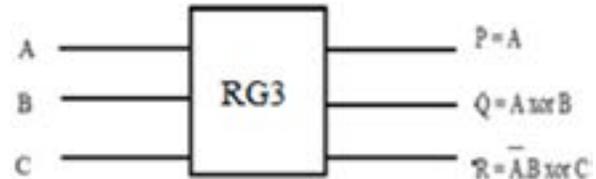


Figure 3. Proposed Reversible Gate 3..

This proposed reversible structure which serves as the basics of computing adders and subtractors. This structure serves as a better gate compared to the other existing gate proposed in the references.

4. Reversibility and Universality

Reversibility represents the one to one mapping between the input and the output bit vectors. As the permutation side of view the input vectors can be represented by 1-cycle or 2-cycles⁴. 1-cycle refers to the bits unchanged in their position in the permutation and 2-cycles refer to the elements swapping their places in its output bit vectors.

Table 1. Reversibility for RG1

A	B	C	P	Q	R	Permutation
0	0	0	0	0	1	2 - cycle
0	0	1	0	0	0	2 - cycle
0	1	0	0	1	1	2 - cycle
0	1	1	0	1	0	2 - cycle
1	0	0	1	1	1	4 - cycle
1	0	1	1	1	0	4 - cycle
1	1	0	1	0	0	4 - cycle
1	1	1	1	0	1	4 - cycle

The Reversible Gate1 satisfies the property of Reversibility in executing that the permutation of output bit vectors have two 2 cycles and four 4 cycles combination as mentioned in Table 1.

The Reversible Gate 2 satisfies the property of Reversibility

in executing that the permutation of output bit vectors have two 1 cycles and six 6 cycles combination.

Table 2. Reversibility for RG2

A	B	C	P	Q	R	Permutation
0	0	0	0	0	0	1 - cycle
0	0	1	1	0	1	2 - cycle
0	1	0	0	1	1	2 - cycle
0	1	1	1	1	0	2 - cycle
1	0	0	1	0	0	1 - cycle
1	0	1	0	0	1	2 - cycle
1	1	0	1	1	1	2 - cycle
1	1	1	0	1	0	2 - cycle

As only 1 cycle and 2 cycles are employed here the reversibility can be easily verified in Table 2.

The Reversible Gate 3 satisfies the property of Reversibility in executing that the permutation of output bit vector have two 1 cycles and six 2 cycles combination as indicated in Table 3. As only 1 cycle and 2 cycles are employed here the reversibility can be easily satisfied.

Table 3. Reversibility for RG3

A	B	C	P	Q	R	Permutation
0	0	0	0	0	0	1 - cycle
0	0	1	0	0	1	2 - cycle
0	1	0	0	1	1	2 - cycle
0	1	1	0	1	0	2 - cycle
1	0	0	1	1	0	1 - cycle
1	0	1	1	1	1	2 - cycle
1	1	0	1	0	0	2 - cycle
1	1	1	1	0	1	2 - cycle

Universality of the gate which refers to the gate utilization in order to compute AND, OR and NOT operations. If the reversible structures use to realize these following functions then it is said to satisfy the universality property. In addition to reversibility, reversible logic gates must provide universality properties, so that they can be used to design any desired logic. Hence, only a subset of the permutation gates is useful as reversible logic gates in practice because some of them do not possess universality properties. For universality the triad of and, or, and not bit operations on 2-bit inputs forms the well-known necessary and sufficient operations to realize arbitrary computation⁴. The proposed reversible structure satisfies

the property of reversibility and universality.

Table 4. NAND realization of RG1

A	B	P	Q	R
0	0	0	0	1
0	1	0	1	1
1	0	1	1	1
1	1	1	0	0

The NAND gate realization of RG1 shown in Table 4 is achieved when the value of c is equal to zero hence $R = \text{NAND}(A,B)$ when c value is equal to one the AND realization can be done.

Table 5. NOT gate realization in RG1

A	B	C	P	Q	R
0	1	0	0	1	1
0	1	1	0	1	0

The NOT gate realization of RG1 shown in Table 5 is achieved by taking any combinations of input. It can be made by $R = \text{NOT}(C)$.

Table 6. NOT realization of RG2

A	B	C	P	Q	R
0	1	0	0	1	1
0	1	1	0	1	0

The NOT gate realization of RG2 shown in Table 6 is achieved by taking any combinations of input. It can be made by $R = \text{NOT}(C)$.

Table 7. NOR realization of RG3

A	B	P	Q	R
0	0	0	0	0
0	1	0	1	1
1	0	1	1	0
1	0	1	0	0

The NOR realization of RG3 shown in Table 7 can be achieved by taking the C value as the control input and setting it as 1.

Table 8. NOT realization of RG3

A	B	C	P	Q	R
0	1	0	0	1	1
0	1	1	0	1	0

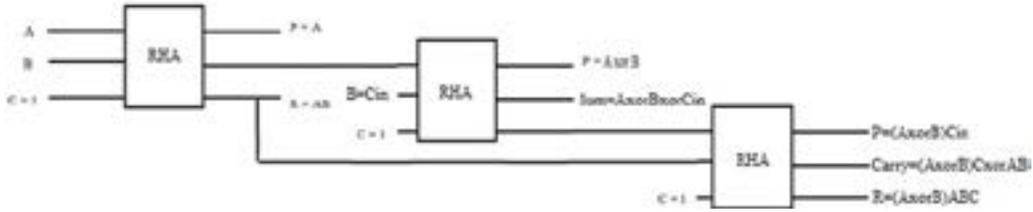


Figure 5. Novel full adder.

The NOT gate realization of RG3, shown in Table 8 is achieved by taking any combinations of input. It can be made by $R = \text{NOT}(C)$. Thus from the above representation we concluded that the proposed reversible gates which satisfies the property of universality and reversibility.

5. Design of Adders

From the novel reversible gates the design of adder is enumerated. The representation depicts the half adder; full adder and ripple carry adder design using the proposed novel reversible gates. The proposed gates are also used to perform the reversible multiplier operation⁵ and the reversible subtraction operation⁶.

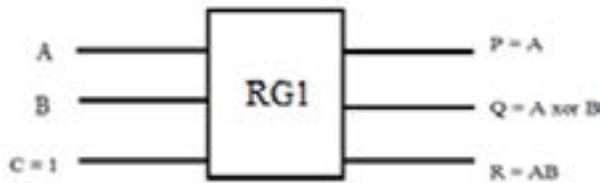


Figure 4. Novel half adder..

The Figure 4 shows the design of novel reversible half adder. The number gates required for this design is 1 and the number of constant inputs used here is 1.

The Figure 5 shows the novel reversible full adder. The number of constant inputs required for this design is 3 and the number of gates used in this design is 3.

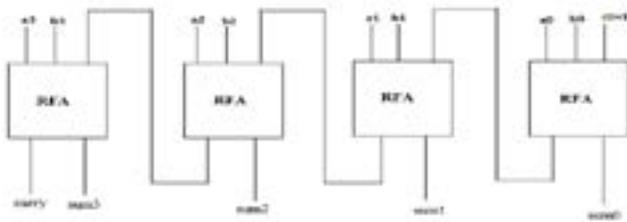


Figure 6. Novel full adder.

The Figure 6 shows the novel reversible ripple carry adder design employing full adders.

6. Results and Discussion

The proposed novel adders are designed and simulated using the cadence environment and QCA framework. Assessment submits is made between existing method and the proposed method which is shown in Table 1. Here, the Quantum cost, Number of Constant inputs and number of Garbage outputs are calculated for proposed novel adders and the proposed design shows betterment as compared to existing adders^{3,7}.

Table 9. Comparison table of reversible half adder

S. NO.	Content	Quantum Cost (QC)	No. of Constant Inputs (CI)	No. of Garbage Outputs (GO)
1	Fredkin ³	7	1	1
2	Proposed Method	6	1	1
3	% of Improvement	14.2%	-	-

The Table 9 represents the design of half adder which shows a significant improvement in terms of Quantum Cost. The Table 10 represents the simulation of reversible gates, it can be seen that the proposed reversible gates is better in terms of number of cells used, area and simulation time. The proposed reversible gates and adders are been simulated in Gate Level and QCA environment. The proposed gates are seems to be feasible as it shows improvement in the number of cells used. Area and simulation time as indicated in the comparison table. Further the ALU can be designed by using these proposed

half adders and full adders⁸. As the important arithmetic operations can be carried out by employing half and full adders.

Table 10. Comparison table of Reversible Gates

S.NO.	Content	No of cells used	Area μm^2	Simulation time(sec)
1	Fredkin gate ⁶	187	0.19	33
2	DKG gate ⁶	752	1.24	16
3	MRG gate ⁶	456	0.52	45
4	Proposed Method(RG1)	108	0.20	23
5	Proposed Method(RG2)	113	0.20	1
6	Proposed Method(RG3)	168	0.20	33

6.1 Simulation in Cadence Environment

The Figure 7 shows the schematic of RG1, it is simulated for various input combinations. The gates used in this schematic are XOR, NOT, and AND.

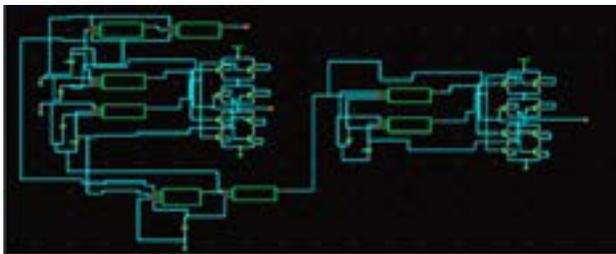


Figure 7. Schematic of novel gate (RG1 Gate).

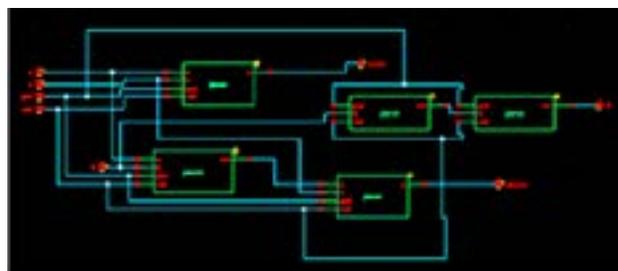


Figure 8. Schematic of novel gate (RG2 Gate).

The Figure 8 shows the schematic of RG2, it is simulated for various input combinations. The gates used in this schematic are XOR, NOT, and AND. The different functionalities of RG2 gate is simulated and it is verified.

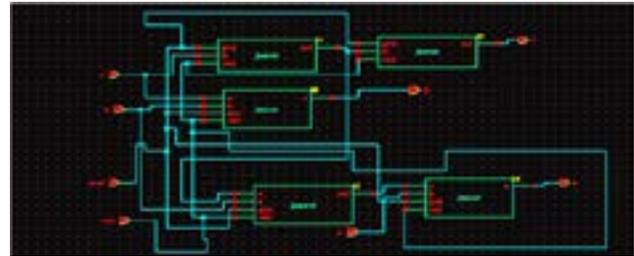


Figure 9. Schematic of novel gate (RG3 Gate).

The Figure 9 shows the schematic of RG3, it is simulated for various input combinations. The gates used in this schematic are XOR, NOT, and AND.

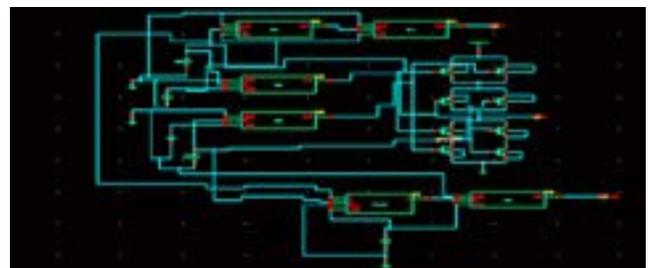


Figure 10. Schematic of novel half adder.

The Figure 10 shows the schematic of reversible half adder the number of constant inputs employed here is 1.

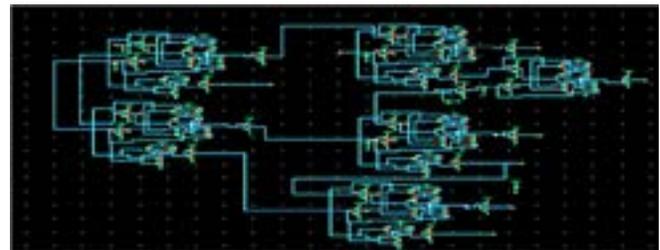


Figure 11. Schematic of novel full adder.

The Figure 11 shows the schematic of reversible full adder the number of constant inputs employed here is 3.

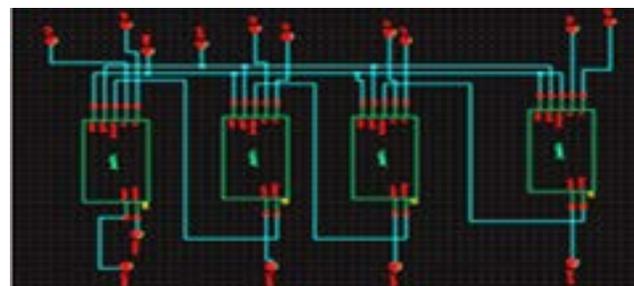


Figure 12. Schematic of novel ripple carry adder.

The Figure 12 shows the schematic of novel ripple carry adder. The RCA employs four novel reversible full adders. The number of constant inputs employed here is 12. The simulation is performed and tested for various input combinations.

6.2 Schematics using QCA Framework

In Quantum Cellular Automata (QCA) the polarization of each cells must be determined. The polarization of the desired cells can be found out by knowing the polarization of the neighboring cells this can be determined by the number of samples in the bistable environment⁹.



Figure 13. QCA layout of RG1.

The Figure 13, shows the QCA layout of Reversible Gate1 the Quantum Cost of this gate is 6. The number of cells need to implement this cell is 108.



Figure 14. QCA layout of RG2.

The Figure 14, shows the QCA layout of Reversible Gate1 the Quantum Cost of this gate is 7. The number of cells need to implement this cell is 113.



Figure 15. QCA Layout of RG3.

The Figure 15, shows the QCA layout of Reversible Gate 3 the Quantum Cost of this gate is 8. The number of cells need to implement this cell is 168.

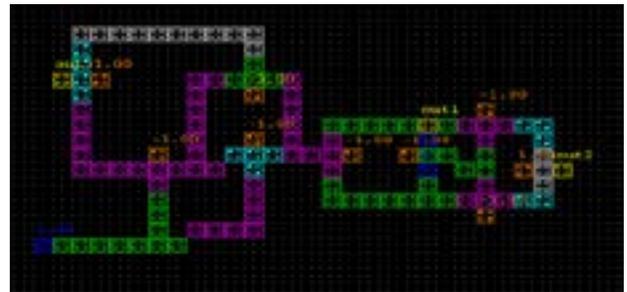


Figure 16. QCA Layout of novel half adder.

The Figure 16, shows the QCA layout of Novel Half Adder. The Quantum Cost of this reversible half adder is 6.



Figure 17. QCA layout of novel full adder.

The Figure 17, shows the QCA layout of Novel full Adder. The Quantum Cost of this reversible full adder is 18.



Figure 18. QCA layout of novel ripple carry adder..

The Figure 18, shows the QCA layout of Novel ripple carry Adder. The Quantum Cost of this reversible half adder is 72.

7. Conclusion and Future Work

Based on the concept of reversible logic, three novel Reversible Gates are proposed. The adders (HA, FA and RCA) were designed using the proposed reversible gates. The complete schematic is designed in Gate Level using Cadence and implementation done in QCA framework. The simulated results prove that the Number of cells used in the design, area and simulation time was reduced when compared to the existing designs in the literatures. Further these structures can also be employed in the Reversible Multiplier design and ALU design^{10,11}.

8. References

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