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Comparative Analysis of different Algorithm for Design of High-Speed Multiplier Accumulator Unit (MAC)

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Abstract

Background/Objectives: Power consumption is one of the important designsin many digital signal processing applications, the main building blocks of the processor is Multiplier-Accumulator (MAC) unit. **Methods/Statistical Analysis:** In the present work, the Baugh-Wooley multiplier is implemented for improving the performance of MAC unit. The Baugh wooley multiplier is faster than the other multipliers like Array multiplier, Wallace tree multiplier, Booth multiplier. The MAC unit using Baugh-Wooley multiplier is implemented using 180nm technology in cadence virtuoso. **Findings:** The speed of MAC unit using Wallace tree multiplier is 93.6MHz and with Baugh wooley multiplier is 99.1MHz. The power consumption of the MAC unit using Wallace tree multiplier is 2.265mW and with Baugh wooley multiplier is 4.628mW. The results show that the MAC unit using Baugh wooley multiplier is faster than the Wallace tree multiplier. **Application/Improvements:** MAC unit processors. In future, we can implement MAC unit using Baugh wooley multiplier withapipelining technique such that the total power consumption will be less.

Keywords: Accumulator, Baugh-Wooley Algorithm, High Speed, Low Power, Multipliers, Pipelining

1. Introduction

There has been high demand now a days for high speed but low power consuming devices. To achieve this Multiplier-Accumulator unit is needed[1]. The multiply-accumulate operation is the main user defined accelerator routine in digital signal processing architectures. It determines the speed of the overall system as it is critical path. To increase the performance of digital signal processing,we need a high-speed Multiplier-Accumulator unit for real-time applications[2,3]. The multiply accumulate unit performs the critical operations in many of the processing applications.

Low-power and high-speed circuitry are playing a crucial role for VLSI systems[4]. The main objective of this work is to investigate how to increase thespeed of multiplier and accumulator unit and suitable algorithms which are more efficiently suitable for implementation the high throughput signal processing algorithms and also to achieve the low power consumption[5]. This is because the speed and throughput rates are always been concerned with the digital signal processing systems. These MAC units become the essential building blocks for the applications as digital filtering, speech processing, video encoding and cellular phone in the digital signal processing. A variety of approaches to implementing the multiplication and addition of the MAC functions are possible. A conventional MAC unit is of the combination of themultiplier, adder and an accumulator that contains the sum of the previous consecutive products.

The MAC is designed using Baugh-Wooley multiplier. These applications include filtering, convolution and the inner products. The Baugh-Wooley multiplier is signed multiplier having the less delay[6]. The function of the MAC unit is used for high-speed filtering and other processing units typically for digital signal processing. The Mac unit designed by the multiplier and accumulator consists of the sum of the previous successive products. The MAC

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inputs are taken from the memory location and give to themultiplier. The Mac unit multiplies 2 values, then adding the result to the previously accumulated value and restored in the register for future accumulations. Here the MAC is designed with the Baugh-Wooley multiplier and with the pipelining technique.

2. Multipliers

Different kinds of multipliers have been used to design the MAC unit, which is given below.

2.1 Booth Multiplier

Booth multiplier isacombination of multiplicand and multiplier in addition with the partial product generator and booth encoder[7]. The partial products are to be generated by using booth encoding technique. Hence, the total number of partial products willreducemore as compared to the conventional multiplier techniques. Finally, all the partial products are to be added by using Carry Save Adder (or) Ripple Carry Adder and the results are gathered in the Accumulator. However, the structure of booth multiplier is increased due to thecomplexity of the booth encoder. The architecture of booth multiplier is given in Figure1.

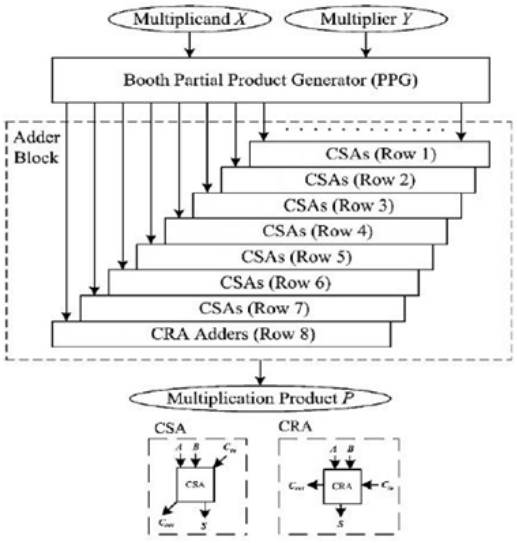

Figure 1. Architecture of booth multiplier

2.2 Array Multiplier

Array multiplier is one of the best conventional multipliers where the partial products are to be generated by AND gate logic. All the partial products are then added by using the half adders and full adders depend upon on the number of inputs[8]. The architecture of Array multiplier is given in Figure 2.

Figure 2. Architecture of array multiplier.

2.3 Wallace Tree Multiplier

Wallace tree multiplier uses the Carry Save Addition to add the partial products generated in each stage. Hence, carry generated in the present state is saved and added to the next state. Hence, the delay will be reduced because carry will be reduced[9]. The design of Wallace tree multiplier is shown in Figure 3

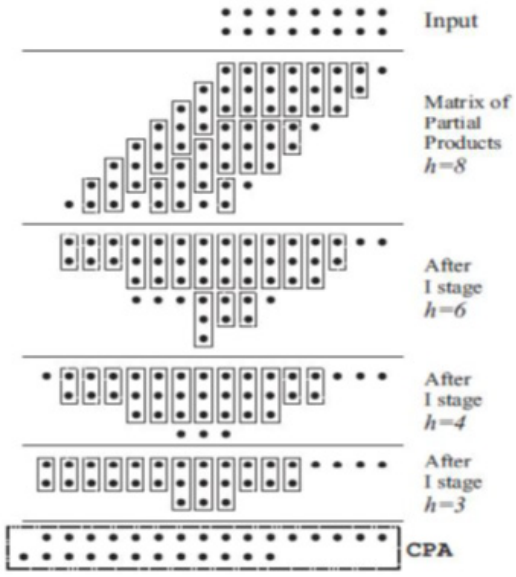

Figure 3. Wallace tree multiplier

2.4 Baugh-Wooley Multiplier

The Baugh-Wooley multiplier is faster than a simple array multiplier, Wallace tree multiplier and booth

multiplier because it used for the complex circuits and it uses'scomplement so the number of partial products will be reduced. The Baugh-Wooley multiplication is one of the best methods to multiply the signed numbers[10]. The Baugh-Wooley multiplier is signed multiplier having less delay. The Baugh-Wooley multiplier uses the ripple carry adder in the final stage. The block diagram of the 4X4 Baugh-Wooley multiplier is shown in Figure 4.Algorithm for 4 X 4 Baugh-Wooley multiplier is given in Figure 5.

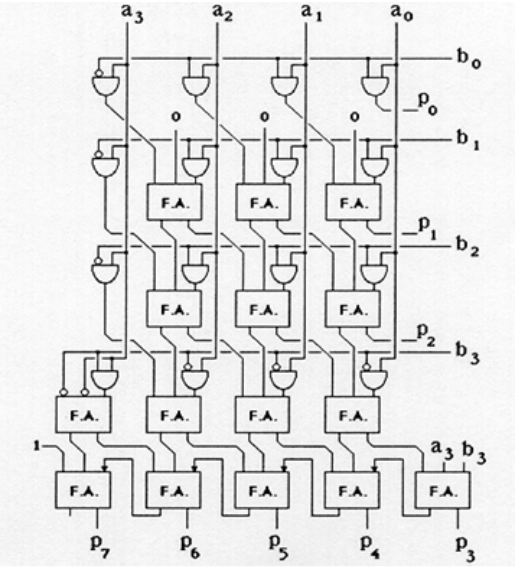

Figure 4. 4 X 4 Baugh-Wooley multiplier.

						a3	a2	a1	a0
*						x3	x2	x1	x0
						-a3x0	a2x0	a1x0	a0x0
					-a3x1	a2x1	a1x1	a0x1	
				-a3x2	a2x2	a1x2	a0x2		
			a3x3	-a2x3	-a1x3	-a0x3			
=		s7	s6	s5	s4	s3	s2	s1	s0

Figure 5. Algorithm for 4X4 Baugh Wooley multiplier

3. Conventional Mac Unit

MAC is the building blocks of a processor and having a great impact on the speed of theprocessor. MAC is consists of theadder, multiplier and an accumulator[5]. The MAC inputs are taken from the memory location and give to themultiplier, which performs the multiplication and result are given to the adder and adder will add the multiplication results are accumulated by using accumulator and then will stores the result into a memory location[2]. The block diagram of MAC unit is shown in Figure 6.MAC unit mainly consists two parts, Multiplier and Accumulator.

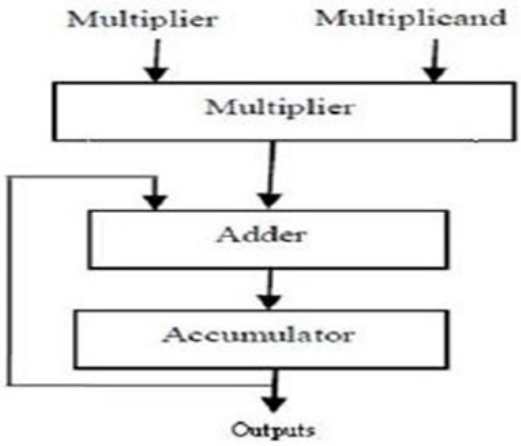

Figure 6. Block diagram of MAC unit.

3.1 Multiplier

Multiplication is one of the basicoperations in the signal processing algorithms. Multipliers are having alarge area, long latency and they consumes considerable power. So low power multiplier design has an important need in low power VLSI systems[8]. There is extensive work on low power multiplier's system performance is determined by the performance of the multiplier because of themultiplier is generally the slowest element in the system.

Hence, the speed of the multiplier is a major concept in design systems[6]. However, area and speed are usually the conflicting constraints to improve the speed in larger areas. So, a whole spectrum of multipliers with different area-speed constraints has been designed.Basically, themultiplier is divided into three steps. The first step is booth encoding in which partial products are generated from the multiplier and multiplicand. The second step is adder to add all partial products and converts in the form ofthesum and carry. The last is the final step is addition[1,8] where the final multiplication results are generated by adding the sum and carry. So to generate the sum and

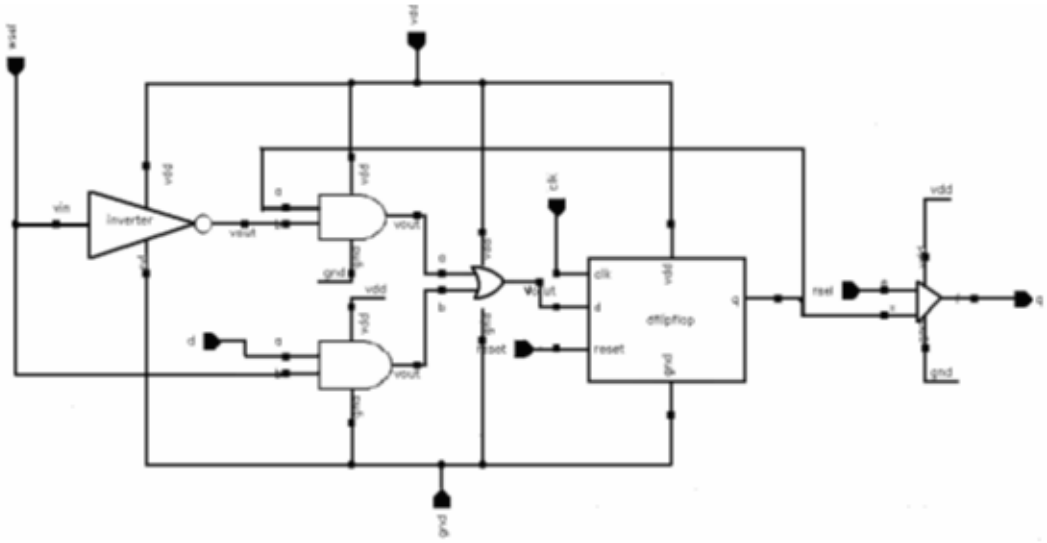

Figure 7. 1-bit accumulator.

carry of the products we use the full adders which are adding the 3 input bits data and gives sum and carry. The full adders can be implemented in many ways like in 28T, 20T, 16T, 14T, 10T and 6T which causes the less power consumption[11]. In this work, we use the conventional full adder with 46T.

3.2 Accumulator

The accumulator is also called as a register. Register holds the output of the previous clock from the adder. Holding the outputs in theregister will reduce the additional adding operations[7]. The architecture of 1-bit accumulator is shown in Figure7.The accumulatorhas used the D flip-flop, two AND gates and one OR gate. The cell is consistsof three inputs and one output. The three inputs are write select, read select and D input and Q is the output. The D-flip-flop will store the value of the input signal and whenever to write select and read select are equal to 1 thenthe input will pass to the output trough a tri - state buffer which allows controlling the current passed through the device. A tri-state buffer has two inputs, data input x and control input. Whenever the data input is high the output will be the input and if the data input is low the output will be Z and finally for fast response of the accumulator we need to implement the one fastest adder like carry select adder[12].

4. Simulation Results

The simulation results of MAC unit usingBaugh-WooleyMultiplier is given in Figure 8.

Table 1. Comparison of power consumption and speed of MAC unit with respect the different techniques

Technique	Power Consumption (mW)	Speed
MAC unit using Wallace Tree Multiplier	1.399	93.6 MHz
MAC unit using Baugh-Wooley Multiplier	2.743	99.1 MHz

All the above results are getting at input voltage 1.8 V.

The Table 1 shows that the speed of MAC unit using baughwooley multiplier is more than the Wallace tree multiplier.

5. Conclusion

Analysis of the MAC unit with the Wallace tree multiplier, Baugh-Wooley multiplier and pipelining technique has done by using cadence virtuoso 180nm technology. The Baugh-Wooley algorithm is a relatively straightforward way of doing signed multiplications. The Baugh-Wooley

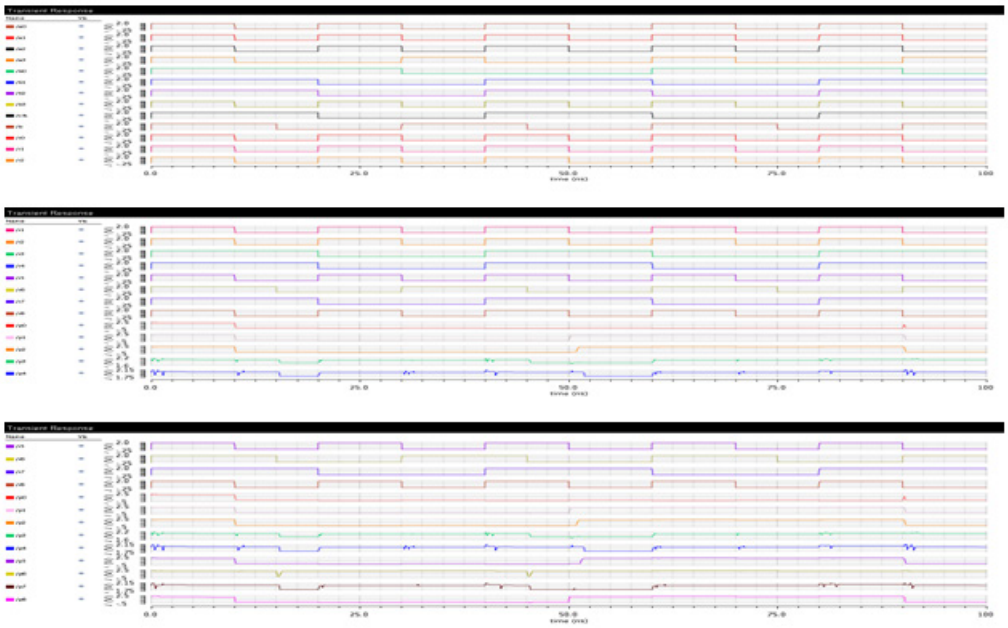

Figure 8. Output waveforms of MAC unit using Baugh-Wooley multiplier.

multiplier reduces the partial products to the MAC unit. So the power consumption is low. By using Baugh-Wooley multiplier the speed of the circuit has been increased and due to pipelining technique the power consumption also very less as compared to the Wallace tree multiplier. In future if it is possible to reduce the power consumption of the Baugh-Wooley multiplier so that the MAC unit speed will increase.

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