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High Gain Opamp based Comparator Design for Sigma Delta Modulator

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Abstract

Sigma delta ADC is mainly used in resolution based application. But the gain of the sigma delta modulator is low. The main objective of the paper is to design the comparator with high gain. Comparator with low gain cannot drive the load effectively through the entire circuit. This paper was designed and simulated using 180 nm process technology (GPDK 180 nm library) in CADENCE Virtuoso Analog Design Environment. In sigma delta ADC, each block should drive the load effectively to the entire circuit. So that the output will come accurately and delay will be less. Based on that concept, need to design the comparator that can be used in sigma delta ADC. In this point of view, some comparators are analysed. In this paper, analyse the performance of regenerative comparators and op-amp based comparators. And find which will efficient comparator for using at sigma delta modulator. Dynamic comparator, double tail comparator, modified double tail comparator are analysed. The gain of these operational amplifiers are low. So high gain based operational amplifier should be designed. For that, first one op-amp was designed which has 84 dB gain. Using this opamp, one comparator was designed. This comparator has high gain. So it can be used for sigma delta ADC for drive the load. And also it meets certain other constraints like speed and moderate power.

Keywords: CMOS, Opamp Based Comparator, Regenerative Comparators, Sigma Delta ADC, UDSM CMOS Technology

1. Introduction

Comparator is used to compare two inputs and give larger one as an output. The inputs may be voltage or current. Basic comparator has two inputs that are analog signals and one output that is digital signal.

Comparator is one of the basic block in Analog to Digital Converters (ADC). According to the purpose of the ADC different types of comparators are used. Some comparators designed for reduced power dissipation. Some may be regarding speed. Normally ADCs need high speed, low power and low area comparators. High speed comparators which act in UDSM CMOS technologies undergo low voltages particularly while considering threshold voltages[1]. It may not been mounted at the similar as the supply voltages of the current CMOS methods. Challenging factor is designing a high speed comparator with low supply voltage. It takes large area and high power.

2. Clock Regenerative Comparators

Clock regenerative comparators are widely used in high speed ADCs because they have positive feedback in regenerative latches to take fast decisions[2]. Comprehensive analyses are used to analyse the performance of different comparators from different aspects like kick back noise and noise offset. In this paper we analyse the performance of conventional dynamic comparator, conventional double tail comparator, modified double tail comparator and opamp based comparator.

2.1 Dynamic Comparator

Figure 1 displays the schematic view of dynamic comparator that is generally used in ADC. The operation of this comparator follows: In the reset stage, the clock is zero and transistor M_{tail} is off and reset transistors $M_{7,}$

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M_8 makes the output node Out_n, Out_p to VDD[3]. During comparison phase, the clock is equal to VDD, transistors M_7, M_8 get off and M_{tail} gets on. At this phase output voltages starts precharge to VDD. It starts discharging depending upon the input voltage. If $V_{inp} > V_{inn}$, then Positive side of output gets discharged faster than another side. Because Outp falls down to VDD–$|V_{thp}|$ before of another side. Here Out_p gets discharged by M_2 drain current. And Outn discharged by M_1 drain current.

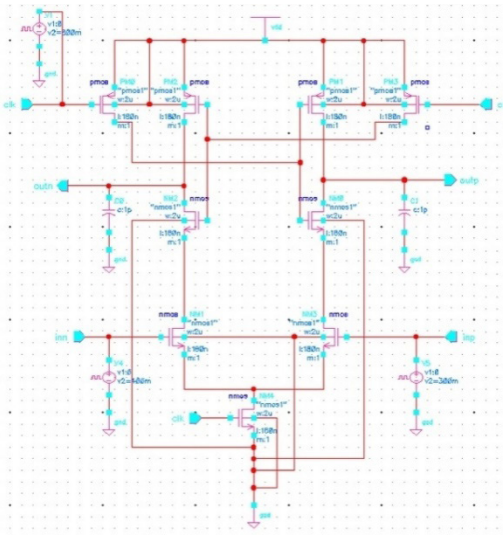

Figure 1. Schematic view of dynamic comparator.

The transistor M_5 will turn on and initiating regenerative latch because of back to back invertors that is M_3, M_4, M_5, M_6. So the Outn start precharge to VDD and Out_p start discharging towards ground[4]. If $V_{INP} < V_{INN}$, then action is reverse. This comparator has two time delays, they are t_0 and t_{latch}. The t_0 delay indicates the discharging capacity of C_L upto M_5 or M_6 gets on. That is until p-channel transistor turns on. If $V_{INP} > V_{INN}$, then Out_p discharge faster. Because of I_d of transistor M_2. This is driven by the transistor M_1 with very low current. The delay, t_0 is represented as:

$$t_0 = \frac{C_L|V_{thp}|}{I_2} \cong 2\frac{C_L|V_{thp}|}{I_{tail}}$$

The delay, t_{latch} is a latching delay between the cross coupled inverters. The voltage swing is the difference between the initial output voltage and falling output. In that half supply voltage is consider as threshold voltage. The latch delay is represented as:

$$t_{latch} = \frac{C_L}{g_{m,eff}}.\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}}.\ln\left(\frac{VDD/2}{\Delta V_0}\right)$$

Advantage of this comparator is high input impedance, no static power and rail to rail swing. In order to minimize the offset voltage, input transistors will design. The disadvantage is, it needs more voltage for maintaining correct delay period due to stacked transistors. And another drawback is, it has only one path for current through tail transistor M_{tail}. It is used for differential amplifier, latch. Though small tail current is used to retain the differential pair in pathetic reversal and achieve extended integration pause, large tail is needed for fast regeneration in the latch. Mostly M_{tail} operates in triode state and tail current rest on input common type voltage. It is not advantageous for reinforcement operation.

2.2 Double-Tail Dynamic Comparator

Figure 2 displays the schematic view of conventional double tail comparator. It has less stacking so that it can operate at low voltage than the dynamic comparator. When the clock is zero, transistors M_{tail1} and M_{tail2} are in off condition. And the transistors M_3 and M_4 precharge the nodes f_n, f_p to VDD and M_{R1}, M_{R2} gets discharge towards the ground[1]. When clock is at VDD, transistors M_{tail1} and M_{tail2} are in on condition. And the transistors M_3 and M_4 turn off and f_n, f_p nodes start to discharge. It discharged in the rate defined by C_{fn} (p) and V_{fn}(p) will buildup. The transistors M_{R1}, M_{R2} forms intermediate stage and V_{fn}(p) passes to the cross tied inverters and it offers worthy protecting between input node and yield node. It reduces the kickback noise. It also has two types of delay, t_0 and t_{latch}. t_0 represented as capacitive charging of C_{Lout}, that is between the starting of latch regeneration and turning on of first n-channel transistor, that is turning on of M_9 or M_{10}. This is achieved from,

$$t_0 = \frac{V_{Thn}C_{Lout}}{I_{B1}} \approx 2\frac{V_{Thn}C_{Lout}}{I_{tail2}}$$

Here I_{B1} is drain current of transistor M_9. And this drain current is equals to half of the I_{tail2}. Here voltage at the positive node is higher than the voltage at the negative node. When the M_9 turns on, the output node that is Out_n started discharging to ground. And front p-channel transistor also turns on. It makes Out_p, charging towards VDD. The regeneration time is obtain same like dynamic comparator. At time t_0, the voltage difference of output is achieved using,

$$\Delta V_0 = V_{Thn}\left(1 - \frac{I_{B2}}{I_{B1}}\right)$$

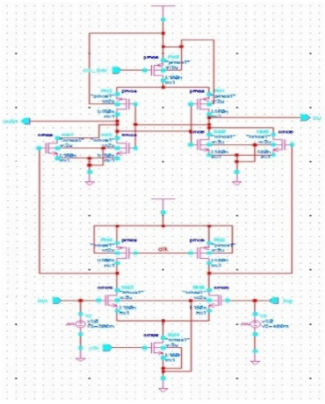

Figure 2. Schematic view of conventional double tail comparator.

From this, two main factors are obtained. They are:

At time $t_{0,}$ difference between the voltages at output has high effects on latch primary differential production voltage and also in latch interval. So by increasing this voltage difference helps to decrease the delay of the comparator.

In this comparator, transitional stage transistor does not have any effect on transconductance. So these transistors are cut off at final stage. Because of nodes fn and fp discharge towards ground, transistors don't have effect on transconductance. At the reset phase, it needs to precharge from the bottom level, i.e. it needs to charge from ground to power supply. So it takes more power consumption.

2.3 Modified Double Tail Dynamic Comparator:

Figure 3 displays the schematic view of modified double tail dynamic comparator. The dynamic comparator has better performance at low voltage. So using dynamic comparator architecture, new architecture will design. It increases the speed of latch regeneration by increase $V_{fn/fp}$. For this reason, two transistors are added with architecture. That are control transistors, namely M_{c1} and M_{c2}. These transistors are cross coupled and parallel to the transistors M_3/M_4.

When CLK = 0, M_{tail1} is in off stage and M_{tail2} also in off condition. It avoids static power dissipation. The transistors M_3 and M_4 make the nodes f_n, f_p to charge towards VDD. The transistors at intermediate stage, reset all latch outputs as ground[5].

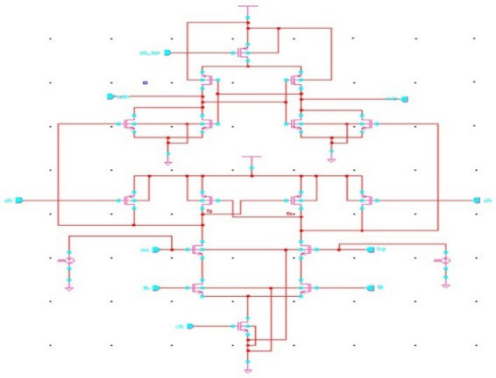

Figure 3. Schematic view of modified double tail dynamic comparator.

For the period of decision making phase, CLK is VDD. And transistors M_{tail1}, M_{tail2} are in on condition. And M_3 and M_4 are in off condition. At starting of decision making phase, M_{c1} and M_{c2} are at off condition because, the nodes f_n, $f_p$are at VDD. So as per the input voltages, these nodes are drop at different rates. If $V_{INP} > V_{INN}$, then f_n drops faster. Because M_2 provides high current than M_1. Whereas f_n falling, equivalent control transistor, i.e. M_{c1} turns on. And node f_p return to VDD. At the time M_{c2} at off condition and f_n fully discharged. When time increases, difference of f_n and f_p also increases as exponential. That reduces the regeneration time of latch. There is one effectiveness in this architecture. That is if any one of the control transistors gets on, the current drain from power supply to ground through the transistors M_{c1}, M_1, and $M_{tail1.}$ i.e. through the tail transistors and input transistors. So it takes static power consumption[6]. Using nMOS switches below the input transistors, this issue is overcome. Here M_{sw1}, M_{sw2} are the nMOS switches.

At the starting of this phase, nodes f_n, f_p have been precharged to VDD. So both switches are closed and those nodes starts discharging with different rates. When the comparator identifies that any one of the node discharging faster, then control transistors increase the difference between the voltages. If f_p is precharged to VDD, then f_n discharged fully. So charging path at f_p will be open. It avoids current drained from power supply. But another switch which is connected to f_n will close to permit the discharge in this node. Control transistors operation similar to the latch operation.

Modified double tail comparator increases speed by affecting two factors. They are, when time is at t_0 it

increases the difference between the voltages. And second one is, it increases the latch transconductance.

2.3.1 Effectof Enhancing V_0

The delay, t_0 is a time takes till the main nMOS transistor of back-to-back inverters goes on. It decreases one of the outputs and starts regeneration. At $t_{0,}$ voltage difference of latch output has effect on latch regeneration time. Output voltage is inversely proportional to the regeneration time. If V_0 high, then regeneration time is less.

$$\Delta V_0 = 4V_{Thn} \mid V_{Thp} \mid \frac{g_{mR1,2}}{I_{tail2}} \frac{\Delta V_{in} g_{m1,2}}{I_{tail1}} \exp\left(\frac{G_{m,eff1}.t_0}{C_L, f_{n(p)}}\right)$$

2.3.2 Enhancing Latch Operative Transconductance

In this comparator, at starting stage of decision making phase, output nodes of first stage will charge to VDD. That makes intermediate stage turns on. So that latch transconductance is increased. That means it reinforced the positive feedback.

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \ln\left(\frac{\frac{VDD}{2}}{\Delta V_0}\right)$$

2.3.3 Opamp Based Comparator

In sigma delta ADC, the outputs should be drive through all the blocks. So it needs high gain. Based on this requirement, opamp is designed and that will be used in comparator[7]. Consider the specification for required opamp that is specially used in sigma delta modulator[8–10]. In two stage opamp, first stage is differential amplifier and second stage is cascade amplifier. Current mirror circuit also present in the architecture. The target gain is 75 dB. CMR ratio is minimum 0.8 V to maximum 1.6 V. Table 1 shows the specifications of opamp.

Table 1. Specifications of opamp

Specifications	Values
DC Gain	75Db
Gain Bandwidth	30MHz
Phase Margin	60^0
Slew rate	20V/μsec
ICMR(+)	1.6V
ICMR(-)	0.8V
VDD	1.8V

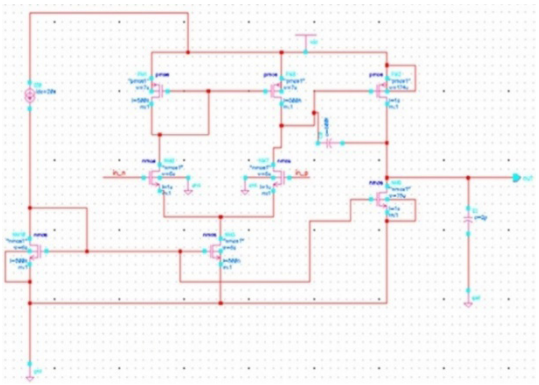

Figure 4. Schematic view of two stage opamp.

Figure 4 displays the schematic view of two stage opamp design. By modifying W/L ratio will affect the transconductance of transistors. Thus it will help to increase the gain of the design. W/L ratios of these transistors will calculate using some concepts. W/L ratio of transistor M_1, M_2 will be achieved by:

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m1})^2}{\mu_n C_{ox} * 15}$$

Here gm1 is transconductance of transistor $M_{1.}$ It is represented as:

$$g_{m1} = GBW * C * 2\pi$$

Here GBW means Gain Bandwidth. Consider that as a 30 MHz. likewise every transistors W/L ratio should be find as per the calculation. Some of the formulas used to calculate the W/L ratios of various transistors is shown below:

$$(W/L)_{3,4} = I_5/(\mu_p C_{ox}) * [VDD-(ICMR+)-V_{T3}+V_{T1min}]^2$$
$$(W/L)_5 = I_5/(\mu_n C_{ox}(Vds\ 5sat_)^2)$$
$$(W/L)_6 = (g_{m6}/g_{m4})(W/L)_4$$
$$(W/L)_7 = (I_7 \times I_5) \times (W/L)_5$$

Table 2. W/L ratios of transistors

Transistor	Calculated W/L ratio	W/L ratio for increasing gain
$M_{1,}$ M_2	6	12μ/2μ
$M_{3,}$ M_4	14	7μ/0.5μ
$M_{5,}$ M_8	12	6μ/0.5μ
M_6	174	348μ/2μ
M_7	75	75μ/1μ

Table 2 shows the W/L values of transistors. They are, $M_1 = M_2 = 6$, $M_3 = M_4 = 14$, $M_5 = M_8 = 12$, $M_6 = 174$, $M_7 = 75$. If we increase the length, then transconductance of the transistor will increase. So increase the length also achieve the obtained value. Using this value the opamp is designed. And it reaches the gain value as 84 dB.

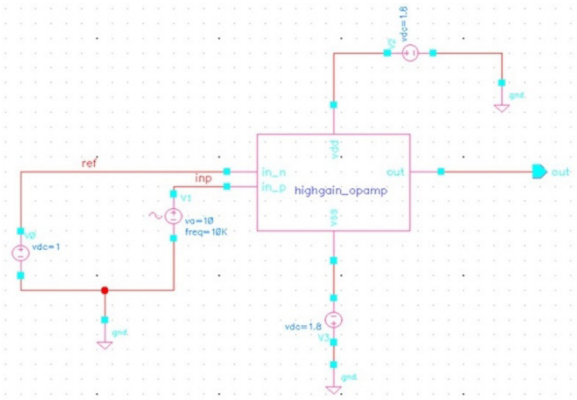

Figure 5. Schematic view of opamp based comparator.

Using this opamp design, comparator is designed. The schematic diagram of opamp based comparator is shown in Figure 5. This design met the functionality of the basic comparator. If the input voltage is greater than the reference voltage i.e. threshold voltage it gives the output as high or 1. If the input voltage is lesser than the reference voltage then it gives the output as low or 0. The output of the opamp based comparator is shown in Figure 6.

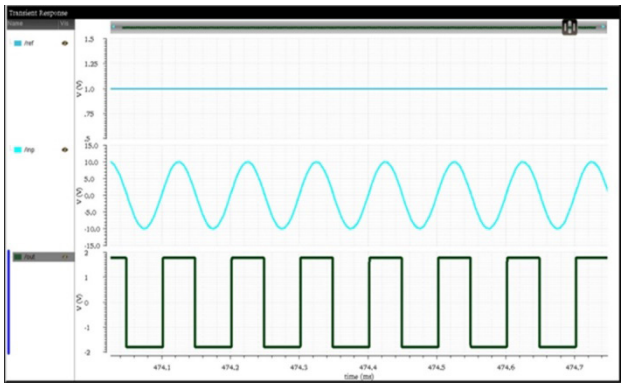

Figure 6. Output of opamp based comparator.

4. Conclusion and Future Work

In this paper, comparison of dynamic comparator, double tail comparator, modified double tail comparator and opamp based comparator was performed. Among this, found that opamp based comparator is most suitable one for sigma delta ADC. In future, using this comparator can able to design a sigma delta modulator.

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