ISSN (Print) : 0974-6846
Indian Journal of Science and Technology, *Vol 9(29), DOI: 10.17485/ijst/2016/v9i29/90875, August 2016* ISSN (Online) : 0974-5645

Cell Stability and Power Reduction using Dynamic Isolated Read Static Random Access Memory

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Abstract

The channel scaling attains the overflow current at the transistor, which impacts on power indulgence. In order to attain reduced power and delay, the devices are assumed to decrease its size. Then transistors size can also be changed. In this paper the unique dynamic isolated read SRAM has been projected for dropping the total power. By linking, the cell with 6T and NC SRAM in numerous features, high constancy and decreased power is achieved by the curvature N (noise) method, which is done when the system is in active mode. The values are calculated with the voltage of 1.8 which reduces 90% of power than the 6T, and 18% of power is reduced than the 8T SRAM cell, and 30% of leakage current is reduced as compared to 6T cell. Thus when related to the existing SRAM, the cell consumes less power and without any distortion the cell stores the data. Also the constancy of the cell is improved when compared with the other cell. The waveform result shows that the cell attains enhanced stability and reduction in overflow using the cadence virtuoso technology of 180 nm.

Keywords: Curvature-noise, Stability, Static Current Noise Margin, Static Voltage Noise Margin, Write Trip Point

1. Introduction

In order to attain the reduced power and delay the devices are assumed to decrease its size. Therefore the supply, transistors size can be changed. The overflow of voltage occurs when the channel is thin. The v^{th} also has the low consuming energy. Sometimes the v^{th} in SRAM is suitable for integrating the logic. If the supply is reduced then the leakages goes higher that causes indulgence of power. If it is comprised to be low then the reliability, working goes effective. The power overflow also arises due to the area consideration in the cache it is around 50%.the constancy (stability) is the issue, which is the demanding factor. However when the power is controlled, the reliability goes lower. The stability defines the noise factor of the cell and it has to be higher. Due to converting the mode from sleep to active mode the SRAM indicates more amounts of voltage flows.

The channelling current contains leakage and that depends on many ways of intersecting nodes. That is reduced by P-FET, which is replaced for N-FET[1]. The most common leakage arises due to supply dropping. This diminishes the power at the time of inactive mode. The fault rate in the cell causes errors, which destroys the bit that occurs due to α ray[2]. That is stopped by splitting the bit lines[3]. Write margin for next generation SRAM[4] and different types of SRAM topologies[5] are described in subsequent papers. The area for the SRAM cell must be lower in order to integrate the cell in the SOC. To enhance the cell, constancy is analysed using noise factor (Curvature-N)[6]. Various approaches are defined for cell constancy. The comparison is made between the write and read operation using curvature N analysis for the 12T. It improves the constancy by comparing the cell with 6T. The cell on the bases of CNFET is also the advantage to develop the performance. By separate BRL, it achieves the power, and gain of the structure[7] which is analysed with the tools variation[8].

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Hence, to get low power and to improve constancy, an isolated read SRAM is projected. The separate Read structure is added to the cell[9]. Thus a new method is performed to reduce its power during active and inactive mode process. Similarly, to increase its constancy separate structure for read and write is analysed. That causes a minor increase in its area and delay, which is not more than 8T. Multiple port model is well defined using PA algorithm it is found by assigning fault in memory, which is efficient in MBIST[10]. Address generator is structured using MBIST. It requires less power and switching[11] and for submicron designs NC-SRAM has low leakage[12]. SRAM cell design for stability methodology[13] has more stability. The cell optimization for SRAM designs[14] and analysis of SRAM cells are described here.

2. SRAM Cell Comparison

2.1 Conventional SRAM

The SRAM consumes two inverters. The NMOS transistor N4, N3 acts as an enabling transistor. The bit1 or bit0 is read by a cell using word line called WL. It is to be turned ON to activate the enabling transistor. The bit is written by a cell using bit line called BL and BLBAR.

2.1.1 Operating Modes

In this conventional 6T as shown in Figure 1, the read and write of bit 0 and 1 is done by using three modes. The working of SRAM cell depends on these three modes, they are.

Standby mode: The word line is low, and so the enabling transistors N4, N3 is switched OFF. Thus the BL and BLBAR is detached from the cell. As the supply is connected to the cell the combined inverters supports each other by passing the bit.

Read mode: Word line is selected and so, the transistors N4, N3 are designated to be ON with the help of WL. When these transistors are selected, the data in A and B are shifted to BL and BLBAR. If suppose the data in A is 1 and 0 at B .The current does not moves in the direction of N3 similarly, particular amount of current moves in the direction N4. Therefore, BL is forced to be active through P1 and BLBAR releases the bit through N1.

Write mode: For write 0 operation, A and B has to be identical means A is 0 and 1 at B. According to this BL and BLBAR is requested to be pre charged manually by 0 and 1. Once bit lines are initiated, WL is designated. Hence 0 at BL use to pull down the bit at A, which acts as the input for the transistor P2, N2.This forces B to be active. Thus write operation is exposed through BLBAR.

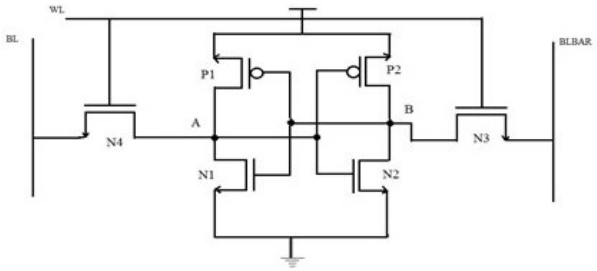

Figure 1. 6T structure.

2.2 NC-SRAM

This type of cell is referred from the (dynamic) Active Voltage Scaling process. This approach is used in the cell to decrease the current, voltage excess and the power. The current overflows are decreased by the supply while the channel length is shorter. The cell holds the data while the cell is in sleep mode. In the concept of NC SRAM cell as shown in Figure 2, the pass transistors N5 and N6 are included with the conventional 6T cell module. That is presented with the change in ground voltages. This type of voltages are depends on modes of the cell. The transistor N5 is connected to source voltage which is positive and assigned to be active during sleep mode and the transistor N6 delivers the cell to be directly grounded during enable state. So these modes is analysed by changing the voltage sources of the pass transistors and that is done to make less leakage. The positive voltage during sleep mode by N5 uses to reduce the leakages at gate than by using N6, which grounds the cell. Thus for this method transistor pull down is raised when pass transistor is included which reduces the excess amount of current and voltage flow. Therefore the constancy for write is enhanced but read time is corrupted and the power intake is lessened. The transistors N5, N6 have high threshold voltages, which switches the source voltage of the NMOS transistor. So

the Transition time for read and write an operation is improved.

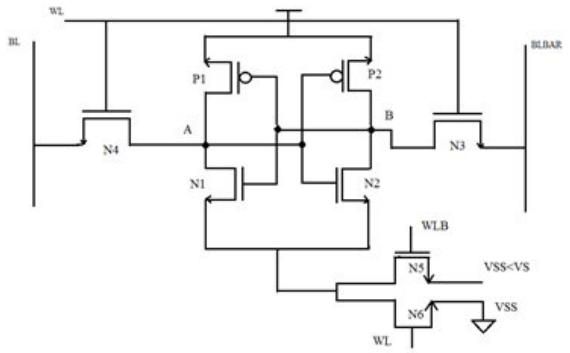

Figure 2. NC SRAM.

2.3 8T SRAM

The cell is arranged with three PMOS and five NMOS transistors as in Figure 3. The bit is stored inside the cell using the consecutive inverters (P1, P2, N1, and N2). The N5 transistor is intended for supply reduction, P3 transistor acts as the switching transistor. Its size must not be greater, as it takes more time for active mode operations. Here for transforming active mode to sleep mode SL signal is preferred. It also varies the faster voltages in active mode. This method is beneficial in the reduction of current overflow at gate of the transistors. Also by comparing 8T SRAM with the 6T cell the power consuming is lesser. The drawback is Area consumption is higher.

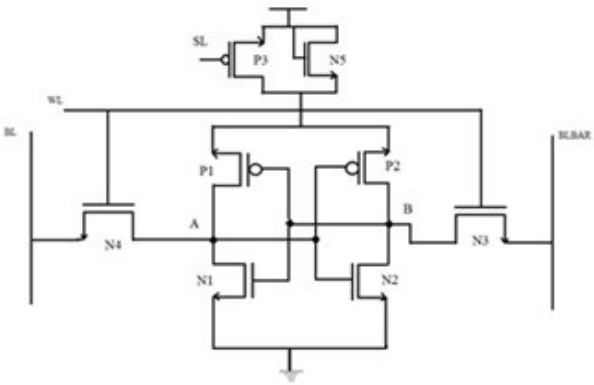

Figure 3. 8T SRAM.

3. Proposed Cell

3.1 Dynamic Isolated Read SRAM

The cell which is shown in Figure 4 is similar to the conventional 6T with two transistor (NR1, NR2). These two transistors are destined for read process. It is forced to be active by P2. N1 is used to pull down the bit. The representation of the whole cell includes eight transistors; it is separated as two structures. The structure includes two circuits: read and write. The cell is consigned, write is done as like the operation in 6T. The read task is done by the two transistors NR1 and NR2. At the time of idle and write mode, the transistors (NR1, NR2) is detached from the cell. From this type of method, the bit that is stored in the cell remains same until the next operation starts. This process is continuously done till (WRL becomes 0). Because of (NR1 and NR2) transistors, the area of the cell consumes moderate, not more than 10T. Due to this issue the array of the cell consumes more area for its memory location similar to 8T SRAM.

3.1.1 Construction

This SRAM requires 8T with isolated read circuit. Whereas, the amount of supply is directly passed into the cell. The operation for sleep and write operation is performed by the cell and the read is performed by the WRL, BRL. Hence during sleep mode nodes are not selected. The bit stores in structure. The WRL, BRL is selected to read. Therefore, the data leftover in BRL. This is done with the bit stored in B, which is assumed to be active with the transistor P2. Same amount of vdd is passed over the read circuit. For the write mode the WL is selected and the value are transferred to the BLBAR to achieve write 1 operation. That is done by charging the BL and BLBAR. Hence the power is saved in read and writes. Therefore the stability factor also improved than the 8T.

3.1.2 Operating Mode

At read process: The read structure line WRL is set as high, and WL as low, so the bit is read and initiated using the P2 transistor. For 1 bit read, the bit stored in the node A is 1, also named as 0 bit write.N2 is inactive during this mode. Similarly for logic 0 read, the bit in A is low, also that is defined to be 1bit write.N2 is enable at this mode. Then the BRL is ready to transfer the stored bit to the cell.

Write mode: At the time of writing WRL is 0 and WL is 1. So that the read structure is detached from the cell. The bit in BL and BLBAR act according to A and B. As like the conventional 6T, write is performed by the cell. Consequently, the bit lines is preselected. On splitting the read and write structure the noise edge goes higher. The

cell controls the inconstancy nature of the nodes. Single bit line (BRL) is preferred for read process. Two bit lines (BL, BLBAR) are required for write process.so the time for the cell to write the bit is lesser. The power is also reduced. So the power takes to read is about 35% less and for write it takes around 50% less when related to conventional 6T. But the area goes comparatively equal to 8T.

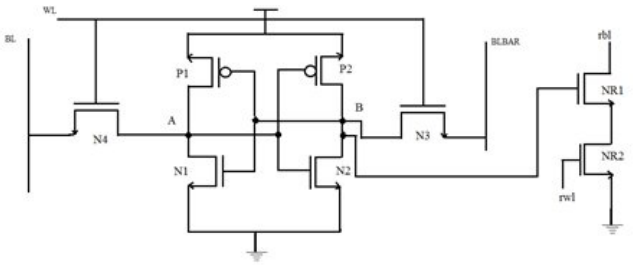

Figure 4. Dynamic isolated read SRAM.

4. Experimental Results

4.1 Transitory Response

The output simulation for the SRAM in write mode is analysed as shown in Figure 5. Hence the corresponding waveforms for read and write is analysed with the supply of 1.8v, technology with 180 nm. Where the performance of 6T is enhanced when compared to the other SRAM structure. It takes lesser amount of time to write the required read bit related to other cell and it is about 6 to 7 ps. Thus the bit is produced in the output, once the bit remains in the cell. The time to write the bit for 8T SRAM is higher, when examined to 6T and NC SRAM. Because of the two transistors (N5, N6) in NC SRAM, the data that takes a time more than 6T but efficient than 8T to reach the BLBAR. It takes 4 % reduction in NC, 2.5 % in 8T and2% in isolated read SRAM.

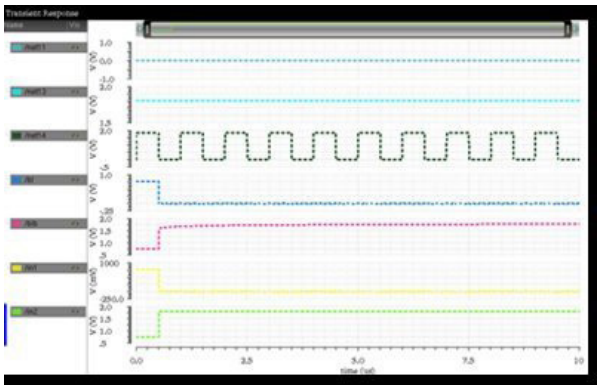

Figure 5. Waveform of dynamic isolated SRAM.

4.2 Power

Table 1 describes the power for the following SRAM with the technology of 180 nm. The amount of the supply is 1.8v.The size of the transistor is assumed to be in a fixed value[14]. The temperature is around 27 Celsius. The complete power is evaluated between the four SRAM cells. The power due to overflows in 8T is 96% reduced by analysing with 6T, and 19% higher than NC. The power goes around 1.35 micro watt which means it is nearly equal to the NC SRAM and lesser than other existing SRAMs which gives 96% less than 6T, and 18% lesser than 8T as shown in Figure 6. The complete power is analysed by the formula $P = \frac{1}{2} C V^2$ .the same SRAM cell with the technology of 90 nm is analysed which takes more power as 118 µW by the supply of 1v in 6T with the time period of 1.25u.

Table 1. Power analysis

SRAM	6T	NC	8T	isolated SRAM
POWER	42.04µW	1.283 µW	1.596 µW	1.351 µW

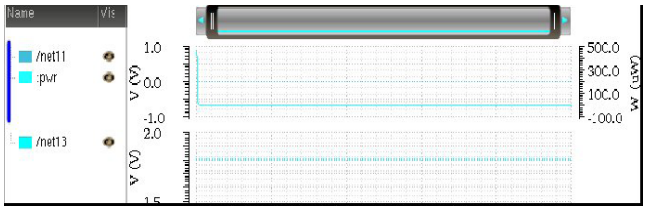

Figure 6. Power for dynamic isolated read SRAM.

4.3 Delay

The Table 2 shows the delay, which is the amount of time the bit takes to stretch to the BLBAR at 10ns.The typical time that takes in 6T is speeder than the other SRAM. The NC and 8T is minimized in its speed due to the additionally added transistor. Similarly in the isolated read low power SRAM the delay goes greater, but lesser than the 8T. The speed of the cell can go lower, but the data efficient by the transistor is improved, which is defined using the constancy factor.

Table 2. Delay comparison

SRAM	6T	NC	8T	Isolated Static RAM
DELAY	17.94 ps	25.3 ps	31.62 ps	30 ps

4.4 Stability (Constancy) Factor

Table 3 shows the type of performance analysis done to

find the read and write ability. This is evaluated using the noise curve called (SNM).also determined using DC analysis undertaken to measure its noise factor [4]. From this noise, exactly how the considerable amount of voltages are accepted without lacking its data at the dc level in the structure is measured[15]. By calculating the curvature vtc, the (SNM) is also simulated using two highest graphical lines. The aligned samples are not useful in measuring the noise factor. It has some scientific measurement to define the data. By the Figure 7, Curvature-N gives, I and V together. Consider the three points (A, C, E) in the waveform output. The positive curve (i.e.) the change in voltage between (A and C) gives the voltage (SNM). The topmost point B between A and C is the current (SNM). The negative curve, the change in voltage between (C and E) provides the voltage during (WT) write mode. The bottom most point D between C and E gives current (WT). The write accessibility should also be improvised in the cell by assuming power and voltage at BL in low level. The constancy factor is analysed with the voltage of 1.8 in the technology of 180 nm. The corresponding value is tabulated (Table 3).

Table 3. Analysis of noise curve

SRAM	6T	8T	ISOLATEDSRAM
SVNM	270mV	303.6mV	310.28mV
SINM	15 µA	23 µA	30 µA
WTV	430 mV	564mV	754.2mV
WTI	-22 µA	-28 µA	-35 µA

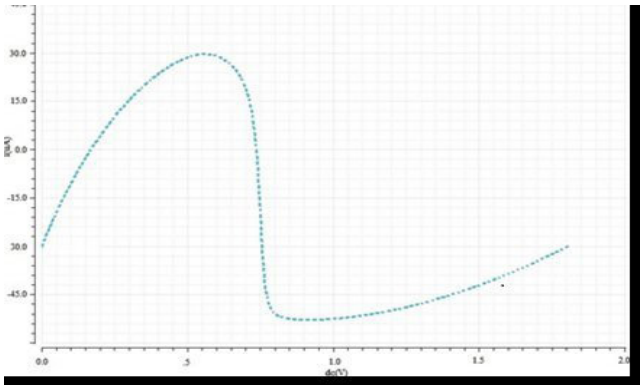

Figure 7. Noise curve for dynamic isolated read SRAM.

4.5 Leakage Current

As shown in Table 4, the dissipation of current and the power arises due to the channel scrambling. It is calculated at the read operation. The source terminal is in contact with the bit lines and the voltage applied is 0, so the amount of overflow current is analysed. Corresponding schematic is shown in Figure 8.

Table 4. Leakage current

SRAM	6T	ISOLATED READ SRAM
LEAKAGE CURRENT	8.056fA	5.592fA

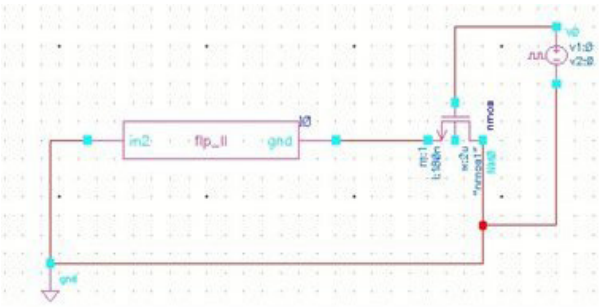

Figure 8. Schematic.

5. Conclusion

The isolated dynamic read SRAM is projected and the corresponding power analysis is made using the technology of 180 nm. The supply that has been used for this paper is 1.8v. By comparing to conventional 6T, and other SRAMs the power savings are acquired. Constancy factor is estimated using curvature-N analysis. In this analysis, the WTP, SINM, and SVNM are calculated and compared. The percentage of power indulgence is 90%, which is saved when related to 6T. 18% of power has been saved in isolated read SRAM while related to 8T. The percentage of curvature-N is enhanced by 2.15% of SVNM, 23% of SINM and 25% of WTP. Isolated dynamic read SRAM has attained the decreased power and overflow current and also enhances the stability.

6. References

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