Low Power Testing based on MOS Design Modified Flip-Flop

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Abstract

Flip-flops are basically data storage elements which can be used for storage of state. However, most non-volatile memory forms have limitations which make them unsuitable for primary storage. One of the disadvantages of existing flip-flop normal flip-flop based circuits and its computing is relatively high write energy to build up normal flip-flop based circuits. There is a need to reduce the consumption of powerand to write energy of flip-flop. Hence, we propose a design of low power normal flip-flop using modified CMOS technology. CMOS technology provides less noise ration during design. The proposed flip-flop design is based on MOS technology. Data store and restore operations can be performed. And in the proposed design performs in retaining data when electrical power fails or is turned off with low power consumption.

Keywords: CMOS Design, D Flip-Flop, Low Power

1. Introduction

Area, performance, cost and consistency are important concern in the past VLSI designing. Nowadays, area and speed concern which is comparing weight by increasing power. Normal D flip-flop is leading flip-flop in recent years and various schemes are being used to reduce the power. The consumed power is the mainly used by synchronous system in low power methods and some of the chip processing technologies also consuming power in low power technology. The proposed scheme is to consume power without concentrating state integrity and also performance in those flip-flop and latches. Flip-flop

Figure 1. CMOS design D flip-flop.

design is to minimize the power which is projected in this paper. Various changes are done and some changes have been proposed using by adopting CMOS based flip-flop. The proposed scheme of design is flip-flop; scan flip-flop and s27 design based on modified CMOS technology. The main idea of the design is to provide low power consumption and reduce delay.

2. Existing System

In existing work they proposed the design depends on flip-flop s27 and scan flip-flop mechanisms. Flip-flops are the non volatile memories. A class of dynamic circuit of flip-flop can be interfaced with dynamic and static. The results of flip-flop show significant saving energy and it operates at high speed. Comparison of simulation results it work on UMC 180 nm technology and it operates at 200 MHz the simulated results compared with previous results. The proposed design of flip-flop shows the reduction of power consumption 80% and increases the speed to 70-90%[1,2]. The design of pulse triggered low power flip-flop is presented. The control logic which has AND functions generates pulse wave form by using
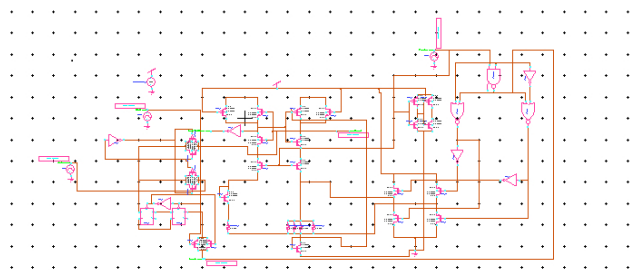
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pulse generation mechanism, Transistor size and pulse generation circuit is reduced by using speeder discharge operation. The simulation results based on UMC CMOS 90 nm Technology[3]. Compared to conventional flip-flop the Reduced Clock-Swing Flip-Flop (RCSFF) is reducing the delay and leak current by the factor of 20%. RCSFF is reduced the delay of RC along RC interconnect to one-half[3,4]. The novel four energy return clocked flip-flops these are enabled to recover from these clocking network, it saves the energy. It operates a single-phase sinusoidal clock. It can be generates with very high efficiency. TSMC can be 0.25 mum CMOS process, which implements 1024 proposed. H-tree clock network is recovering the energy by using the clock flip-flops and generating the sinusoidal clock. The simulation output shows 90% power reduced on the clock tree and the total power up to 83% power saved in comparison with the implementation of square wave clock scheme and base flip-flops and the [power can be saved 25% of multi chip[5]

Conditional capture and conditional pre charge technologies are classified by using high performance flip-flops. This classification is used to decrease the switching based on redundant mechanism. Here a new flip-flop is generated, that the flip-flop is Conditional Discharge Flip-Flop (CDFF). This CDFF technology which reduces the internal switching mechanism and generating glitches and to maintain the negative time setup. The future flip-flop is reducing the speed of flip-flop by 40%[6]. The hysteresis mechanism is used in the d flip-flop to improve the low performance.

The standard DFF, DICE FF and HDFF can be design in 28 nm CMOS technology and it exposed to neutron, alpha and heavy ion beams. It improves the neutron SER and alpha compared to basic D flip-flop[7]. The pass transistor and gate with two inputs can be given to clock pulse to reduce the discharge path and improve speed and reduces the complexity of circuit. Compared to conventional basic pulse triggered flip-flop, the pulse triggered flip-flop design can improve the speed and power delay product. The design can be generated in TSPICE CMOS 180 nm process[8]. For the design of flip-flops and the sequential circuits it can use conventional CMOS. Now here we can use pre settable adiabatic flip-flops then reduce the energy loss of the flip-flops. As compared to pre settable adiabatic flip-flop with sequential circuits the SPICE simulation result shows the emery loss reduction it reduced greatly when compared to conventional CMOS technology[9]. The basic and spatial hardening techniques in the flip-flop implementation for Single Event Upset (SEU) at

different supply voltages. They observed in three SEU tolerant flip-flop circuits for low supply voltage operation. The reduction of energy per transition can be compared with dual interlocked storage cell it can be based on flip-flop when the supply voltage can be operated at 1 V. These flip-flops can be fabricated and designed in low power commercial 90 nm CMOS technology[10]. Analog to digital converters high performance to require jitter low clock in order to get high resolutions at high speed operating frequencies. The D2S operation in the current modern as to minimize the trade-offs between power consumption and output jitter. Compared with different clock driver circuit with ultra low power jitter specifications are compared in 0.18 um commercial CMOS process[11]. The flip-flop can be a class of dynamic circuit of static and dynamic circuits. The basic flip-flop consumes power, as to reduce the power they designed the CMOS based D flip-flop. It reduces the power up to 80% and increases the speed up to 70-90%[12]. Single bit flip-flop can be compare with multi bit flip-flop and it reduces then timing and gate delay. The timing performance of single bit flip-flop and multi bit flip-flop can be simulated in Xilinx Vertex-5 family (XC5VLX50). The results can be favour of multi bit flip-flop for the reduction of clock network, clock buffer and gate delay[13].

2.1 Draw Backs

- Excess of logic gates used in existing system and normal flip-flop is used to design the s27 and scan flip-flop, which consumes amount of power.
- And requires relatively high energy to build up the normal flip-flop.

2.2 Flip-Flop

The data storage elements are flip-flops and latches and this storage is used to store the state, so they are called sequential logic. Flip-flops can be transparent or opaque or clocked synchronous or edge-triggered flip-flops. In previous flip-flop can be both simple and clocked circuits, now a day it is most preferable for considering clocked circuits. Quit they are called as latches.The D flip-flop consumes the power 4.9 nano watts with 2.9 seconds.

3. Proposed System

In the proposed system, the design of normal flip-flop using CMOS technology using MOS design. The MOS is for exchange of transmission and The MOS is applied to

the designed D flip-flop. Then the signal feed is applied to the D flip-flop. As the results, the power consumption will be reduced to the proposed design of flip-flop and focused on data transition to reduce the delay time. The proposed design replacing the blocks normal flip-flop. Hence the power consumption can be reduced by the proposed system.

3.1 CMOS Design Modified Flip-Flop

The structure of modified CMOS based flip-flop is shown in Figure 1. This flip-flop consists of MOS based structure. Power reduction can be done by the use of CMOS structure. The unwanted node transition can be avoided by allowing only different logic in two successive clock cycles with the help of these flip-flops.

In CMOS technologies, both NMOS and PMOS perform like as shown in above Figure. A MOS Swap is a derivative in which two counter terminal exchange current/voltage flows of one MOS terminal for those of the other MOS terminal. Specifically, two ends are agreed to exchange one stream of source (voltage/current) against another stream. The streams are called multiple combinational design of the MOS swap. The MOS swap defines the time when the flows are to be complete and the way to accrued and calculated.

The first thing is basic D flip-flop which it can be design with MOS swap CMOS technology. The MOS technology can be ultra low power, As it consume low power as well as the data store of write and readability the performance of system is good.

3.2 Advantages

- Design focused on both power and speed performance.
- And also which solves the long discharging problem during the data transition.

The S27 benchmark circuit can be designed instead of normal D flip- flop used the CMOS design modified D flip-flop can be shown in below figure3. The simulation results for the above designs are shown in figure2 and
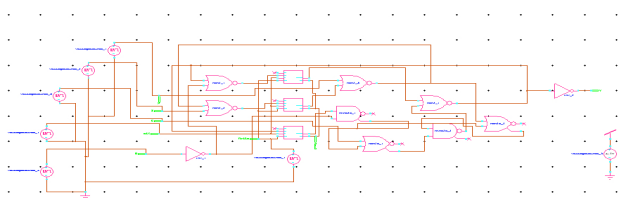

Figure 3. S27 proposed schematic

read, write and output variations are shown in figure4 respectively. The comparison can be made for the above designs are shown in table1 and table 2 respectively.

4. Simulation and Results

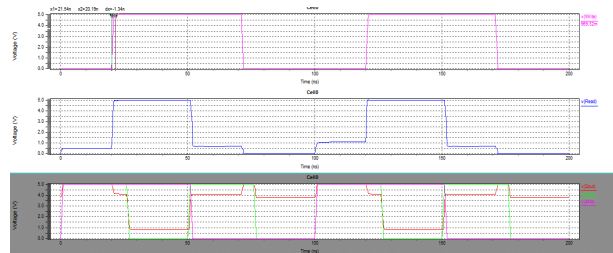The simulation results of above designs are show in below Tables and Figures.

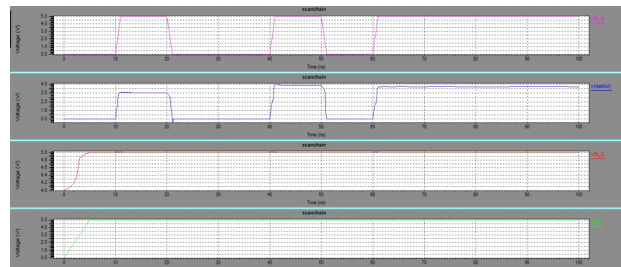**Figure 2.** CMOS design D ff read, write and output variations.

Figure 4. S27 proposed CMOS design waveform

Table 1. comparison of D ff and CMOS design D ff

	Power	Timing
D flip-flop	**4.7mw**	**2.9ns**
CMOS D flip-flop	3.2mw	2.1ns

Table 2. Comparison of S27 D ff and S27 CMOS D ff

	Power	Timing
S27 D flip-flop	**42.85nw**	**1.25ns**
S27 CMOS D flip- flop	**9.2pw**	**1.25ns**

Table 3. Comparison of Scan D ff and Scan CMOS D ff

	Power	Timing
Scan D flip-flop	**6.5μw**	**60ns**
Scan CMOS D flip- flop	**5.0μw**	**5.08ns**

Table4. S27 Scan CMOS D ff Power and Timing

	Power	Timing
S27 Scan CMOS D flip-flop	**0.1nw**	**10ns**

The power consumed by D ff is 4.7 mw, CMOS 3.2 mw, S27 D ff 42.85 nw, S27 CMOS D ff 9.2 pw, Scan D ff 6.5 uw, Scan CMOS D ff 5 uw, and S27 Scan CMOS D flip-flop 0.1 nw. By comparing all results, came to know that the power consumption of CMOS based designs is low.

5. Conclusion

In the paper, from existing design of normal flip-flop based on s27 benchmark circuit, scan flip-flop and s27 benchmark circuit with scan flip-flop based on normal flip-flop is proposed in the work with MOS technology, in the existing design that was based on logic gates and normal d flip-flop mechanism, but the proposed design provides promising result than existing system. The work concentrated on reduction of power and reduced delay, and also efficiency, thus from the overall parameters achieved better performance than existing design of flip-flop. For this design held in CMOS design methodology and used tanner EDA 13.0 as simulation tool to show the performance analysis.

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