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Low Power, High Speed 8-Bit Magnitude Comparator in 45nm Technology for Signal Processing Application

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Abstract

Design of a high speed magnitude comparator with minimal power consumption is essential for addressing the ever growing need of real time signal processing and data acquisition. Simultaneous optimization of speed and power constraints is the major design bottleneck associated with digital datapath design for higher word length processors. In this work, a novel architecture for 8-bit digital comparator is proposed which is directed at high speed signal processing without incurring significant power consumption. The principle of Parallelism has been successfully employed in the proposed architecture for reduction of overall power consumption without affecting the speed. The 8-bit comparator unit is realized using three different 1-bit comparator architectures proposed in this study and their performance analysis is carried out using several combinations of input vectors. The proposed topology is designed using pass transistor logic, static CMOS logic and transmission gate based logic which accounts for the improved performance metric as compared to the more commonly employed dynamic CMOS logic based designs due to relatively smaller data activity factor. The architecture is designed in 45 nm standard CMOS Process technology using Cadence EDA tool. The introduction of parallelism and use of modified 1-bit comparator topologies significantly lower the overall power consumption along with increasing the processing speed. The proposed design achieves average power dissipation of 196 nW and propagation delay of 129 pS for a power supply voltage of 1 volt. Performance metric associated with the proposed design shows a significant improvement in performance over similar architectures reported earlier in literature. Further improvement in performance can be achieved by introducing higher degree of parallelism into the proposed architectures.

Keywords: Comparator, Dynamic CMOS Logic, High Speed, Low Power, Pass Transistor Logic, Static CMOS Logic, Transmission Gate Based Logic

1. Introduction

The importance of a high speed and low power binary comparator is wide felt because of its extensive use in decoding of ×86 instructions. Furthermore, the incorporation of comparator units in to several stages of binary number comparison units in the iterative decoding algorithms of Multiple-Input-Multiple-Output (MIMO) communication systems has significantly increased the importance of high speed low power binary comparator architectures[1,2]. Conventionally, a comparator unit comprises of an equality detection unit and a chain of several Boolean logic gates for the comparison task. A high performance tree-structure comparator using All-N-Transistor (ANT) dynamic CMOS logic, proposed by Wang et al.[3], employs a parallel tree structure with two phase clock to increase the throughput. The comparator units of two adjacent layers are triggered by two out-of-phase clocks such that the individual outputs of respective comparator stages are efficiently pipelined without using extra sequential circuitry. The design, however, includes heavy pipelining stages and accounts for a large on chip area making it unsuitable for low power single cycle applications. A low voltage low power double tail dynamic

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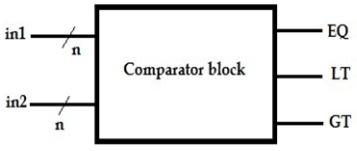
comparator is proposed by Lotfi and Babayan-Mashhadi[4], which employs a strengthened positive feedback during regeneration. The maximum clock frequency of the proposed comparator can be increased up to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153μW power, respectively. Upendra Soni et al. proposed a footed domino logic and current mirror based high speed leakage tolerant comparator[5] which is realized in UDSM Technology. A priority encoder based single cycled two phase comparator for high performance and power efficient arithmetic was proposed by Huang and Wang[6] which provided significant improvement in performance over the design presented by Wang et.al.[3]. Amit Grover presents a comparison between GDI and TG based power reversible comparator designs using 90nm and 180 nm process technology by Grover[7]. Design of Low Power and High Speed Comparator with sub-32-nm Double Gate-MOSFET is presented in Bhumireddy et.al.[8]. Chuang, Li and Sachdev proposed a single-cycle 64-bit binary comparator utilizing a radix-2 tree structure, specifically for static logic to achieve both low-power and high-performance operation, particularly at low-input data activity environments[9]. Lu and Holleman presented a low power high precision comparator with time domain bulk tuned offset cancellation[10]. The design has been fabricated in a commercially available 0.5 micron process technology. The offset cancellation scheme utilised in the topology does not introduce observable offset or noise, and can achieve fast and robust convergence with a wide range of common mode input, as reported by the authors. The novel comparator architecture presented by Kim and Yoo[11] utilizes Bitwise Competition Logic (BCL) to detect the earliest first "1" away from the MSB after pre-encoding the inputs. Perri et al. propose a new efficient architecture[12] for the design of fast low-cost single-clock-cycle binary comparators.

Most of the works related to comparator architectures reported in literature make use of dynamic CMOS logic to achieve high-performance. Though the use of dynamic logic has resulted in superior performance, as compared with static logic, it is certainly not suitable for low-power operation because the high data activity factor associated with it. In this paper, a new architecture for 8-bit binary comparator is proposed based on static CMOS logic. This design is implemented with pass transistor logic, static CMOS logic and Transmission Gate (TG) based logic[13,14] to ensure low-power consumption. The proposed work is realized in Cadence EDA tool in 45 nm CMOS process technology. The proposed static logic implementation of the comparator unit achieves improved performance compared to state-of-the-art designs. The lower data activity factors associated with static CMOS logic ensures that the proposed comparator architecture results in significant energy efficiency. The rest of the paper is organised as follows. Section 2 reviews the basic structure of a binary comparator unit. Section 3 introduces and explains the proposed comparator implementation. Section 4 describes the simulation setup and presents the performance analysis. Section 5 concludes the discussion.

2. Comparator Fundamentals

The basic logic structure of a binary magnitude comparator involving two n-bit numbers is shown in Figure 1. The comparator block takes two n-bit numbers, in 1 and in 2, as inputs and results in three distinct outputs, conventionally[15]. The EQ, LT and GT signals shown in the figure correspond to the conditions when in1 is equal to in 2, in1 is less than in 2 and in 1 is greater than in 2, respectively. At any instance of operation, either of the three output signals is active high or active low depending on the architecture, representing any one of the three possible outcomes of a comparison process, as represented in Figure 1.



	EQ	LT	GT
in1 = in2	1	0	0
in1 > in2	0	0	1
in1 < in2	0	1	0

Figure 1. Conventional Comparator block diagram and logic of operation.

The equality detection unit embedded in basic comparator architectures usually comprise of a chain of xnor gates. The use of xnor gates for equality detection is evident from the fact that an xnor gate results in an active high output when all of its inputs are equal, resulting in a coincidence logic. The EQ output of an n-bit comparator is high if and only if both the inputs are bitwise equal, i.e. all the n-bits of in1 are equal to the corresponding bits of in2. In such a scenario, the LT and GT outputs are attain logic level zero. The condition 'in1> in2' results in the GT output being pulled up to logic level one and the other two outputs being active low. Such a condition can be realized by any of the following means: if the MSB of in1 is

greater than the MSB of in2, then irrespective of the status of the remaining (n-1) bit pairs, in1 is greater than in2; if the MSB pair in both the inputs are equal and the next significant bit of in1 is greater than the corresponding bit of in2, the also in1 is greater than in 2; and so on. The LT signal at the output is turned active high if in1 is less than in 2. In such a scenario, the EQ and GT output lines attain logic low. As mentioned for the in1 > in2 case, the in1< in2 case can also be realized for several input combinations.

3. Proposed Comparator Architecture

The paper proposes three architectures for 8-bit magnitude comparator based on pass transistor logic, TG based logic, precharge-evaluation logic and static CMOS logic[13]. The proposed architectures are realized in 45 nm CMOS process technology using Cadence EDA tool. Prior to developing the proposed high speed low power architectures based on static CMOS logic, a novel topology for 8-bit comparison is developed based on bit wise comparison technique based on precharge-evaluation logic analogous to the dynamic CMOS logic.. The topology, presented in the paper as 8-bit comparator architecture 1, is found to provide high speed arithmetic with the power dissipation being on the higher side corresponding to the higher data activity and switching issues associated with dynamic logic.

3.1 Magnitude Comparator Architecture 1

The 8-bit magnitude comparator architecture 1 is based on the precharge-evaluation logic and essentially is a bitwise comparator assembly. Two 8-bit operands a and b, as shown in Figure 2, are compared at every bit position using 1-bit comparator units and the results of these bitwise comparison stages are accumulated to predict the overall comparison result. The 1-bit comparator unit used for the proposed topology is a 9T design as presented in Figure 2.

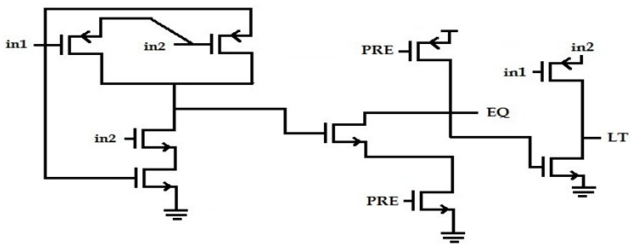


Figure 2. 1-bit Magnitude Comparator 1.

In the 1-bit magnitude comparator architecture, the equality condition of the two inputs (in 1 and in 2) is represented by the EQ signal being active high and the LT signal being pulled down to 0. For the case when the two inputs are not identical, the EQ signal attains low level output voltage while the LT signal achieves logic 1 or logic 0 depending on whether in1 is less than in2 or in1 is greater than in 2, respectively. The overall operation of the design is divided in to two phases: precharge and evaluation, as in the case of dynamic logic circuits. In the precharge phase (PRE = 0), the EQ output is pulled up to logic 1 (Vdd) using the pull up transistor controlled by the PRE input and the LT terminal is pulled down to logic level 0 by the pull down NMOS transistor driven by EQ signal. Thus essentially LT is said to be pre-discharged. In the evaluation phase (PRE = 1), the pull up transistor is cut off and the state of the output signals EQ and LT are decided by the two inputs. The inequality of in1 and in2 is evaluated using a 4T xor arrangement which drives the EQ signal value in the evaluation phase. If in1 is not equal to in2, then the xor logic output goes to 1 and the EQ output is pulled down eventually. This operation is not enabled in precharge phase as the pull down path is controlled by an NMOS transistor driven by the PRE input and hence, the EQ output can only be pulled down in the evaluation phase when the two inputs are unequal. The pre-discharged LT signal stays in the same state as long as the condition in1< in 2 (i.e. in1 = 0 and in2 = 1) is not satisfied. In such a condition, LT is pulled up to logic level 1 by the pull-up PMOS transistor driven by in1. The condition when both the output signals are pulled down to 0, essentially represents the fact that in1 is greater than in 2. However, the circuit operation is limited to a single evaluation in the evaluation phase. If the EQ signal is pulled down for some input combination, then it can't be pulled up again in the same evaluation phase as no pull up path exists in this phase of the circuit operation. Similarly, if the LT output is pulled up in the evaluation phase, then it cannot be pulled down when the necessary condition arises in the same evaluation period. This operation is analogous to the conventional CMOS dynamic logic theory which ensures only a single logic operation in the evaluation phase. This approach is significant to control the high data activity factor associated with conventional dynamic logic as in the precharge phase, the switching of EQ signal from 0 to1 is not obligatory, rather it depends on the state of the signal. If and only if EQ signal is at logic 0 at the end of the evaluation phase, then only such a

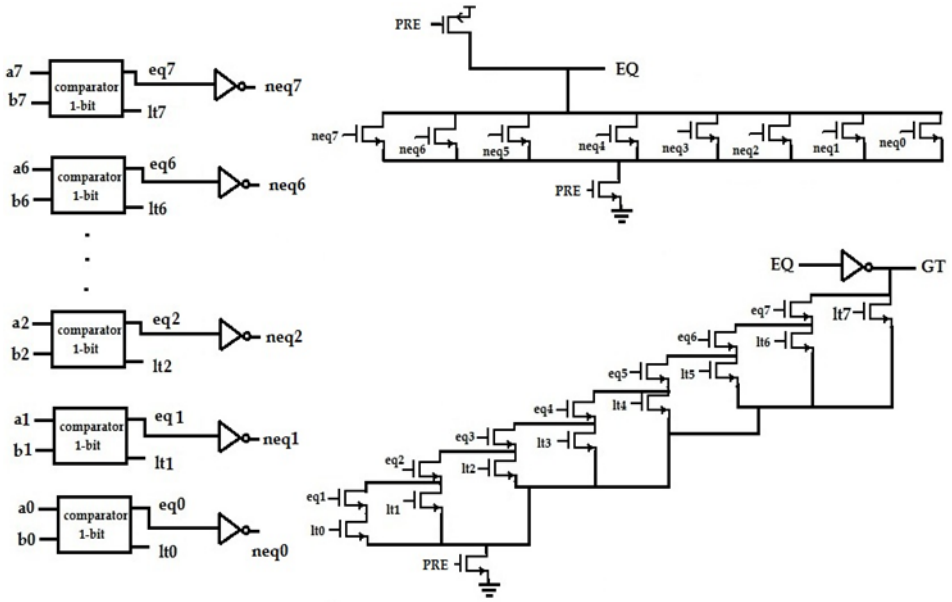


Figure 3. 8-bit Magnitude Comparator 1.

switching is performed. Thus the data switching activity is dependent upon the input combination in the evaluation phase. However issues like charge leakage and charge sharing[13] may still contribute to higher dynamic power dissipation by introducing unwanted switching activities at the EQ node in the precharge phase.

The bitwise 8-bit magnitude comparator architecture1, shown in Figure 3, makes use of two distinct output signals EQ and GT, to represent the comparison process. The equality condition of the two inputs a and b is represented by the EQ signal being at logic 1 and the GT signal being at the low logic level. The inequality condition is demonstrated by the EQ signal being pulled down logic level zero. The GT signal, in such a situation, stays at logic level zero if a is less than b and it is pulled up to logic 1 if a is greater than b. The overall operation of the 8-bit comparator is carried out in two phases: Precharge and Evaluation. In the precharge phase (PRE=0), the EQ signal is charged to Vdd and the GT signal is pulled down to low level logic. The evaluation phase is initiated with the PRE signal being 1. In such a situation, the EQ signal stays at the precharged state if and only if all the individual bit pairs of the two inputs are equal. Inequality condition in any of the bitwise comparator stages is represented by the individual neq signal being 1 which pulls down the EQ signal via the pull down NMOS transistors. Because of the static CMOS inverter arrangement, the GT signal is pulled up to Vdd once the EQ signal is grounded representing the inequality criteria. The GT signal stays at logic level 1 indicating a being greater than b, unless the pull down NMOS network controlled by the lt and eq signals from the individual bitwise comparator blocks is active. For the condition when a is smaller than b, the pull down NMOS arrangement drags the GT signal to logic level 0. In the worst case scenario, when the two inputs a and b are equal on all the bit positions except for the least significant bit pairs (a0 and b0), then the pull down network has 8 NMOS transistors in series resulting in larger propagation delay. An ambiguous situation occurs in the case of inequality of the two inputs when GT is to be pulled down to 0. In such a case, the voltage level at GT terminal is essentially controlled by the relative strengths of the charging current (flows via the PMOS transistor driven by EQ) and the discharging current (that flows through the pull down NMOS arrangement). Thus the corresponding voltage swing at the GT terminal is not ideal as it attends a somewhat intermediate level. The performance evaluation of this comparator topology is presented in section 4.

3.2 Magnitude Comparator Architecture 2

This architecture for comparing two 8-bit numbers is also based on bitwise comparison logic. The two inputs are compared bitwise at each of the 8 bit positions using a new 1-bit comparator design shown in Figure 4. The 1-bit comparator architecture 2 developed for this 8-bit

comparator topology is a 9T design that incorporates a 6T xor-xnor design[16] for equality detection. The EQ output in the figure is high when both the input bits are equal. The NEQ output presented in the topology is merely the negation of the EQ signal, which indicates the state of inequality. The LT terminal in the topology represents the condition when in1 is less than in 2. As shown in Figure 4, LT signal is at logic low if EQ and/or in1 are logic high, as both the conditions suggest in1 cannot be less than in 2. Only for the input combination of in1 is being logic zero and in 2 being logic one, the LT signal displays logic one indicating the 'in1 less than in 2' condition. The condition when both EQ and LT signals are at logic zero is inferred as in1 being greater than in 2.

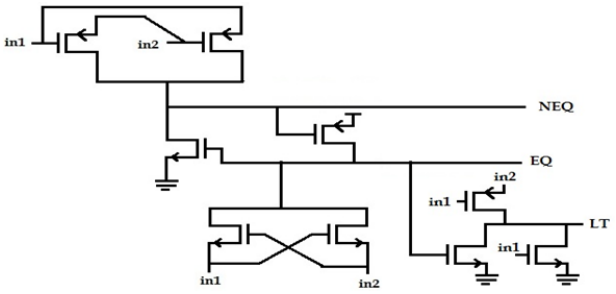


Figure 4. 1-bit Comparator Architecture 2.

The 8-bit comparator architecture 2 is realized by instantiating the 1-bit comparator block eight times, once for each of the bit positions and the resulting topology is shown in Figure 5. As shown in the figure, the EQ output for the architecture is logic high only if all the 'neq' (shown as NEQ in the 1-bit comparator presented in Figure 5 outputs of the bitwise comparator modules are logic zero simultaneously. If any of the 'neq' signals attain logic 1, the EQ signal goes to logic zero indicating the condition of inequality. The GT output signal is modelled as the negation of EQ output, using an inverter. Whenever the equality condition is enabled, i.e. EQ = 1, then the GT signal is forced to logic zero, as desired. If the equality criterion is not satisfied, the EQ signal goes to logic zero there by forcing the voltage at GT terminal to logic 1. The GT terminal voltage stays as active high indicating in1 being greater than in2, unless the arrangement of pull down NMOS transistors force it down to logic zero, indicating a condition where in1 is less than in 2. As mentioned in section 1, the voltage level at GT terminal in such a condition is determined by the relative strengths of the conflicting charging and discharging currents. A close observation of the architecture in Figure 5 shows there are at least 8 transistors connected in series in the worst case operation (8 NMOS transistors in the pull down arrangement at GT terminal and 8 PMOS transistors in the pull up arrangement at the EQ terminal), which is highly unacceptable as far as the speed of operation is considered.

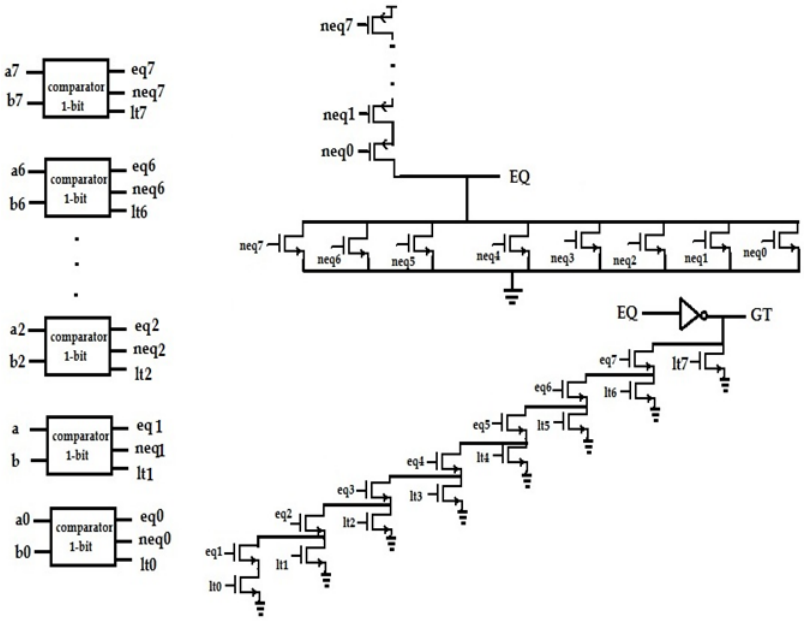


Figure 5. 8-bit comparator architecture 2.

3.3 Magnitude Comparator Architecture 3

The modified architecture for low power and high speed magnitude comparison is realized by using two 4-bit comparator modules that operate in parallel, one for the higher nibble and the other for the lower nibble of the 8-bit operands. Each such 4-bit comparison module makes use of a new 1-bit comparator block for the MSB stage.

The new topology for 1-bit comparison is a 7T design as shown in Figure 6. This modified 1-bit comparator includes two output signals, Gt_n and Lt_n, for the n^{th} bit stage comparison, with A_n and B_n being any two arbitrary inputs. The signal Gt_n goes to logic one if A_n is greater than B_n and the signal Lt_n goes to logic 1 if A_n is smaller than B_n. The condition of equality is demonstrated by both the Gt_n and the Lt_n signals being pulled down to logic zero. It is worthwhile to mention that the signals Gt_n and Lt_n do not realize rail-to-rail swing because of the pass transistor arrangement.

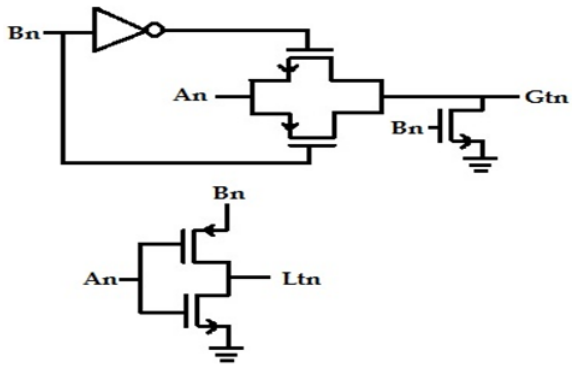


Figure 6. 1-bit Comparator 3.

The subsequent stages of the comparator are realized using the *i^{th} stage comparison unit* which is presented in Figure 7. The i^{th} stage comparison depends upon the operand values at the i^{th} bit position as well as the comparison results of the previous bit position. The operation of this unit is demonstrated in Table 1.

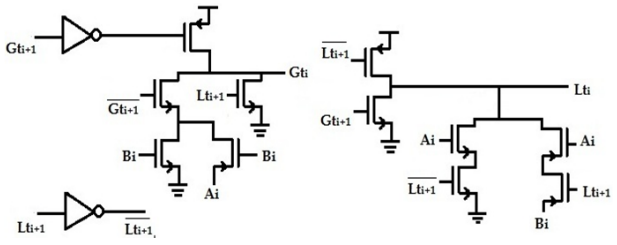


Figure 7. i^{th} stage comparison unit.

Table 1. Operation of the i^{th} stage comparison unit

Gti+1	Lti+1	Gti	Lti
1	0	1	0
0	1	0	1
0	0	0, for Ai<=Bi 1, for Ai>Bi	1, for Ai<Bi 0, for Ai>=Bi

The Gt and Lt notations used in this i^{th} stage comparison unit stand for 'greater than' and 'less than' respectively (relevance is self-explanatory) and the subscripts refer to the bit position to which they correspond. The Gt_i signal does not depend upon the i^{th} stage inputs, A_i and B_i, as long as the condition of inequality holds good in the higher bit position, designated here as the $(i+1)^{th}$ stage. If the Gt_{i+1} signal is at logic 1 (indicating A_{i+1} being greater than B_{i+1}), then irrespective of the i^{th} stage inputs, Gt_i is pulled up to Vdd and Lt_i is pulled down to 0, implying A being greater than B. Similarly, If the Lt_{i+1} signal is at logic 1 (indicating A_{i+1} being smaller than B_{i+1}), then irrespective of the i^{th} stage inputs, Gt_i is pulled down to 0 and Lt_i is pulled up to Vdd, implying A being smaller than B. The state of the two signals are determined by the i^{th} stage inputs only when both Lt_{i+1} and Gt_{i+1} signals are at logic level zero indicating a state of equality at the $(i+1)^{th}$ bit position. In overall operation of the i^{th} stage comparison unit is explained in Table 1. The i^{th} stage comparison unit incorporates several precautionary arrangements to ensure smaller power consumption. The i^{th} stage inputs, though arrive at the same time as all other stage inputs, do not induce any logical operation as they are cut off from the i^{th} stage outputs Gt_i and Lt_i, via transistors driven by the $(i+1)^{th}$ stage outputs. Hence prior to the arrival of the $(i+1)^{th}$ stage outputs, any data activity in the i^{th} stage input does not propagate to the corresponding outputs. As indicated in Table 1, the i^{th} stage inputs mostly affect the switching of the ith stage outputs if both the previous stage outputs are at logic level zero. Thus the switching probabilities of the i^{th} stage outputs are largely reduced resulting in a small dynamic power reduction. The modified 8-bit magnitude comparator for high speed and low power applications is presented in Figure 8. The topology incorporates two stages of four bit comparator units operating in a parallel manner. The parallel arrangement results in a critical path that consists of one 1-bit comparator and three i^{th} stage comparison units, which does not introduce any unacceptable latency.

The 8-bit magnitude comparator, shown in Figure 8,

compares two arbitrary 8-bit inputs (A and B) and the result of comparison is approximated using two outputs, GT and LT. The 1-bit comparator block used in the four bit comparator arrangement for the higher nibbles of the two operands takes the most significant bits of the two operands (A7 and B7, as shown Figure 8) as inputs while the 1-bit comparator used in the other four bit comparator array (for the lower nibble) accepts the most significant bit of the lower nibble of the two operands (A3 and B3) as inputs. The signals Gt_4 and Lt_4, as shown in the figure, are used to indicate the comparison results of the most significant four bits of the two operands, while the comparison results for the lower nibble of data is modelled using Gt_0 and Lt_0. The fact that the upper four bits of the operand A is greater than the corresponding four bits of the operand B is represented by the signal Gt_4 being pulled up to logic level 1 and Lt_4 being pulled down to the lower logic level. The opposite polarity of the two outputs holds good for the case when the higher nibble of A is smaller than that of B. the case of equality of the higher four data bits of the two operands is modelled by pulling both Gt_4 and Lt_4 signal voltages to logic level zero. It is to be noted that under no conditions, the normal operation of the topology assumes both the Gt_4 and Lt_4 signals being at logic level one simultaneously. A similar analogy can be provided for Gt_0 and Lt_0, the only modification being they correspond to the comparison of the least significant four bits of the two operands.

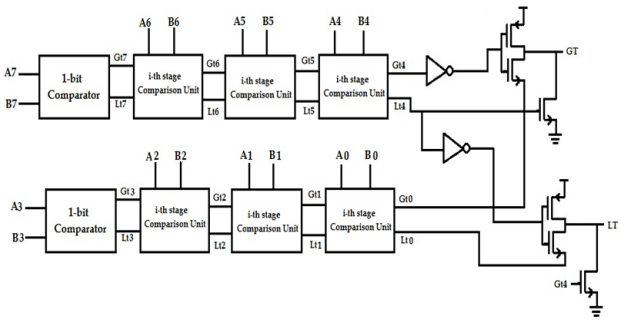


Figure 8. 8-bit magnitude Comparator 3.

The overall operation of the 8-bit comparator stage can be summarized as follows. If Gt_4 is at logic level one, indicating the higher nibble of A is greater than that of B, it pulls up the GT signal to logic 1 and pulls the LT signal down to logic 0, irrespective of Gt_0 and Lt_0, indicating A>B. In an identical manner, if Lt_4 is at logic 1, it results in LT being logic 1 and GT being logic 0, irrespective of the outputs of the lower nibble comparator, indicating A<B. If both Lt_4 and Gt_4 are logic zero, it is inferred that the higher order four bits of both the operands are equal to each other. In such a case, the values for GT and LT are determined by Gt_0 and Lt_0, as shown in Figure 8. The voltage level at the GT terminal for the condition Gt_4 being 0, Lt_4 being 1 and Gt_0 being logic 1 is marked by the relative strengths of two currents, one charging current flowing due to Gt_0 through the NMOS transistor driven by Gt_4 and one discharging current flowing through the pull down NMOS transistor driven by the Lt_4 signal. Such a path induces some unwanted larger short circuit power dissipation and also results in non-ideality in the output swing at the GT terminal. A similar situation can be analysed at the LT terminal for the Lt_4 signal voltage level being at logic 0, Gt_4 being at logic 1 and Lt_0 being at logic 1. In the proposed architecture, the output signals GT and LT do not attend rail-to-rail voltage swing. Because of the pass transistor arrangement, the swing is limited to Vdd-Vtn level (Vdd being the supply and Vtn being the nmos threshold voltage) instead of being complete logic 1. The condition of equality of the two operands is represented both GT and LT signals being pulled down to logic zero.

4. Simulation Results and Performance Analysis

The proposed comparator architectures are realized in 45 nm CMOS process technology using Cadence EDA tool. The performance evaluation is done by subjecting the topologies to various combinations of input vectors. The layout for the proposed high speed low power comparator (architecture 3) is realized using the Layout XL editor of the Cadence EDA tool for performing the post layout simulation. The effectiveness of the topology is analysed both for the pre-layout and the post-layout stages, for a power supply of 1volt. The results are tabulated in Table 2 to 4. Table 2 enlists various performance metrics of the 8-bit comparator architecture1 presented in Figure 3. The transistor count associated with the design is 116, resulting in a compact topology and smaller on chip area requirement. The propagation delays from input to EQ output terminal and from input to GT output terminal are mentioned separately. The delay associated with the topology yields a satisfactory performance as compared to the state-of-the-art reported in the literature. However, the power dissipation associated with the architecture is 14 μw for a power supply of 1 volt. This high value

of the power dissipation is accounted for the use of dynamic logic technology which introduces a high data activity probability (due to switching of the output voltage levels in every precharge phase). The transistor count, propagation delay and average power dissipation values associated with the 8-bit magnitude comparator architecture 2 are tabulated in Table 3. The topology utilizes fewer transistors as compared to the dynamic logic based architecture and hence results in a more compact topology. The propagation delay values associated with this architecture also indicate an improved performance metric. The use of static CMOS logic significantly reduces the average power dissipation, as compared to the 8-bit magnitude comparator architecture 1.

Table 2. Performance Analysis of 8-bit Comparator architecture 1

Name of the topology	Transistor Count	Propagation delay		Power dissipation
8-bit comparator architecture1	116	Input-EQ Input-GT	73.29 ps 95 ps	14 µw

Table 3. Performance Analysis of 8-bit Comparator architecture 2

Name of the topology	Transistor Count	Propagation delay		Power dissipation
8-bit comparator architecture2	105	Input-EQ Input-GT	48.61 ps 66ps	1.426 µw

Table 4 summarizes the performance of the proposed 8-bit magnitude comparator architecture3 for a power supply of 1 volt. The pre-layout propagation delay and power dissipation account for the performance without considering the physical parasitics. As evident from the data, the propagation delay for the modified topology has undergone an approximate two fold increase as compared to the previous architecture. However, the power dissipation associated with the topology is reduced significantly, resulting in a much better performance. The post-layout propagation delay and power dissipation values account for the performance in presence of the physical parasitics.

Table 4. Performance Analysis of 8-bit Comparator architecture 3

Name of the topology	Transistor Count	Propagation delay (in ps)		Power dissipation (in nw)	
8-bit magnitude comparator3	114	Pre-layout	129.6	Pre-layout	196
		Post-layout	436	Post-layout	641.8

Table 5. Comparison of performance with state-of-the-art

Name of the topology	Technology	Propagation delay (in ps)	Average power (in µw)
[5]	45 nm	231	277.01×10^3
Low power design[17]	100 nm	392	82.4
High speed design [17]	100 nm	175	200
[18]	HSPICE Simulation	22.29	0.876
[19]	SPICE Simulation	29.2	5.45
[20]	120 nm	-	109
[21]	65 nm	57	-
Proposed Magnitude Comparator architecture1	45 nm	95	14
Proposed Magnitude Comparator architecture2	45 nm	66	1.426
Proposed Magnitude Comparator architecture3	45 nm	129.6	0.196

The performance of the magnitude comparator architectures proposed in the paper is compared to several eminent topologies reported in the literature. The comparison results are tabulated in Table 5. The high speed low power topology realized with footed domino logic in 45 nm Technology accounts for a propagation delay of 231 pS. However the power dissipation associated with the topology is in the high mille watt range.

The low power design presented in[17] accounts for a propagation delay of 392 pS with a power dissipation of 82.4 µW. The high speed design presented by the same researchers in[17] results in a propagation delay of 175 pS. However this improvement in speed comes at the expense of a larger power dissipation of 200 µW. The performance analysis for the architecture presented in[18] demonstrate a fairly improved result as compared to that of the above two topologies.

The propagation delay associated with the topology is 22.29 pS with a power dissipation of 876 nW. The performance of this architecture is much better as compared to the first two 8-bit comparator architectures presented in this thesis work. The architecture presented in[19] accounts for a small propagation delay (29 pS), however the power dissipation is very high compared to the topology presented in[18]. The power dissipation associated with the magnitude comparator design presented in[20] is 109 µW, which is much higher than most of the topologies reported in the literature. The architecture presented in[21] accounts for a delay of 57 pS for the 8-bit comparison process with the topology realized in 350 nm Technology. The propagation delay and power dissipation values for the proposed magnitude comparator1 are very high as compared to the topologies presented in[17,18,21]. This result is accounted to the use of dynamic CMOS logic style for realization of the topology. The magnitude comparator architecture 2 presented in the thesis work presents significantly lower power dissipation and some improvement in propagation delay over the dynamic CMOS based topology. The power dissipation associated with this architecture is comparable to that of the topologies presented in[18,19]. The low power and high speed magnitude comparator architecture3 proposed in this work provides significant improvement in the overall power dissipation. The topology results in a power dissipation of 196 nW, which is nearly a fivefold improvement over the topology presented in[18]. The power dissipation for the proposed topology is 27 times smaller than the architecture reported in[19]. A close inspection of the tabulated data clearly indicates the effectiveness of the proposed architecture with respect to low power arithmetic. However, the improvement in power consumption is achieved at the expense of a larger propagation delay. The propagation delay associated with the design has undergone a fourfold increase as compared to the topology reported in[19]. However, because of the improvement in power dissipation, the overall performance offered by the proposed topology much better compared to several other architectures reported in the literature.

5. Conclusion

The paper proposes a novel architecture for 8-bit magnitude comparison. The architecture is based on pass transistor logic, static CMOS logic and TG based logic and is realized in 45 nm CMOS process technology using Cadence EDA tool. The layout for the proposed topology is developed using the Layout XL editor of the Cadence EDA tool, using Virtuoso platform. The performance analysis was carried out with different test vectors for a supply voltage of 1 volt and the results are tabulated. The comparative analysis presented in Table 5 demonstrates the effectiveness of the proposed architecture against the state-of-the-art. Further improvement in performance can be achieved by introducing higher degree of parallelism into the proposed architectures. It can be modified for improved speed characteristics by realizing the four bit comparator blocks using two 2-bit comparator arrangements that operate in parallel.

6. References

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