

Computational Optimization of Placement and Routing using Genetic Algorithm

S. Nazeer Hussain* and K. Hari Kishore

KL University, Green Fields, Vaddeswaram, Vijayawada, Guntur - 522502, Andhra Pradesh, India;
nazeerhussain45@gmail.com, kakarla.harikishore@kluniversity.in

Abstract

In the VLSI chip designing process, Floor-planning is one of the vital stages which in turn have Placement and Routing tasks. This paper concentrates on solving the problems which occur in VLSI floor planning and gives an overview of placement and routing problems in ICs. This approach depends on recursive optimization prototypes with redefined algorithm. The searching for best solutions is carried out by Genetic Algorithm (GA) on each iteration since these algorithms is already known and proven to solve similar type of problems. GA has been tested randomly and is simulated. By conducting experiments on GA we can realize optimized solutions for the above said problems.

Keywords: Field Programmable Gate Arrays (FPGA) Placement, Genetic Algorithm (GA), VLSI Design

1. Introduction

Field Programmable Gate Arrays (FPGA) is a reconfigurable device used to implement any digital system application. VLSI Design engineer can able to reconfigure it for various digital applications based on computer aided design flow. There is various design steps involved in the process.

In circuit design, placement is one of the crucial steps. Modules and its elements are placed in distinct locations in placement. Placement step takes the most time in design of chip. So, fast response and better algorithms are preferred to meet the requirements. In current modern layouts, the transistor number is increasing and element size is decreasing making surface area becoming very small, which means that space of modules should be minimized. In physical design, the layout structure is mapped with surface of the chips by Placement.

In Computational aspect, placement problem is a very difficult and is considered as NP-complete problem. So, it cannot be dedicated with a unique answer and different algorithms are to be checked to get a set of answers for solving the requirements of the design. The Structure of applied algorithms is heuristic nature. If a circuit consists of modules of different sizes the VLSI placement becomes more complicated.

Optimization algorithms for placement of the cells can be categorized into the following:

- **Analytic algorithms**
Computations are the basis for the techniques used for optimization in this section. Most parameters and functions are represented in mathematical formula and the process of optimization is then implemented according to the above method for getting optimal values. Methods described in³ fall in this list. Module overlapping is one major consideration in this technique. Also the possible solutions are also represented in mathematical format.
- **Partitioning based algorithms**
Many of placement algorithms can be sorted in this part. Each module of problem gets divided into number of sub modules and the algorithm for optimization is applied separately for each one of the modules. A method that is based on division and replacement was introduced that concentrates on wiring parameters in².
- **Evolutionary Algorithms:**
Random answers are offered in optimization process with these kinds of algorithms. Simulated Annealing algorithm is the most applicable one in placement of cells in this

* Author for correspondence

section. The principle of this algorithm is explained in the model used in⁴. Mean Field Algorithm is brought up in⁵. In this paper, VLSI placement algorithms comparison is presented. SA algorithm simulates the problem to the annealing process (melting metal and slowly cooling it). Module placement is carried out parallel with cooling process. The Algorithm is constituted with numerous movements which lead to temperature changes and the corresponding parameters. Every such movement is acceptable if the cost decreases, this process will continue until a reasonable cost as well as a stable state is achieved. The major problem with this algorithm is its run time, and also it requires laborious cost functions to have a proper placement. The other algorithm which is much faster is Mean field annealing which is based on neural network basis and again cooling process. In this, the surface of chip to equal squares. Wire length has direct effect on power consumption. The smaller wire length cost, the more economical circuits they are. On the other hand, overlaps make the IC design with lot of fabrication as well as their routing problems hence its optimization is required.

2. Methodology

2.1 Design Flow of FPGA Based System Design

An FPGA⁶ based digital system design flow is shown in Figure 1.

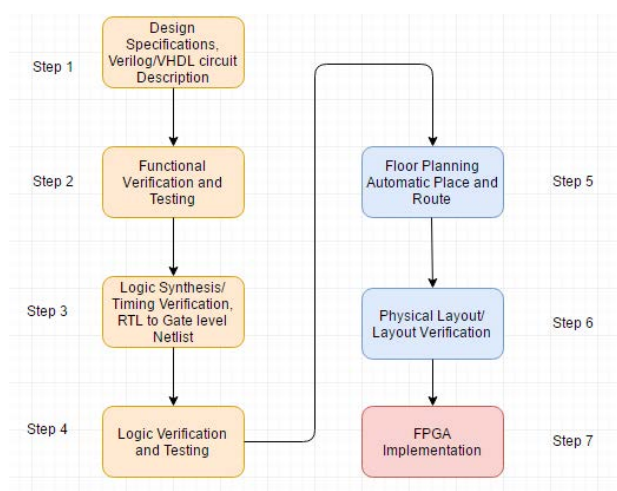


Figure 1. FPGA based digital system design flow.

The step1 gives the complete description of the functionality of design. Behavioral description is often

written using Hardware Description Languages such as VHDL or Verilog. In step 2 various Simulation vectors are applied as inputs to the test bench, to perform functional verification and testing of the design. The RTL description is converted into net list in step 3. The detail of the logic gates and its interconnection in the circuit is contained by Netlist. The process is called Logic Synthesis Step4. Gate level Netlist is given as the input to a Placer and Router in Placer and Router phase. Next Step to placement is the physical Layout and its verification where many issues are yet to be solved. Final step includes downloading the layout information into FPGA. Factors like wire length, delay, area and power are considered as constraints for Placement.

2.2 Architectural Details of FPGA

One can implement any kind of digital system or circuit by electrically programming the prefabricated silicon device called FPGAs. FPGAs possess number of advantages over ASIC design such as Re-configurability, fast turn and low complexity. The architecture of FPGA consists of array of Logic cells surrounded by the Switch blocks, Connector matrix and I/O Pads. The logic cells in a FPGA will be of same type in Homogeneous FPGAs where as in heterogeneous FPGAs, various special purpose blocks like memories, adders and multipliers also included apart from the logic cells and I/O Pads. Programmability is defined as changing the behavior of pre-fabricated chip as per the system design. Programming Technology differ the FPGAs available outside. The architecture of Homogeneous FPGAs is shown in Figure 2.

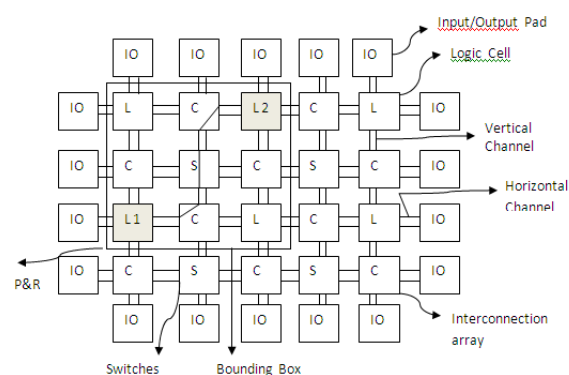


Figure 2. Flow chart of contents.

2.3 Genetic Algorithm

The genetic algorithm¹ is a method of solving optimization problems which are based on natural selection, the process

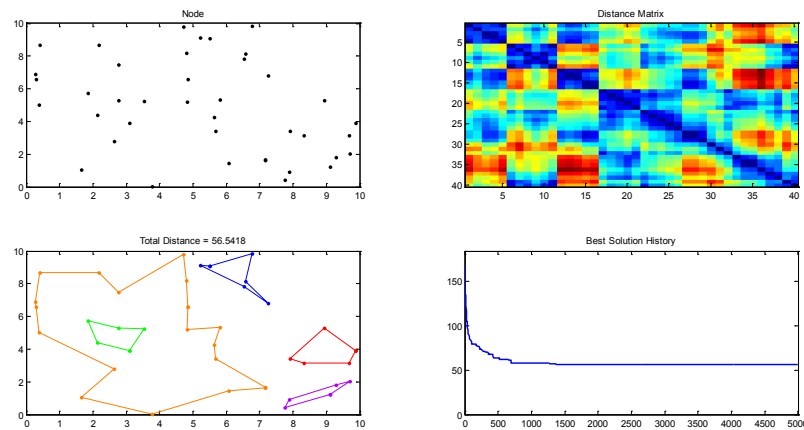


Figure 3. Placement of CLB using GA.

that drives biological evolution. At every step, the genetic algorithm selects individuals at random from the current population to be parents and uses them to produce the children for the next generation. Over successive generations, the population “evolves” toward an optimal solution. Here each individual in the population of GA represents a sequence of actions, which, if applied to the prototype floor-plan, creates another floor-plan.

- **Fitness Function**

The negative amount of unused area is called fitness value that is the total area of the enclosing rectangle without the area of placed modules.

- **Selection**

To select a parent, the selection procedure used is Roulette selection procedure. By simulating the roulette wheel the above process chooses the parents. In which the area of the section of the wheel corresponding to an individual is proportional to the individual's expectation. To select one of the sections with probability which is equal to the area, a random number is used by the technique.

- **Mutation**

The options in mutation specify how good the genetic algorithm makes changes randomly in the individuals to generate mutation children. Also the Mutation allows GA to provide genetic diversity and a broader space to search. This paper proposes uniform mutation method. This includes two processes. First, the algorithm selects a fraction of the vector entries of an individual for mutation, where each entry has a probability Rate of being mutated.

In the second step, the algorithm replaces each selected entry by a random number selected uniformly from the range for that entry.

3. Results and Discussions

The fitness function for a placement problem is calculated based on minimization of metrics, denoted as equivalent distance. Here CLB's are shown from left, corresponding x and y co-ordinates are derived for the logic blocks by using genetic algorithm. Figure 3 shows CLB's placed in x and y co-ordinate system using Genetic algorithm.

The routing of different CLB's is demonstrated in Figure 4.

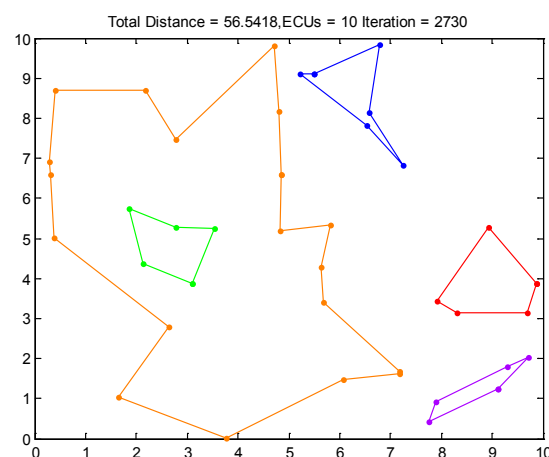


Figure 4. Routing of CLB using GA.

For the above work, coding is written in MATLAB software and then optimization algorithms are simulated using MATLAB software.

4. Conclusion

FPGAs are utilized to implement high performance digital system applications with regard to area, speed and power. FPGA design is reliable only when the placement and routing are effectively implemented. Therefore it is important to use an efficient optimization algorithm. In this brief, GA is proposed for optimizing the tasks of placement and routing the CLBs in FPGAs with optimal wire length.

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6. References

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