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Design of Cascaded Common Source Low Noise Amplifier for S-Band using Transconductance Feedback

Anu Ravindran*, Karthigha Balamurugan and M. Jayakumar

Department of Electronics and Communication Engineering, Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Amrita University, Coimbatore – 641112, Tamil Nadu, India; 007anuravindran@gmail.com, b_karthigha@cb.amrita.edu, m_jayakumar@cb.amrita.edu

Abstract

Background/Objectives: Now-a-days advancements in CMOS technology increase the demand on transceiver design in the aspect of gain, linearity, power, re-configurability and cost-effectiveness[1]. The performance of RF frontend of transceiver system using MOS device are excellent and found to be the par of 3-5 semiconductor technology. **Methods/Statistical Analysis**: The first component present in transceiver design is Low Noise Amplifier (LNA) which requires high gain, low noise, better input-output matching, low power, good linearity and stability. Trade off between these performances is more complex when transistors operate at reduced supply voltage and reduced power consumption. So many researchers focus to modify the existing topology by adding active/passive feedback elements and/or using current re-use inductors[2,3]. But the latter, suffer from large power consumption. Moreover LNA using cascode configuration offers good gain with low power but the circuit has the limitation of output voltage swing[4]. So the proposed work focuses on the design of LNA using transconductance feedback in Common Source (CS) configuration circuits. **Findings:** At RF frequencies, distributed parasitic of the device dominates thus altering the input-output matching characteristics which degrades gain, noise figure and stability of Low Noise Amplifier. So design of multistage LNA with feedback techniques is necessary to increase the gain. The transconductance feedback used in the design of LNA suits well for increase of gain provided if it is properly designed to ensure stability. The proposed work involves the design of MOS based low noise amplifier using single stage and cascaded Common Source (CS) configuration in S-band. By using the transconductance feedback in CS amplifier, the voltage gain is boosted. Using the extracted small signal equivalents, single stage and cascaded CS amplifier with the transconductance feedback are designed and analyzed. Importance of device parasitic like gate to source capacitance, gate to drain capacitance and the output resistance influence the loop gain. This is brought in the design and emphasizes on the proper utilization of these parasitic in LNA design with transconductance feedback. Using a standard 90 nm CMOS process, LNAs have been demonstrated for 2-GHz frequency (S-band) applications. Operated at a supply voltage of 0.6 V, the gain and noise figure of single stage CS LNA with transconductance feedback are observed to be 17.9 dB and 2.1 dB respectively. It is noted that nearly 17% gain improvement has been achieved with excellent input reflection coefficient of -54.8 dB and low power consumption of 2.92 mW. Similarly, for a cascaded CS amplifier when operated at 0.6V, it is observed that the gain and noise figure are found to be 13.6 dB and 2.38 dB respectively. It is noted that nearly 6.25% increase in gain is achieved with appealing reverse gain of -52. 8 dB when compared to cascaded CS circuit without transconductance feedback. Higher reverse gain ensures the stability of the designed amplifier. **Applications:** The proposed work is needed in the design of transceivers working at S-band (2 GHz – 8 GHz). Few noticeable applications are: Communication satellites (NASA), weather radar systems, microwave ovens and optical communication[5] which require low power modules. **Improvements:** This work can be further extended to reconfigure the input matching network so that UWB bandwidth is covered.

Keywords: Cascaded Common Source (CS) Configuration, Low Noise Amplifier (LNA), MOS Parasitic, S-Band, Trasconductance Feedback

**Author for correspondence*

1. Introduction

The design of Low Noise Amplifier is important since its gain should be high so that the noise present in the subsequent blocks is reduced. LNA is a crucial key block in RF receiver ICs which decides the overall system NF (Noise Figure) of the receiver. This paper proposes the design of Low Noise Amplifier at S-band using single stage and cascaded CS amplifier which uses transconductance feedback in the second stage[6]. By considering the propagation characteristics of millimeter-wave band[7], the proposed design focus on the device parasitic and its effect on Low Noise Amplifier at S-band. By properly designing the transconductance feedback using device parasitic, gain can be boosted at the frequency band of interest which is illustrated with relevant analysis. This approach is the novelty of the paper. According to the device parasitic, the gate bias and aspect ratio of transistors are optimized for obtaining high voltage gain, Low Noise Figure, good linearity and high stability in the proposed LNA circuit. Using a standard 90 nm CMOS technology, the proposed single stage and cascaded LNA are designed for the 2-GHz (S-band) band applications.

This paper is ordered as follows. Section 2 in brief illustrates the single stage common source amplifier without and with transconductance feedback. Section 3 describes the cascaded CS amplifier using the transconductance feedback and the influence of device parasitic in the loop gain. Results and discussion of the designed work are presented in Section 4. Finally conclusion is presented in Section 5.

2. Common Source Amplifier

2.1 Single Stage Common Source Amplifier

The most commonly used circuit schematic of a common source amplifier with source degenerative inductance, L_{S1}, is shown in Figure 1(a). The resistive term offered by L_{S1} is used for matching input real part, R_{in}, whereas the reactive part is made to cancel the gate capacitance (C_{gs}) of transistor, M_1. The output impedance matching is achieved using the design of drain inductance, L_{d1} which cancels the output drain capacitance at 2 GHz. Additional resistances, say Rs, is used for compensating internal loss of L_{S1} and R_d is used to match with output terminal resistance.

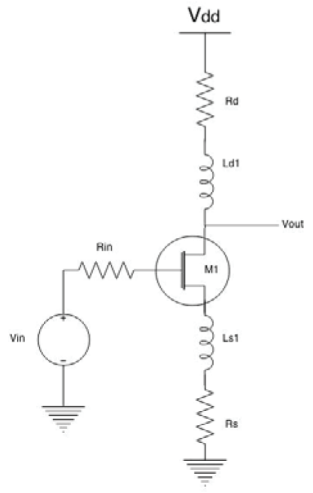

Figure 1 (a). Single stage common source-amplifier.

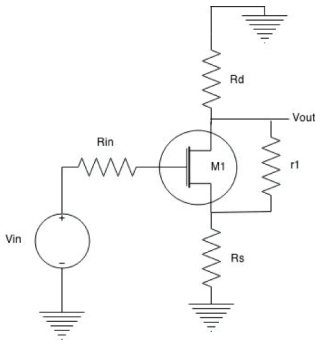

Figure 1 (b). Its equivalent-circuit.

In order to simplify the analysis, the body effect can be ignored. Based on the equivalent circuit shown in Figure 1(b), the overall voltage gain is known to be:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} r_1 R_d}{r_1 + (1 + g_{m1} r_1) R_s + R_d} \approx \frac{g_{m1} R_d}{1 + g_{m1} R_s} \qquad (1)$$

From Equation (1), it is known that the gain depends on the ratio of R_d to R_S, which yields a moderate value.

2.2 Single Stage Common Source Amplifier with Transconductance Feedback

In order to boost the effective voltage gain at low supply voltage, transconductance feedback is included in the common-source amplifier[6]. It can be achieved by properly designing a transconductance stage and the illustrations are shown in Figure 2(a) and Figure 2(b). To inspect the

influence of the feedback stage on the effective voltage gain, an equivalent circuit of the common-source amplifier with transconductance stage is illustrated in Figure 3. Transistor, M_2, forms the feedback element, g_{mf}, as denoted in Figure 2. The small signal equivalent of Figure 1(a) is given in Figure 3. Applying network analysis in the equivalent circuit shown in Figure 3, the overall voltage gain is given by:

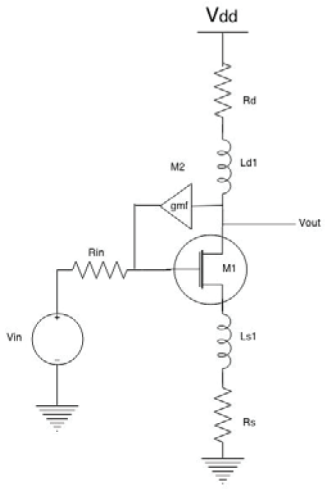

Figure 2 (a). Single stage common source amplifier with transconductance stage.

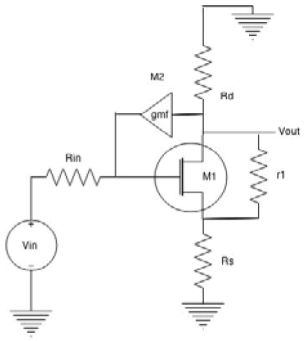

Figure 2 (b). Its equivalent-circuit.

$$Av = \frac{v_0}{v_{in}} = \frac{-g_{m1}Q\left(SC_{gd1} + 1/r_{0f}\right)}{\left(SC_{gd1} + 1/r_{01}\right)\left(SC_{gd1} + 1/r_{0f}\right) - (S^2C_{gd1}) + SC_{gd1}g_{mf}} \quad (2)$$

Where g_{m1}, C_{gd1}, r_{o1} are the transconducatance gain, gate-to-drain capacitance and output resistance of transistor, M_1. Q is the quality factor of input tuning circuit. g_{mf} and r_{of} are the transconducatance gain and the output resistance of feedback transistor.

For maximum gain, make the denominator of Equation (2) equal to zero. And the maximum gain given by:

$$g_{mf} = \frac{-(1 + SC_{gd1}(r_{01} + r_{0f}))}{SC_{gd1}r_{01}r_{0f}} \quad (3)$$

After re-arranging:

$$g_{mf} \approx -\left(\frac{r_{01} + r_{0f}}{r_{01}r_{0f}}\right) \approx -\left(\frac{1}{r_{01} \,||\, r_{0f}}\right) \quad (4)$$

If the parallel combination of r_{01} and r_{0f} is less, then the transconductance gain increases. At least $r_{01} = r_{0f}$ should be maintained, so that higher g_{mf} is achieved.

3. Design and Analysis of Proposed LNA

The proposed circuit topology is basically a two-stage cascaded CS amplifier that includes the input and output

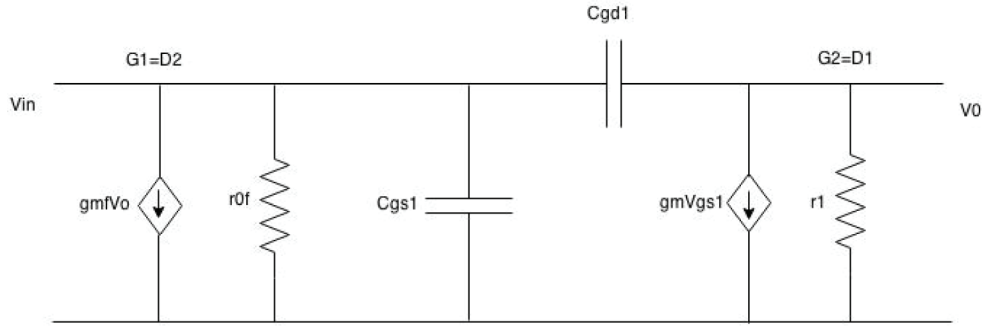

Figure 3. Equivalent-circuit of single stage common source-amplifier with transconductance stage.

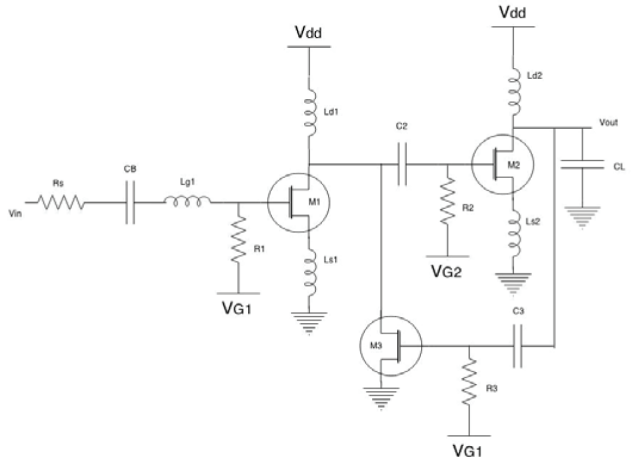

Figure 4. Cascaded CS LNA with transconductance feedback.

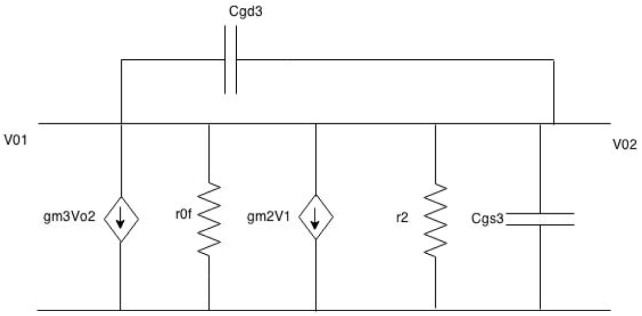

Figure 5. Small-signal equivalent circuit for the analysis of the feedback loop in the second stage of the proposed LNA.

matching network as illustrated in Figure 4 and its equivalent circuit shown in Figure 5.

Assume that the Miller capacitance (C_{gd1}) between the drain and gate nodes of transistor (M_1) is small, so its effect can be removed from the circuit. The input impedance is given by:

$$Z_{in} = s(L_{g1} + L_{s1}) + \frac{1}{sC_{gs1}} + \frac{g_{m1}L_{s1}}{C_{gs1}} \tag{5}$$

The input reflection S_{11} can be written as:

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = \frac{(L_{g1} + L_{s1})C_{gs1}s^2 + (g_{m1}L_{s1} - C_{gs1}Z_0)s + 1}{(L_{g1} + L_{s1})C_{gs1}s^2 + (g_{m1}L_{s1} + C_{gs1}Z_0)s + 1} \tag{5}$$

Where Z_o is the characteristics impedance of transmission line connecting the component and the transistor. The value of Z_o is compensated by the real term offered by the source degenerative inductance, L_{S1}.

$$\frac{g_{m1}L_{s1}}{C_{gs1}} = Z_0 \tag{6}$$

As a result, in circuit implementations, the gm_1 and L_{S1} value should be selected such that $Z_{in} = Z_0 = 50\Omega$ is achieved at the operating frequency of interest,

$$\omega_0 = \frac{1}{\sqrt{(L_{g1} + L_{s1})C_{gs1}}} \tag{7}$$

The small signal equivalent of Figure 4 is given in Figure 5.

Here r_2 represents the parallel combination of output resistance of M_2 transistor and the load resistance. V_{o1} represents the output voltage due to first stage. If proper matching occurs between the output of first stage and input of second stage, then $V_{o1} = V_1$. Appling circuit analysis in the equivalent circuit of Figure 5 gives the expression of loop gain in the feedback path.

$$\frac{V_{02}}{V_{Cgs3}} = \frac{g_{m3}(g_{m2} - s(C_{gd2} + C_{gd3}))}{\left(\frac{1}{r2} + sC_3 + sC_{gd2}\right)\left(\frac{1}{r_{of}} + sC_2 + sC_{gd3}\right) + s(C_{gd2} + C_{gd3})(g_{m2} - s(C_{gd2} + C_{gd3}))} \tag{8}$$

For analysis purpose, assume the transistors M_2 and M_3 are identical. To achieve maximum loop gain, the following constraint on feedback transconductance, g_{m2} of M_2 is ensured to make Equation (8) infinity.

$$g_{m2} = \frac{4(sC_{gd})^2 - \left(\frac{1}{r} - sC_x\right)^2}{2sC_{gd}} \tag{9}$$

Where:

$$C_x = C_3 + C_{gd2}$$

$$r = r_{02} = r_{03} = r_{0f}$$

$$C_3 = C_{gs3} + C_{gd3}$$

Thus depending on parasitic of M_2 and M_3 transistors, the value of feedback transconductance, g_{m2} is adjusted. If this constraint is satisfied then the loop gain increases to larger value. From circuit shown in Figure 4, the effective voltage gain of the two stages LNA can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{I_{d1}}{V_{in}} \cdot \frac{V_{out}}{I_{d1}} = A_{v1}.A_{v2} \quad (10)$$

Where Av_1 and Av_2 are the voltage gains of the first stage and second stage of the two stages cascaded LNA. From the above analysis, it is observed that the overall voltage gain is mainly determined by the effective transconductance of transistors (M_1, M_2 and M_3) and their output resistances. Hence, the bias current and the aspect ratio of the common-source MOS transistors must be chosen accordingly to increase the gain.

As indicated in[8], the total noise factor of the LNA can be written as:

$$NF_{cas} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \ldots\ldots\ldots \quad (11)$$

By using the transconductance feedback, the gain can be boosted in the second stage and hence the denominator product term, $A_{v1}A_{v2}$ increases. This reduces the noise figure considerably, which is the desired performance. The stability of the circuit is determined by the design of input-output matching circuit. In this work, values of R_{S1} and R_d are adjusted according to the source and load impedance connected to the circuit. Thus, absorption of resistance at input-output ports does not happen and hence negative resistance at each port is avoided. This ensures the stability of the designed circuit.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \geq 1$$
$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (12)$$

Based on the observed S-parameters, Equation (12) is used[9] for testing the stability of the circuit.

4. Results and Discussion

Based on 90 nm CMOS technology, cascaded CS LNA using transconductance feedback is designed. Performance metrics like S-parameters, stability and noise figure of designed cascaded CS LNA are compared with circuit having no feedback. Figure 6 and Figure 7 shows the output S-parameter curves corresponding to transconductance feedback and without using feedback for comparison. All S-parameters occur at 2 GHz except S_{11}, input reflection co-efficient. This might be due to slight mismatch of impedance that has occurred due to L_{S1} and R_S. Respective numerical values are tabulated in Table 1.

Figure 8 and Figure 9 shows the result of the stability factor and the noise figure of cascaded CS amplifier using transconductance feedback and without using feedback

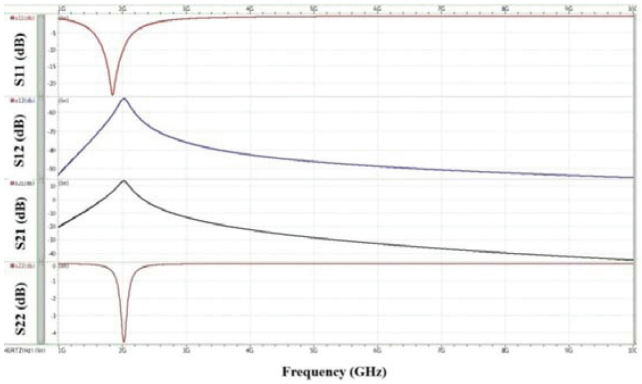

Figure 6. S-parameters of cascaded CS LNA using transconductance feedback.

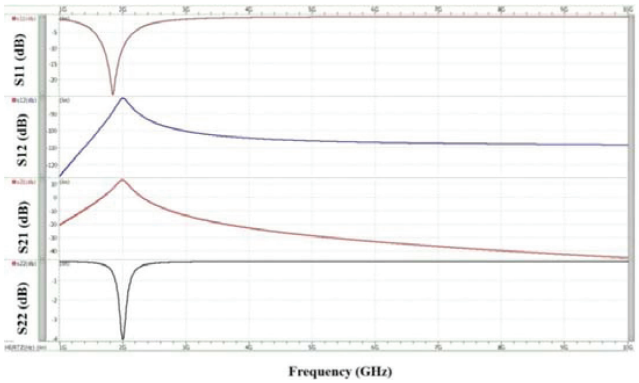

Figure 7. S-parameters of cascaded CS LNA without feedback.

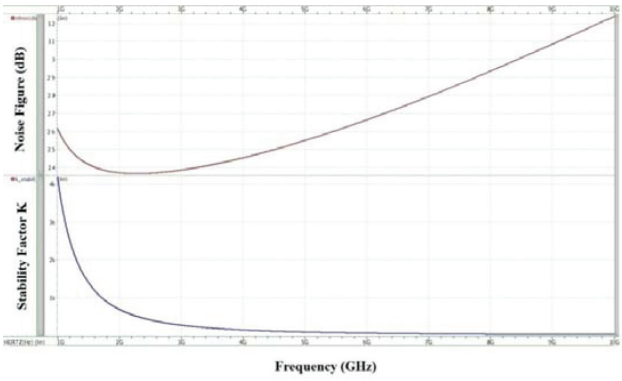

Figure 8. Stability and noise figure of cascaded CS LNA using transconductance feedback.

Table 1. Performance summary of the low-voltage LNA

	CMOS Tech.	Freq.	Supply Voltage	DC Power	|S21|	NF	|S11|	|S12|	|S22|	K
Unit	**nm**	**GHz**	**V**	**mW**	**dB**	**dB**	**dB**	**dB**	**dB**	-
Two stage with transconductance feedback	90	2	0.6	50.5	13.6	2.38	-10.3	-52.8	-4.4	2.62
Two stage without transconductance feedback	90	2	0.6	48.2	12.8	2.37	-9.6	-81	-3.94	6.85
Single Stage with transconductance feedback	90	2	0.6	2.92	17.9	2.1	-54.8	-15.1	-13.3	1.2
Single stage without transconductance feedback	90	2	1	23.6	15.3	1.4	-7.53	-32.3	-2.74	1.4

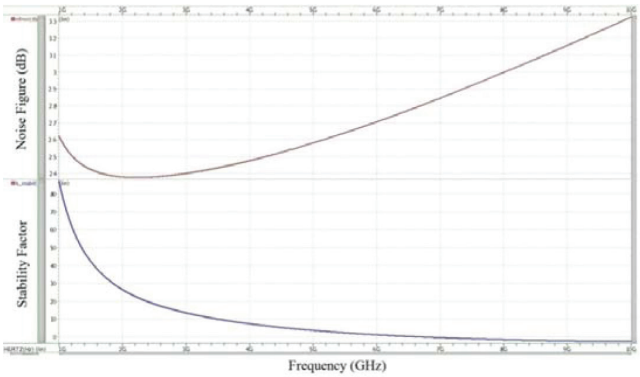

Figure 9. Stability and noise figure of cascaded CS LNA without feedback.

respectively. Stability of cascaded CS LNA using transconductance feedback comes down to 2.62 from 6.85, but still the value is >1, which ensures stability. Whereas the noise figure for both the circuits are observed to be same value, since the transconductance feedback CS LNA does not contribute the resistive component in the design. Hence additional thermal noise is not included and the noise figure is constant value even after adding transconductance feedback.

The power dissipation of the cascaded CS LNA with feedback is observed to be 50.5 mW whereas for without feedback is 48.2mW. Adding transconductance feedback the power dissipation increases by 4.77 % only.

5. Conclusion

By using a standard 90 nm CMOS technology, a 2 GHz (S-band) single stage and two stage CS LNA using transconductance feedback have been designed. Gain boosting is achieved by adding transconductance feedback in the circuit topology. About 17% increase in gain is achieved for a single stage CS amplifier by adding transconductance feedback. The power dissipation in this case reduces to 2.92 mW from 23.6 mW with excellent input reflection co-efficient. Similarly when compared to two stage CS amplifier without feedback, gain increases by 6.25% for a two stage CS amplifier using transconductance feedback with excellent reverse isolation. Thus the stability of the proposed designed circuits is guaranteed. Performance of cascaded CS amplifier with transcondcutance feedback is achieved at the cost of additional 2.3 mW power. Noise figure is almost constant value after adding transconductance feedback. For each design, small signal equivalent is obtained and presented. Respective voltage gain and loop gain of transconductance feedback are derived. Based on device parasitic, the constraints on designing transconductance of feedback transistor and amplifying transistors are presented. This clearly gives a picture that how the device parasitic influence the transconductance, g_m, voltage gain and the loop gain of the circuit. This work can be extended by designing an input reconfigurable circuit to provide a constant gain in the entire UWB band.

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