Indian Journal of Science and Technology, Vol 9(22), DOI: 10.17485/ijst/2016/v9i22/90152, June 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Various Techniques to Overcome Noise in Dynamic CMOS Logic

Misbah Manzoor[1], ShekharVerma[2]*, Tapsi Singh[2] and Mahwash Manzoor[2]

[1]Department of Electronics and Communication Engineering, SSM College of Engineering, Srinagar - 191111, Jammu and Kashmir, India; Misbah1002@gmail.com
[2]Department of Electronics and Communication Engineering, Lovely Professional University, Phagwara - 144411, Punjab, India; Shekharverma05@gmail.com, Er.tapsi14@gmail.com, Mahwash25@yahoo.com

Abstract

The advent of dynamic logic especially domino logic has made the use of dynamic circuits very wide for the implementation of low power VLSI circuits. Dynamic logic style is becoming the designers' choice these days because it has very fast speed and occupies very small area. In this paper we have used various techniques based on domino logic to overcome noise. Each technique has its merits and demerits. Out of these techniques mentioned below we have taken two widely used techniques in domino logic, conditional keeper technique and diode footed domino. We calculated their noise margins at different values of supply voltage. We have done simulations in 90 nm technology. After calculations we found both techniques show fairly good noise immunity but diode footed domino gave better results.

Keywords: Delay, Diode Footed Domino, Immunity, Leakage Tolerance, Noise, Power Consumption, Subthreshold Voltage, Technology Scaling

1. Introduction

Very Large Scaling of integration made it possible to incorporate many transistors on a small circuit and has thus increased the circuit performance. But this scaling of technology poses problems in the design of deep submicron. Noise immunity needs to be paid attention in DSM. The increase in various leakage currents, rapidly changing clock frequencies, large amount of crosstalk and various other noise sources reduce the noise immunity of different circuits. Since we know technology scaling takes place day by day supply voltage needs to be reduced to keep up the device reliability,and thus it demands reduction in threshold voltage. A noise immunity of a circuit can be reduce by decreasing the threshold voltage of a circuit reduce the noise immunity but it increase the exponential in subthreshold leakage currents that in turns increase the leakage power of subthreshold region. As frequencies of processors increases day by day, domino logic has become the choice of circuits as it accomplishescritical paths so as to offer significant faster switching speed than other circuit styles. Since domino logic circuits tend to occupy smaller areas which makes them attractive for use, but these advantages have some drawbacks also. Domino logic is susceptible to noise. Hence its usage includes many design risks and there is a need to verify its functionality and performances.

Figure 1, shows a general form of aCMOS dynamic logic circuit. General functioning of dynamic gates basically takes place because of charge storage for a small amount of time in the dynamic node. For this there is a need of continuous up gradation and refreshingof various internal nodes. Now this brings into account that refreshing of charges can be performed by regular application of clock signal. A dynamic logic circuit as shown in Figure 1 reduces the number of transistors used. All the dynamic circuits follow the same basic principle which is initially precharge the output node then after that evaluates the output in accordance with applied inputs. The precharge phase has a function to keep the circuit on adefined initial state andevaluation phase shown the basic response of the circuit. Although low switching threshold voltages can be

*Author for correspondence

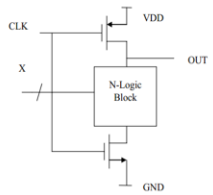


Figure 1. Generalized dynamic logic circuit.

achieved by dynamic logic but it may suffer from different process variations and design.

Noise in CMOS circuits can be seen as a change whichtakes the dynamic node voltage response away from its actual response. Noise affects different circuit parameters thatmay include leakage, crosstalk, supply variations etc. Due to low switching threshold voltage V_{th} Domino circuits more susceptible to noise. Threshold voltage is defined as the input voltage at which the output state changes. There are many methods to reduce the effects of noise; one of them is raising the switching threshold voltage. It will automatically sacrifice the circuit performance in terms of parameters like power consumption, delay, speed that makes dynamic circuits popular and feasible. Hence a noise tolerant method should provide improvement against noise without compromising other attributes like speed, power and delay. Noise in digital circuits occurs due to charge sharing and charge leakage. Charge leakage is further of two types that is Subthreshold Leakage and Reverse Bias P-N Junction Leakage. Subthreshold Leakage is commonly assumed that when the transistor is off there is no current flowing through it, but actually what happens is there exists a non-zero leakage current that flows in the channel at the microscopic level even if the transistor off. This current is called as subthreshold leakage current as it flows at a region below threshold voltage. Subthreshold leakage depends on various parameters such as device dimensions, temperature, drain to source voltage, fabrication process etc. Impact of drain to source voltage is almost negligible when it is much larger than thermal voltage. When the V_{th} threshold voltage is lowered or scaled down the various variations do not scale down in accordance. As a result of this subthreshold leakage current increases with lowering of threshold voltage. It is very small and is measured in pico amperes. It is usually independent of the operating voltage of a device and is very hard to ignore. It often becomes very difficult to predict and measure leakage current. It also poses power problems at times and hence needs to be looked after.

The second type of leakage which is Reverse Bias P-N Junction Leakage which occurswhen either when the source of an N transistor is at Vdd or the drain of a P transistor is at Gnd. It has been observed that because of the parasitic effect of bulk CMOS devices, and p-n junctions are formed at the drain or source of transistors. The small current that flows as a result of this reversed biased p-n junctions is called as p-n junction reverse bias leakage current. The amount of current that flows depends on various parameters like temperature, area of p-n junction, applied voltage.

2. Noise Tolerant Dynamic Techniques

Noise is a phenomenon which causes our output to change from normal value to an abnormal value. Noise can be measured in terms of noise margin. Noise margin may be defined as the ability of a circuit to withstand noise. Gate internal and external noise are some classification of noise in dynamic logic circuit[1]. For improvement of noise immunity in dynamic CMOS logic gates a large number of techniques have been developed. These are listed as under 1. Dynamic feed through logic; 2. Diode footed domino; 3. Precharging internal nodes; 4. Raising source voltage; 5. Using keeper.

2.1 Employing Keeper

It is the most simple and old technique used to increase noise immunity. Different kinds of keepers are employed for these purposes are mentioned below. The main aim ofkeeper is to take a very small amount of current from the supply voltage to replenish the charges which are stored in node known as dynamic node as shown in Figure 2(a). In some keepers the gate is connected to ground for some time and this structure known as an always on keeper, it increase the dc power consumption. This is because the keeper remains on supplying the charge continuously even if the charge replenishment is not required. As such a large amount of charge is wasted unwantedly and power consumption gets increased. A feedback keepers technique were used in which the output is given to the keeper as a feedback as shown in Figure 2(b) to overcome this problem. This technique decreased the problem of dc power consumption. In this technique the charge is supplied to the dynamic node only when it is required hence saving power dissipation unlike always on keeper. Further it was seen that using a keeper causes a serious problem which

was contention, hence it put stress on sizing of keepers[2]. If the keeper transistor size is kept smaller from those of transistors in a pull down network it reduces delay and power consumption but if we want better noise immunity its size is kept large. Hence keeper size puts forward a tradeoff between noise immunity and other parameters. Now in order to overcome this problem a new keeper technique called as conditional keeper was employed as given in Figure 2(c) it makes use of two keepers. It came up with the result of less leakage and faster evaluation. In this technique first keeper pk1 is larger in size and is turned off after some time delay so as to stop the wrong discharge of dynamic node when input combination is all low. The second smaller keeper pk2 is kept on to makeup for leakage of charges till pk1 is turned on[2]. One more important keeper technique called as saturated keeper was introduced which is shown in Figure 2(d). Here when the evaluation phase starts the keeper is biased in saturation region so that it reduces delay and power and provides the required amount of noise margin. To achieve the required level the gate voltage of keeper is kept at V_{DD}-V_T level. The voltage of the gate of keeper, is connected to the output of a Not gate with input sensing the dynamic node voltage. At the beginning of evaluation phase clk and are high, if the inputs available do not call for discharging the dynamic node, the gate voltage of keeper will be maintained at V_{DD}-V_{Tn2} and will provide desired noise immunity[3].

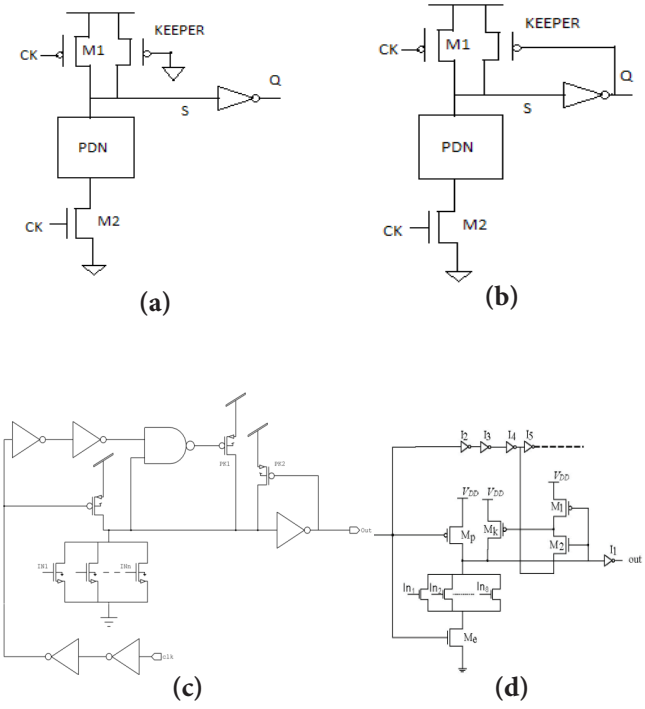


Figure 2. Noise immunity improvements techniques. **(a)** Saturated keeper. **(b)** Conditional keeper. **(c)** Feedback keeper. **(d)** Always-on keeper.

2.2 Raising Source Voltage methods

2.2.1 NAND Gate by D'Souza's Method

A 2 input NAND gate as shown in Figure 3(a) called as a D'Souza's method. In figure given below transistor Mn turns on during evaluation and node N_1 is brought down which further turns on Mp and that leads to a voltage divider circuit. The voltage at node N_1depends on feature of transistors Mn and Mp. It also depends on many technological parameters. Source node of transistor Mb is node N_1; increase in the voltage at N_1 inturn increases threshold voltage of Mb because of body effect. The difference between input voltage at B and the N_1 surpasses the increased threshold voltage of the transistor when Mb is turned on. Due to this noise immunity of the circuit improve although it comes with a problem of dc power consumption. It does not result in rail to rail voltage swing. To avoid this problem the feature size of transistor may be increased but this can decrease the noise immunity provided by this technique[4].

2.2.2 NAND Gate by using Mirror Technique

The two input NAND gate as shown in Figure 3(b) designed by using mirror technique. The basic working principle of this technique is same as of the technique mentioned above. Here an external feedback is used to avoid the problem of power dissipation. It does so by showing the working of Schmitt trigger circuit. Pull down nmos network is duplicated and the node N_1 is precharged by transistor Mn. During the evaluation phase transistor Mn is on, in the meantime N_1 is precharged to V_{dd}-$V_{t,Mn.}$ For some kind of input combinations a path is formed in the pull down network which brings down node N1. Meanwhile transistor Mn is still on, a voltage divider gets formed and voltage at node N_1 is brought down. It short this technique replicates the pull down network and also makes use of a feedback control nmos transistor whose function is to decreases dc power consumption and enhances the noise immunity. As the transistors in the pull-down network are off, the mirror network of transistor is also turned off. As such it cuts off dc conducting path. Thus it solves dc power consumption problem[5]. Besides this, the mentioned technique results in increased area and speed[5].

2.2.3 NAND Gate by Twin Transistors Technique

The 2 input NAND gate as shown in figure 3(c) designed by using twin transistor technique. The additional transistors used here called as twin transistors increase the turn on voltage as it pulls up the voltage of the common source nodes. The technique given above provides good noise immunity but it consumes more energy. The twin transistors used in the circuit increase the node capacitance and circuit delay. Moreover by increasing the size of the transistors used in the pull down network, delay can be improved. The additional twin transistors remove the charge sharing problem. To precharge the internal node an extra transistor at each node is used only when the input combination is such that charge sharing may take place[6].

2.3 Internal Node Precharging

2.3.1 Precharge of all Internal Nodes

Mostly charge sharing takes place in dynamic circuit among various internal nodes and the dynamic nodes

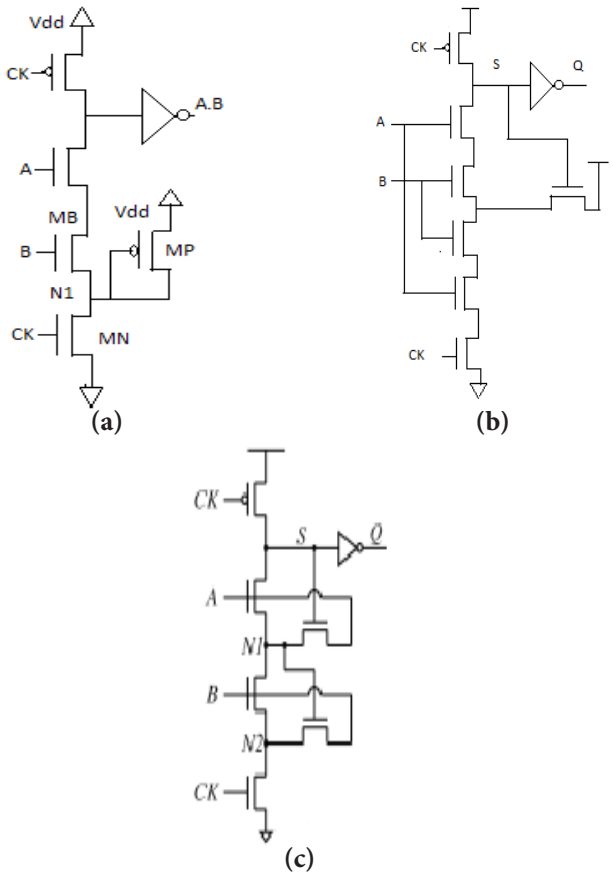


Figure 3. **(a)** D'Souza's method. **(b)** Mirror technique. **(c)** Twin transistor technique.

and it often causes wrong output. Charging the internal nodes firstly present in the pull down network can overcome this problem. As the internal nodes have been precharged this charge sharing is removed but it comes with greater area. Also this effect on the load capacitance by increasing it on clock net[7]. Here the internal nodes are precharged by pmos transistors. They act more like keepers which supply the charges to the respective nodes when charge leakage and charge sharing occurs. This is shown in Figure 4(a). It most likely eliminates charge sharing problems in dynamic circuits.

2.3.2 Precharging by Convino's Methods

As shown in Figure 4(b), is a modification of internal node precharging technique. In this method the input data given actually precharges the internal node. It gives better noise immunity as it precharges pmos. The switching threshold voltage in the dynamic logic gate depends on sizing of pmos transistors. The disadvantage this technique has is that it is not helpful to wide fan in or gates firstly because there are multiple paths for charge leakge and secondly it causes static power dissipation[9].

2.4 Diode Footed Domino Technique

It gives a better noise immunity in a standard domino circuit. The NMOS transistor used here is in diode configuration. The main thing that helps here is stacking effect which has great impact on noise and reduces it by decreasing the leakage current in the evaluation path. There is a leakage current caused by evaluation transistors which result in some voltage drop along the diode footer transistor used (M_1). This drop in the voltage causes gate to source voltage of the off evaluation transistors negative. This results in reduction in subthreshold leakage current. Also the diode increases the body effect which also reduces the subthreshold leakage. Furthermore the diode footer switching threshold voltage of the gate of the nmos devices which in turn leads to better noise immunity. But all this is done at the expense of degradation in performance. To enhance the performance a mirror transistor is used which mirrors the evaluation current. Transistor M_4 is used in the feedback configuration. This prevents the short circuit power dissipation. Mostly circuits like comparators, multiplexers are employing this technique. Here mirror ratio also puts forward a way to trade off two parameters like performance and robustness. As shown in Figure 5(a) used this network in evaluation phase in order to enhance the speed a current mirror.

2.5 Logic Design Technique by Dynamic Feed

In this method of noise immunity is applicable as it gives more noise immunity in addition to low power. It is shown in Figure 5(b). As the clk is kept higher thess transistor Mr is turned ons, discharged the output node. This phase known as reset phase. Evaluation phase comes into play when the clock goes low. Initially there is false logic evaluation occurs and there is no path between transistor Mq and pull down network as all inputs to NMOS are reset to low in this period. After finishing that the inputs obtain their correct logic value and hence S evaluates to correct logic level. If the input combination applied is such that the pull down network is ON then contention takes place between PMOS and pull down network. In the evaluation period although it has performance advantage FTL results in lesser noise margins and direct and non-zero nominal low output voltage. Thus to remove this problem modified feed through logic technique was introduced. Here an additional PMOS transistor is used to decrease charge sharing between internal node and dynamic node. This in turn results in an increase in Vt in the pull down transistor and thus gives better noise immunity. Charge sharing between capacitance C1 and C2 in the evaluation phase may lead to wrong output, therefore transistor M3 avoids this problem as it precharges the internal node T. What happens here is that node S and T are precharged to the same potential and no charge sharing occurs between C1 and C2. Since only extra transistor is used to improve noise immunity of the circuit unlike other techniques. Also as numbers of transistors are less the overall power dissipation is also less[8]. As shown in Figure 5(c).

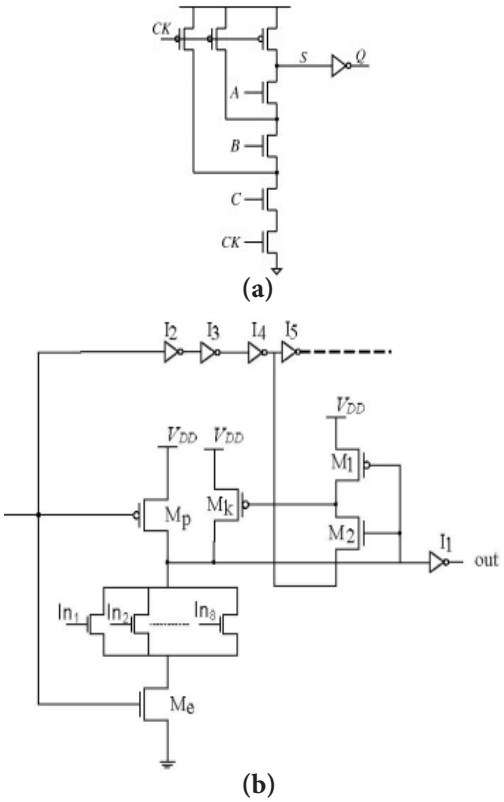
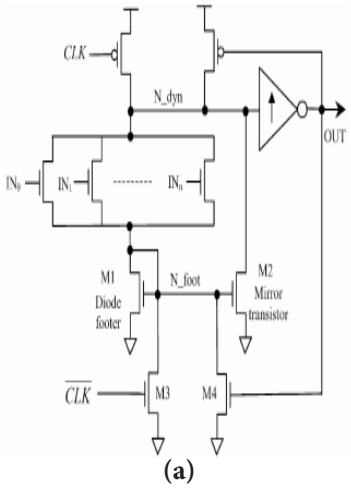
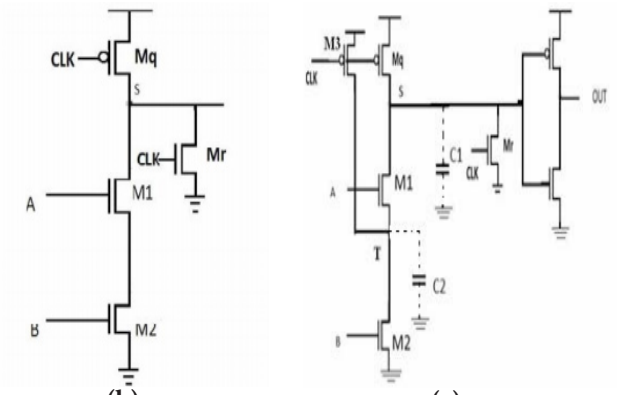


Figure 4. Precharging of internal nodes by. **(a)** Precharging of all internal nodes. **(b)** Precharging by Convino's method.

3. Conclusion

Different noise tolerant techniques have been discussed in Table 1 and Table 2. Keeper technique used is very helpful in providing good noise immunity and gives lesser power consumption in addition to lesser area as shown in Figure 6. It is most widely used technique and can be used in different forms like feedback keeper, conditional keepers etc. Raising the source voltage techniques which include mirror and twin transistor technique result in more silicon area of the circuit, low speed of circuit and increased power dissipation. Techniques like internal node precharging puts forward the problem of dc power consumption. It is effectively used for only specific types of logics. Diode Footed Domino is mostly used for high fan-in circuits and is a leakage tolerant and high performance technique. It gave better results than conditional keeper technique which can seen in the table and graph given below. Diode footed domino also consumes less power. Conventional FTL is not that much helpful in reducing noise as modified FTL is, so an advanced new version of FTL is used for increasing noise immunity. It





(b) (c)

Figure 5. **(a)** Domino logic by diode footed. **(b)** Conventional Feed through Logic (FTL). **(c)** Modified FTL.

Table 1. Comparison of noise tolerance techniques of dynamic circuits

Category	Methods or Techniques	Consumption of DC Power	Noises of all types
I	Always on keeper	Higher	Effective
	Feedback keeper	Lesser	Effective
	Conditional keeper	Higher	Not Effective
	Saturated keeper	Lesser	Not Effective
II	D'Souza	Higher	Effective
	Mirror technique	Lesser	Effective
	Twin transistor	Lesser	Not Effective
III	Precharging of all internal nodes	Lesser	Not Effective
	Precharging by Convino's method	Higher	Not Effective
IV	Diode footed domino	Lesser	Effective
V	Modified Feed Through Logic	Lesser	Not Effective

Table 2. Comparison of noise tolerance techniques of dynamic circuits.

VIL (mV)		
Supply (v)	Conditional Keeper	Diode footed Domino
0.8	380.0061	396.5633
0.9	412.8481	444.1028
1	449.9281	492.9904
1.1	504.5413	542.7832
1.2	543.7096	593.7402

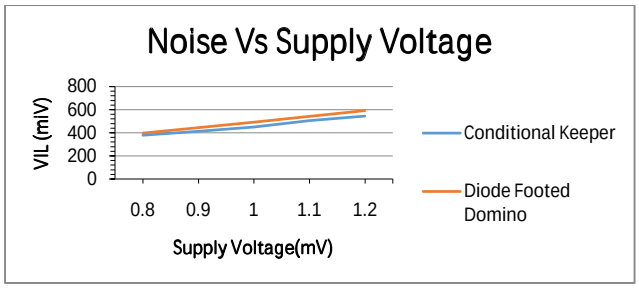


Figure 6. Noise vs supply voltage.

eliminates the charge sharing problem and also results in less power dissipation

4. References

1. Ding, Mazumder P. On circuit techniques to improve noise immunity of CMOS dynamic logic. IEEE TransactionsonVery Large Scale Integration VLSI Systems. 2004 Sep; 12(9).
2. Govindarajulu S, Prasad TJ, Sreelakshmi C, Chandrakala, Thirumalesh U. Energy efficient, noise tolerant CMOS domino VLSI circuits in VDSM technology. IJACSA. 2011; 2(4).
3. Mahmoodi H, Roy K. Diode footed domino: A leakage tolerant high fan in dynamic circuit design style. IEEE Transactions Circuits and Systems. 2004 Mar; 51(3)495–503.
4. Booba S, Hajj IN. Design of dynamic circuits with enhanced noise tolerance. Proceedings of 12th Annual IEEE International ASIC/SOC Conference; Washington, DC. 1999 Feb. p. 54–8.
5. Wang L, Krishnamoorthy R, Soumyanath K, Shanbhag N. An energy efficient leakage tolerant dynamic circuit technique. Proceedings of International ASIC/SOC conference; 2000 Apr. p. 221–5.
6. Kursun V. Domino logic with variable threshold voltage keeper. IEEE Transactions. 2003 Dec; 11(6).
7. Assaderaghi F, et al. Dynamic threshold voltage MOSFET for ultra low voltage VLSI. IEEE Trans Electron Devices. 1997 Mar; 44:414–22.
8. Pattanaik M, Parashar S, et al. A novel low noise tolerant high performance dynamic feed through logic design technique. International Symposium on Electronics System Design; 2011 Oct.
9. Anis MH, Allam MW, Elmarsy MI. Energy-efficient noise tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies. IEEE Trans Very Large Scale Integr Syst. 2002 Sep; 10(2):71–8.
10. Wang L, Shanbhag NR. An energy efficient noise tolerant dynamic circuit technique. IEEE Transactions Circuits and

Systems-II: Analog and Digital Signal Processing. 2000 Nov; 47(11).
11. Govindarajulu S, Jayachandra T, et al. Energy efficient, noise-tolerant CMOS domino VLSI circuits in VDSM Technology. International Journal of Advanced Computer Science and Applications. 2011; 2(4).
12. Alvandpour A, Krishnamurthy R, Sourrty K, Borkar SY. A sub-130-nm conditional-keeper technique. IEEE J Solid-State Circuits. 2002 May; 37(5):633–8.
13. Jung S-O, Kim KW. Noise constraint transistor sizing and power optimization for dual V T domino logic. IEEE Transactions on VLSI Systems. 2002 Oct; 10(5).
14. Peiri A, Asyaei M. Current-comparison-based domino: New low-leakage high-speed domino circuit for wide fan-in gates. IEEE Trans Very Large Scale Integration (VLSI) Systems. 2013 May; 21(5).
15. De V, Borkar S. Technology and design challenges for low power and high performance. Proc Int Symp Low Power Electronics and Design, ISLPED 99; San Diego, CA, USA. 1999 Aug. p. 163–38.
16. Kim J, Roy K. A leakage tolerant high fan-in dynamic circuit design technique. Proc 27th European Solid-State Circ Conf, ESSCIRC; Villach, Austria. 2001 Sep. p. 309–12.
17. Ye Y, Borkar S, De V. A new technique for standby leakage reduction in high-performance circuits. Proc IEEE Symp on VLSI Circuits. 1998. p. 40–1.
18. Choi SH, Somasekhar D, Roy K. Dynamic noise model and its application to high-speed circuit design. Microelectron J. 2002; 33:835–46.
19. Stan MR, Panigrahi A. The Selective Pull-up (SP) noise immunity scheme for dynamic circuits. Proc Design, Automation and Test in Europe 2002; Paris, France. 2002 Mar. p. 1106.
20. Sinthuja S, Kumar JH, Manoharan N. Energy efficient voltage conversion range of multiple level shifter design in multi voltage domain. Indian Journal of Science and Technology. 2014; 7(6):82–6.
21. Sanapala K, Sakthivel R. Low power realization of subthreshold digital logic circuits using body bias technique. Indian Journal of Science and Technology. 2016; 9(5):1–5.
22. Karthikeyan A, Arunarasi J, Arul Mary A. a neoteric fpga architecture with memristor based interconnects for efficient power consumption. Indian Journal of Science and Technology. 2016; 9(5):1–9.
23. Hemalatha SB, Vigneshwaran T, Jasmin M. survey on energy-efficient methodologies and architectures of network-on-chip. Indian Journal of Science and Technology. 2016; 9(2):1–8.