ISSN (Print) : 0974-6846
Indian Journal of Science and Technology, Vol 8(31), DOI: 10.17485/ijst/2015/v8i31/70388, November 2015 ISSN (Online) : 0974-5645

A Novel Concept of Nine Level Active Neutral Point Converter

R. Hari Nandeeswara Rao* and K. Narasimha Raju

Department of EEE, KL University, Vaddeswaram, Guntur - 522502, Andhra Pradesh, India;
harinandeeswar@gmail.com, nraju@kluniversity.in

Abstract

This paper presents a new single-phase nine-level active neutral-point clamped converter topology. The main aim of this topology is to achieve optimal total harmonic distortion and helps to obtain voltage balancing among the capacitors. An analysis of the switching state and commutation of the converter are also presented here in order to balance the power losses among the semiconductor devices. This paper also analyzes the Space Vector Pulse Width Modulation (SVPWM) strategy for 9L-ANPC converter in the virtual coordinate, and presents an optimized control strategy which can balance the Neutral Point (NP) voltage and avoid the dead-time effects for the first time. The nine-level active neutral-point-clamped (9LANPC) converter has been widely studied for its excellent performance in high-power medium-voltage applications. The simulation has been carried out in MATLAB SIMULINK to investigate the effectiveness of the proposed topology.

Keywords: Active Neutral Point Clamping, Multi-Level Inverter, SVPWM Technique

1. Introduction

In many studies the balancing problem of multilevel three phases diode-clamped was the main focus. However until now the only solution that has been implemented is for high modulation indices. Balancing is not possible unless additional hardware is used for balancing the voltage as the number of levels increases in the converter[1]. Another drawback is unequal distribution of losses among semiconductor devices. This characteristic reduces the maximum output power and reduces the converter efficiency. To maintain equal distribution of losses among switches devices the three-level active neutral-point clamped (3L-ANPC) converter is considered the best choice[2]. Since the introduction of the 3L-ANPC great deal of attention has been given to multilevel converters topologies. To achieve optimal THD active neutral-point clamped five-level (ANPC-5 L) has been proposed. However, the capacitors voltage balancing is a crucial task in ANPC and the control is also more complex. To maintain the voltage of the capacitors in the dc link, numerous redundancies are used in[3] to control the capacitors voltage. Such topology contributes to increasing the inverter output voltage levels and enhances the power.

This paper presents a novel single-phase 9L-ANPC for low-voltage applications. The waveform profile of the inverter output is close to a pure sine wave. A technique to make the voltage in dc-link capacitors balanced has been proposed.

To ensure the equal distribution of switching losses two Pulse-Width Modulation (PWM) strategies are used and compared with each other. A brief comparison between the proposed inverter and other counterparts is carried out. Finally, simulation and experimentation results are provided to ensure the feasibility of the proposed inverter and the employed modulation techniques[4].

2. Proposed Converter

The new 9L-ANPC converter is presented in Figure 1. It combines features from the NPC and the FC topologies resulting in two main advantages:

- It only uses one Neutral Point (NP) like the 3L-NPC, which makes it capable of operating in the four quadrants. A neutral point voltage balance study for the

* Author for correspondence

new 9L-ANPC converter has been carried out as it is done in [5] for the 3L-NPC. At any point below the curve the neutral point can be controlled each switching period and above the curve a voltage ripple at three times the fundamental frequency appears. In any case, the voltage ripple is controllable at any point using a Nearest Three Vectors (NTV) modulation. This characteristic is independent of the topology and common to multilevel topologies with one neutral point, that is, it can be observed in the 3L-NPC, in the previously employed 5L-ANPC and in the proposed 9L-ANPC converter.

- The volume required by the flying capacitors is reduced in comparison to the FC topology, making the construction of the converter feasible. Furthermore, the C1 flying capacitor of the new topology is dimensioned like the C1 capacitor of the previously employed 9L-ANPC. C2, C3, C4 and C5 capacitors are much smaller comparing to C1, their size is similar to the size of a decoupling capacitor and no control is required to maintain their voltages at their rated values[6]. Thus, the new 9L-ANPC requires the same number of voltage sensors to control the topology as the previously employed 9L-ANPC (VC1, VDC and NP voltage).

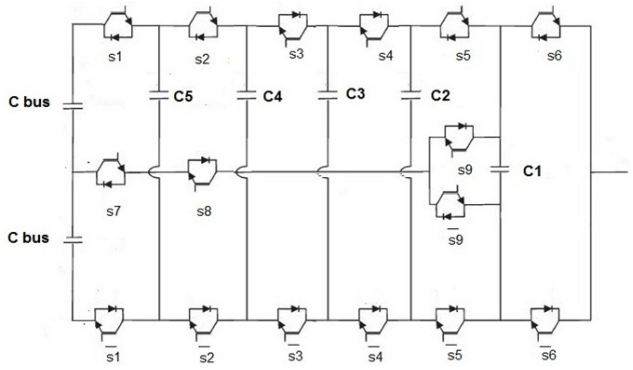

Figure 1. Proposed Nine-Level ANPC configuration.

The previously employed 9L-ANPC also features these advantages. However, the new 9L-ANPC has two main advantages over the previous 9L-ANPC.

It does not require any series connection of semiconductors, whereas the previous topology connects semiconductors in series and requires additional hardware[7] to hold their blocking voltage at their rated value. C1, C2, C3, C4, and C5 assure the desired blocking voltage value of all semiconductors in the new topology.

2.1 Operating Principle

The new converter has 5 voltage levels (+VDC/2, +VDC/4, +VDC/6, +VDC/8, 0, -VDC/8, -VDC/6, -VDC/4 and -VDC/2). The operation of the new converter can be divided in two distinct half-periods: the positive and negative half-period of the output voltage. During the positive output voltage half-period, CBUS1 and C1 are used to obtain +VDC/2, +VDC/4, +VDC/6, +VDC/8, 0 voltages and during the negative output voltage half-period[1], CBUS2 and C1 are used to obtain 0, -VDC/8, -VDC/6, -VDC/4 and -VDC/2 voltages[8]. Each half period can be identified with an inner 3L-FC, as shown in Figure 2. Dotted polygon delimiters the inner 3L-FC for the positive half-period and the dashed polygon delimiters the inner 3L-FC for the negative half-period. S7 switches at fundamental frequency similarly to S1 in the previously employed 5L-ANPC.

During the positive output voltage half-period +VDC/8 can be obtained adding the C1 voltage (VC1) to the NP or subtracting VC1 to +VDC/2. These two different switching states have opposite effects on VC1. In the same way, during the negative output voltage half-period -VDC/8 can be obtained adding VC1 to -VDC/2 or subtracting VC1 to the NP. These two different switching states have also opposite effects on VC1. Therefore, VC1 can be kept under control by choosing the appropriate switching states[9].

3. Modulation Technique for 5L-ANPC System

In this section a simple modulation technique is described to control the new 9L-ANPC converter for a three phase system. The modulation is based on that described in [10], but in our case, the Space Vector Modulation (SVM) technique is used instead of the carrier-based PWM. A sixth part of the vector diagram for a five-level converter is shown in Figure 2, where +VDC/2, +VDC/4, +VDC/6, +VDC/8, 0, -VDC/8, -VDC/6, -VDC/4 and -VDC/2 voltage levels are denoted as 8, 7, 6, 5, 4, 3, 2, 1 and 0 respectively.

The modulation and the control technique comprises in different stages such as:

- Depends on the reference value of phase angle and modulation index consider the nearest three possible vector components.

- Choose a sequence consists of four vectors as {x1, x2, x3, and x4} in this the first and last vectors are similar. From the Figure 2 consider the sequence of four vectors as {(841), (840), (740), (730)}. And from this the duty cycles are obtained as {d1, d2 and d3}[11].

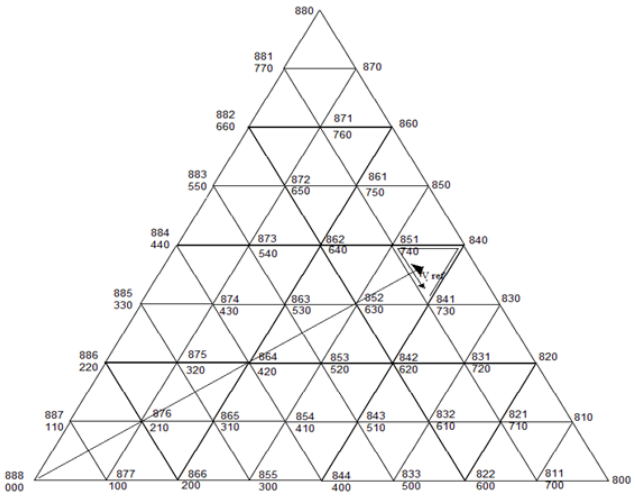

Figure 2. Vector diagram for 9Level converter.

4. Simulation Diagram and Explanations

In this paper the Figure 3 shows the simulation experimental diagram for the nine level Active Neutral Point Clamped technique based on the Figure 1. The gate signals for this converter is obtained by the space vector method.

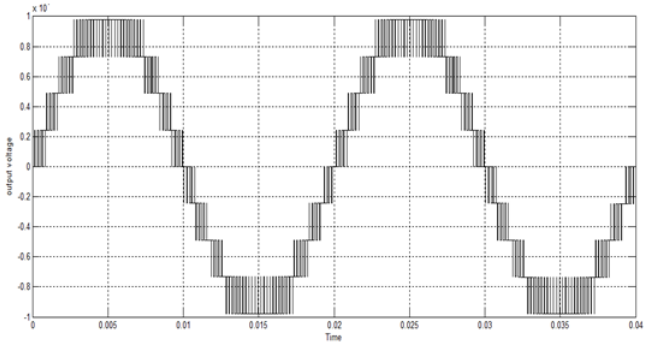

Figure 4. Nine Level Output Voltage.

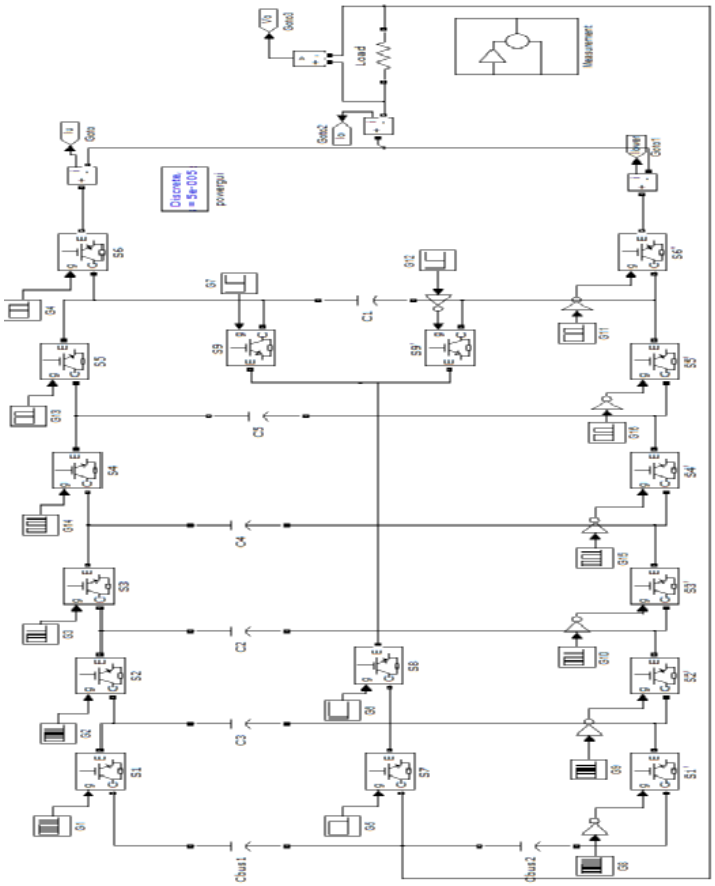

Figure 3. Simulation Diagram for the ANPC system.

Figure 4 shows the simulation results of nine level output voltage of the proposed ANPC converter under unity power factor load.

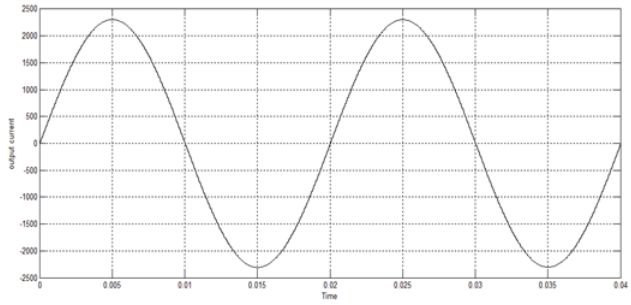

Figure 5. Output Current.

The simulation results for the output current of ANPC converter under unity power factor load is as shown in Figure 5.

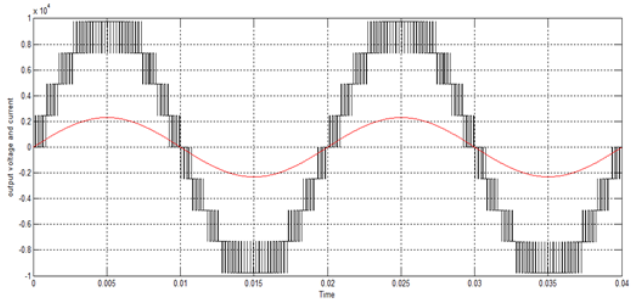

Figure 6. Output Current and voltage.

Figure 6 shows the simulation result of power factor observation in terms phase difference of voltage and current in ANPC converter under unity power factor.

CASE 2: At lagging power factor

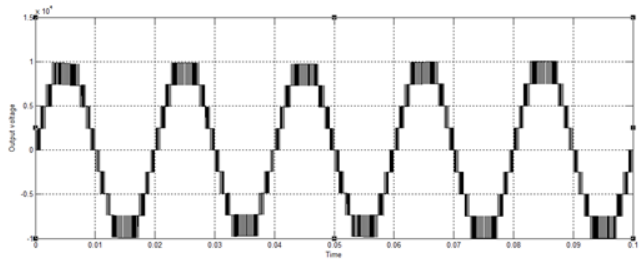

Figure 7. Nine Level Output Voltage.

Figure 7 shows the simulation results of nine level output voltage of the proposed ANPC converter under lagging power factor load.

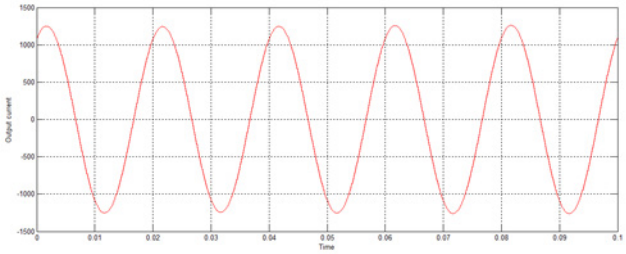

Figure 8. Output Current.

The simulation results for the output current of ANPC converter under lagging power factor load is as shown in Figure 8.

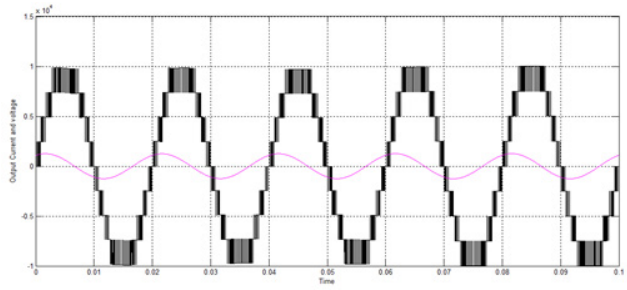

Figure 9. Output Current and voltage.

Figure 9 shows the simulation result of power factor observation in terms phase difference of voltage and current in ANPC converter under lagging power factor.

5. Conclusion

This paper presents an optimized control strategy based on the well-known SVPWM for 9L-ANPC converters. The proposed strategy analyzes all the space vectors' characteristics of balancing the NP voltage, and divides them into seven categories of triangles. Every category has its own principles to choose the vector sequence and compute the vector durations based on the NP voltage difference, which can balance the NP voltage flexibly. This optimized control strategy also provides principles to choose appropriate switching states for voltage levels to make sure that the No-Offset-Glitches of phase voltages can be avoided successfully. A low power three-phase 9L-ANPC converter prototype is built to verify the performance of the optimized control strategy.

6. References

1. Burguete E, López J, Zabaleta M. New five-level active neutral point clamped converter IEEE. IEEE Transactions on Industry Applications. 2014; 51(1):440–7.
2. Rodriguez J, Franquelo LG, Kouro S, Leon JI, Portillo R, Prats M, Perez M. Multilevel converters: An enabling technology for high power applications. Proc IEEE. 2009 Nov; 97(11):1786–817.
3. Wang K, Li Y, Zheng Z. A neutral-point potential balancing algorithm for five-level ANPC converters. International Conference Electrical Machines and System (ICEMS); Beijing. 2011. p. 1–5.
4. Guedouani R, Fiala B, Berkouk EM, Boucherit MS. Modelling and control of three-phase PWM voltage source rectifiers- five-level NPC voltage source inverter-induction machine system. 2010 18th Mediterranean Conference on Control Automation (MED); Marrakech, Morocco. 2010 Jun. p. 533–8.
5. Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: A survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics 2002. 2002 Aug; 49(4):724–38.
6. Osman RH. Medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality. 34th IAS Annual Conference on IEEE Industry Applications. 1999 Oct; 4. p. 2662–9.
7. Barbosa P, Steimer P, Steinke J, Meysenc L, Winkelnkemper M, Celanovic N. Active Neutral-Point-Clamped Multilevel Converters. 36th Power Electronics Specialists Conference; 2005 Jun. p. 2296–301.
8. Subhashini M, Latha P, Bhagyaveni MA. Comparative Analysis of Harmonic Distortion of a Solar PV Fed Cascaded H-bridge Multilevel Inverter Controlled by FPGA and Diode Clamped Inverter. 2015 Jul; 8(16).
9. Zhang Y, Sun L. An efficient control strategy for a five-level inverter comprising flying-capacitor asymmetric H-Bridge. IEEE Transactions on Indus trial Electron, ICS. 2011; 58(9):4000–9.
10. Thielemans S, Ruderman A, Reznikov B, Melkebeek J. Improved natural balancing with modified phase-shifted PWM for single-leg five level flying-capacitor converters. IEEE Trans Ind Electron. 2012 Apr; 27(4):1658–67.
11. Bharathi Sankar A, Seyezhai R. Development of Active Neutral Point Clamped Multilevel Inverter Fed BLDC Drive Employing FPGA. 2015 Feb; 8(4).