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Modified Architecture for Binary Array Multiplier with Reduced Delay using Tristate Buffers

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Abstract

In VLSI design of system configuration, among the three important parameters of speed, area and power, the speed is purely determined by the delay of the design. In the delay of the design the design delay is contributed by gate delay and routing i.e. path delay. Nowadays in the design, the path or routing delay dominates more towards the design delay compare to the earlier days where gate delay dominates more towards the design delay. Because of scaling in the design, it is essential to concentrate more towards routing delay of the design to get the optimized delay or desired speed of the design with the reduced area. In this work, by studying different architectures constructed with different basic module for binary array multiplier contributes towards the routing delay which can be realized to result in reduced delay.

Keywords: Architecture, Binary Array Multiplier, Path Delay, Routing Delay, VLSI

1. Introduction

For any system design, the arithmetic units are much important to make it as a successful design. Arithmetic units like adders took much important part to play a role since subtraction and multiplication are all computed by computation of addition only. For any design there is a need to use arithmetic circuits. Without those circuits none other designs can be made. By concentrating delay minimization in arithmetic circuits surely that leads to make impact in minimizing the delay in all the design. So, if the speed is achieved by minimizing the delay in the architecture of the adder and multiplier surely it leads to better performance in the speed of the design in the system. So, various multiplier architectures were surveyed, realized and their delay was compared in various literature.

This paper is organized as follows. Section - 1 says about the introduction. Section - 2 deals about Binary Array Multiplier. Section - 3 deals with Literature Survey with Existing Architecture. Section - 4 says about the proposed Architecture. Section - 5 deals with experimental results with conclusion of the work completed Section - 6 brief about the future work.

2. Binary Array Multiplier Architecture

A combinational multiplier was a good example of how simple logic functions (gates, half adders and full adders) can be combined to construct a much more complex function. In particular, it is possible to construct a 4x4 combinational multiplier from an array of AND gates, half-adders and full-adders, as a hierarchical design it has got extended to a more complex circuit. The purpose of this work was to introduce how relatively a complex arithmetic functions like binary array multiplication can

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be implemented using simple logic building blocks i.e. using sub-block. It was very useful and interesting while considering how a binary array multiplication can be performed. Figure 1 describes the structure of binary multiplication of two four bit integer values[24].

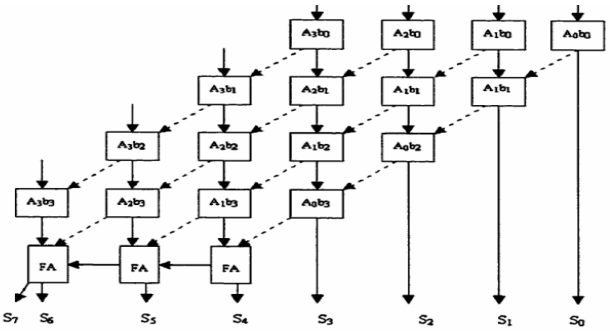

Figure 1. Four bit binary array multiplier architecture.

In this work the following sub modules are used to realize binary array multiplier. The multiplier architecture with different sub modules is constructed and comparison was done with implemented architecture.

- Multiplier Architecture with basic gates.
- Multiplier Architecture with NAND only gates.
- Multiplier Architecture with Half and Full Adders.
- Multiplier Architecture with multiplexers.
- Multiplier Architecture with tri-state buffers.

In order to achieve the high speed and low power demand in the design of ICs for DSP applications, parallel array multipliers are widely used. For these applications, most of the power is consumed by the multipliers only. Hence low power multipliers must be designed in order to reduce the power dissipation in DSP applications. IO path delay specifies the cell delay. Interconnect delay specifies the point to point delay. The two basic functions of array multiplier, partial product generation and summation are combined. For unsigned NXN multiplication, N^2+N-1 cells are connected to produce a multiplier, where N^2 AND gate for partial product generation, a full adder for summing and N-1 cells containing a full adder[25].

For unsigned 4X4 multiplication, 19 cells are connected to produce a multiplier, where 16 AND gate for partial product generation is shown in Figure 2.

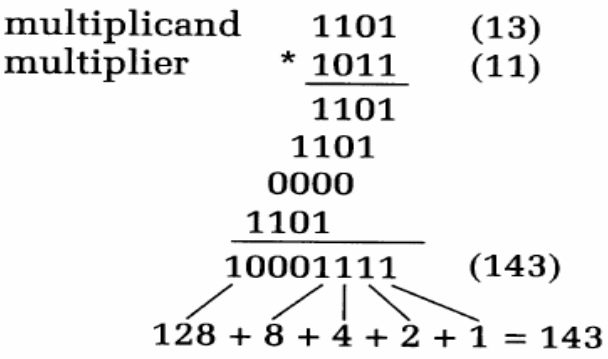

Figure 2. Partial products and interconnect path length.

3. Literature Survey

The architecture of the multiplier plays a vital role in the design of any digital system. Novelty in its architecture towards the delay minimization is much important. In the paper[1], the critical path delay between input and output was minimized by properly doing the vertical and horizontal slicing between the input nodes and output nodes. In the paper[2], the node to node (every input node to every output node) delay was examined and it was reduced by proper interconnection between the array elements with the neighborhood row in the four bit systolic array multiplier architecture. In the paper[3] the array generates N lower product bits directly and uses a carry-propagate adder, in this case a ripple carry adder, to form the upper N bits of the product. Replacing full adder with half adders, possibly reduces the complexity to N^2 AND gates, N half adders and N (N-2) full adders. The worst case delay is (2N-2) $X\Delta_c$ where Δ_c is the adder delay.

4. Proposed Architecture

The work proposes architecture for binary array multiplier using tri-state buffers. This architecture results in following advantages such as reduced interconnect delay, reduced size, reduced development time and quick prototyping, flexibility, also it can quickly adapt to different architecture.

Figure 3 and Figure 4 illustrate the sub modules used in the proposed architecture. As the outcome from the

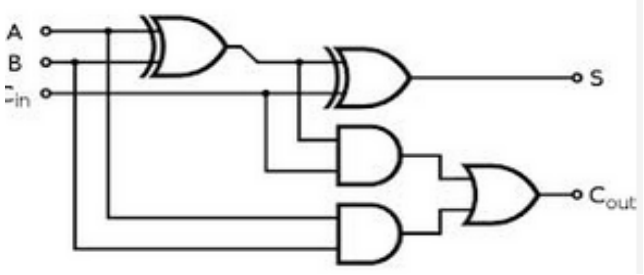

Figure 3. Full adder as sub module in the architecture.

carried out modified architecture by reviewing various existing high speed multipliers, the improved speed (lesser delay) was achieved.

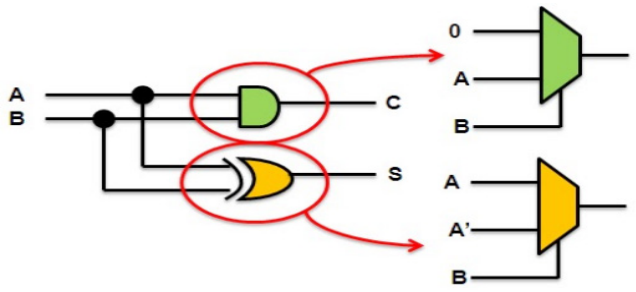

Figure 4. Half adder implementation using MUX.

Shannon's decomposition theorem is used to implement all the gates by using multiplexers[23].

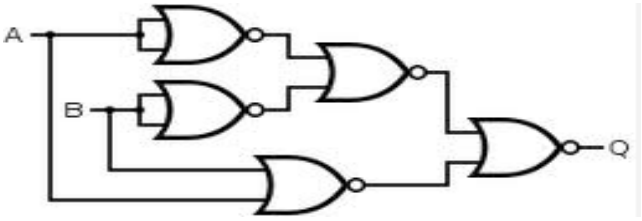

Figure 5. NOR only circuit for XOR implementation.

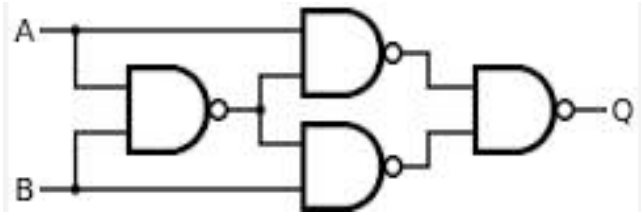

Figure 6. NAND only circuit for XOR implementation.

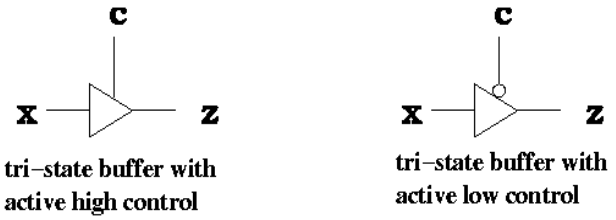

Figure 7. Tri-state buffer with active high and low control.

Tri-state buffer/inverter is such a good device for many devices to communicate with one another is on bus interconnected architecture. And that a bus should only have one device writing to it, although it can have many devices reading from it. Since many devices always produce output (such as registers) and these devices are hooked to a bus, we need a way to control what gets on to the bus and doesn't.

5. Results and Conclusion

In the proposed work an improved architecture for the design of binary array multiplier with tristate buffers was arrived and implemented on VLSI by using the target device as Spartan-3E which provided an optimized combinational path delay for the design of architecture.

Table describes the results for multiplication architecture with various sub modules. Even though various sub-modules are used in the construction of architecture of binary array multiplier using tri-state inverter provides

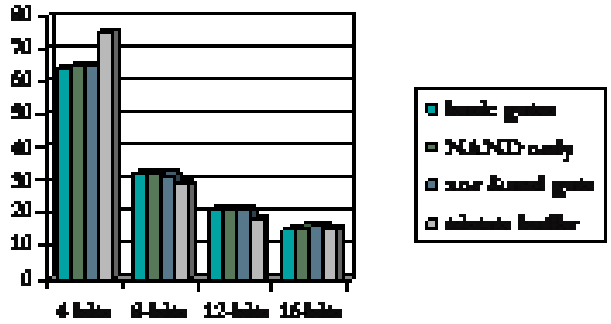

Figure 8. Results comparison.

Result Table **(for 16 bits)**

Schemes	No. of LEs	Freq. X10 $^{-6}$	Power(Watts)
Multiplier architecture with basic gates	292 slices 508 LUT	15.588	0.081
Multiplier architecture with NAND only gates	293 slices 510 LUT	15.653	0.081
Multiplier architecture with Half adder & full adder gates	293 slices 510 LUT	15.635	0.081
Multiplier architecture with decoder	290 slices 504 LUT	15.963	0.081
Multiplier architecture with multiplexers	293 slices 510 LUT	15.635	0.081
Multiplier architecture with tristate inverters	381 slices 714 LUT	14.891	0.081

Figure 9. Result table (for 16 bits).

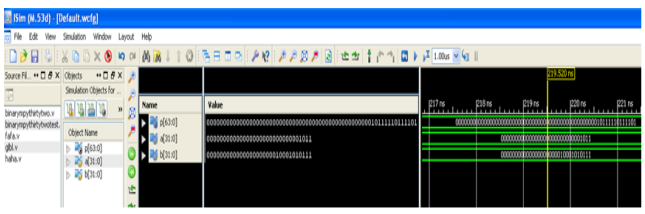

Figure 10. Simulation Result (for 16 bits).

a 5% less delay compared to other sub-module architecture. Binary array Multiplier Architecture with 8, 12, 16, 32 and 64 bits are taken and realized.

By analysis, it was concluded that the reduced path delay was obtained for architecture with tri-state buffers. Due to reduced delay this architecture will find applications in high speed system design like system on-chip and Network on chip.

6. Future Work

Although this work is focused towards the minimization path delay in the architecture, the same can be achieved by implementing the design using some other sub module like mirror adder which may also be controlled by routing algorithm.

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