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Design and Implementation of FPGA based 64-bit MAC Unit using VEDIC Multiplier and Reversible Logic Gates

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Abstract

Now a days in VLSI technology size, power, and speed are the main constraints to design any circuits. In normal multipliers delay will be more and the number of computations also will be more. Because of that speed of the circuits designed with the normal multipliers will be low and it will consume more power. This paper describes Multiply and Accumulate Unit using Vedic Multiplier and DKG reversible logic gates. The Vedic multiplier is designed by using UrdhavaTriyagbhayam sutra and the adder design is done by using reversible logic to perform high speed operations. Reversible logic gates are also the essentialconstraint for the promising field of Quantum computing. The UrdhavaTriyagbhayam multiplier is used for the multiplication function to reduce partial products in the multiplication process and to get high concert and less area.The reversible logic is used to get less power. The MAC is designed using Verilog code, simulation, synthesis is done in both RTL compiler using Xilinx and implemented on Spartan 3e FPGA Board.

Keywords: MAC, Reversible Gates, Vedic Multiplier

1. Introduction

Multiplication Multiplier design is the most important factor in the design of Multiply accumulate unit. In digital signal processing applications multipliers plays major role in many applications ling FFT, DFT and convolution applications. In such cases the number of computations performed also very important. Why because If the number of computations increases the delay also increases. So that the speed of processor reduced. In VLSI multipliers can be designed in many ways. By using logic gates or by using transmission gates or by using multiplexers we can design multipliers. We have booth's Multipliers, Array multipliers, Baugh Wooley Multipliers and Vedic Multipliers[1].

One the most important factor in the MAC design is Adder. Adders are key elements in the design of multipliers. Such that high speed adders requires to perform high speed operations. The design of adder elements determines performance of the system. We have Serial adders. Parallel adders, Carry Select Adders, Carry Save Adders, Ripple carry adders and Reversible adders.

In many Digital Signal Applications Multiplier block consumes more power and occupies large area. Area and power consumptions also depends on the number of computations of the design of multiplier block and adder block[13].

2. Literature Review

Nareshnaik, SivaNagendra Reddy proposed "Design of Vedic Multiplier for Digital Signal Processing Applications"[1]. In this method design of adders is difficult and design may be complex and also its require more power.

Anitha, Kumar proposed "A 32 BIT MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate" design.

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In this paper they designed for 32-bit Multiplier. But most of the multipliers used in Digital signal processing applications 64-bit multipliers.

So many researchers proposed many methods to design multipliers and adders. Among all the methods multiplier design with reversible logic gate design is the efficient method. In reversible gates also different reversible gate are available[4].Some researchers used Kogge stone Adders, some researchers used Toffiligates[5].DKG is the one of the gate used in the MAC design. This proposed method represents 64-bit MAC design using reversible logic gates.

3. Proposed Method

MAC (Multiply Accumulate) uses both Adders and multipliers and from both the result is accumulated .MAC is used in so many applications like DSP advanced microprocessors and so many logic functional units. this particular block in processors is one of the major important factor to determine the speed which uses efficient FFT/IFFT algorithms. in general, these two techniques use most of the time addition and multiplication which are building blocks in operating faster. Delay in processors is due to irregular structure of the adders. this is one factor we need to consider for improving the speed.

A multiplication operation in processors is done generally in three different factors.1.Addition 2.Intermediate product addition.3.Final result generation. Our proposed design uses of one of the most efficient multiplier i.e. vedic multiplier and reversible logic gate and it can be done in two stages. in the initial stage we will replace the normal multiplier with vedic multiplier using one of the old multiplication technique which is known as urdhava tiryakabhyamsutra. speed is primarily determined by the multiplication block which later will effect on area, power consumption and dissipation to avoid these we will go for one of the efficient multiplication operation in DSP Processors. The later part is reversible logicgate system in which the information lost was determined by the kT*log2where k is the Boltzmann's constant and T is the absolute temperature at which computation operation is done.

4. Design of MAC Architecture

The design of MAC architecture consists Design of Accumulator which integrates both multiplier and adder stages, Design of 64 X 64-bit Vedic Multiplier and Design of 128 bit DKG adder of three sub designs is shown in figure 1.

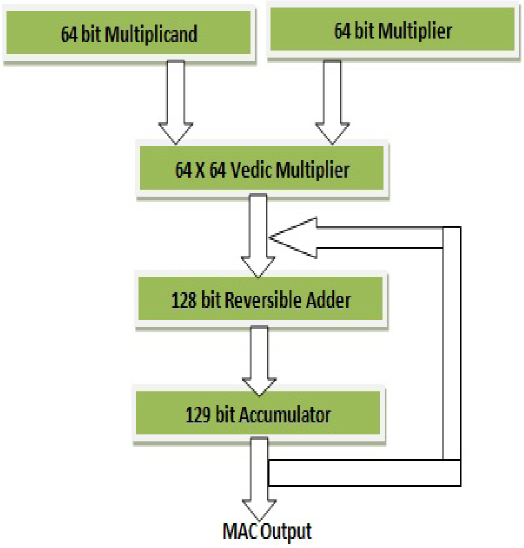


Figure 1. 64 bit multiply accumulator architecture.

In most cases the delay in the architecture is due to the addition in parallel stages which we have to concentrate more to improve the speed. Finally, we are going to compare our Vedic MAC unit with the Conventional MAC unit based on the parameters like Speed, area and power consumption[2].

A multiplying block function can be conceded in three different ways: conventional addition, Partial Product Addition (PPA) and finally Partial Product Generation (PPG). The two bud vase materials that must be considered are raising the speed of MAC which is accumulator block partial and product reduction[7, 8]

4.1 Vedic Multiplier

Vedic Mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. Vedic Mathematics existed in ancient India and was revived by a popular mathematician, Sri Bharati Krishna Tirthaji. He divided Vedic mathematics into sixteen formulae (sutras). Those are Chalana Kalanabyham,Gunakasamuchyah,NikhilamNavatashcaramam Dashatah,ParaavartyaYojayet,(Anurupye)Shunyamanyat, Shunyam Saamyasamuccaye, Ekanyunena Purvena, Vyashtisamanstih, Puranapuranabyham, Shesanyankena Charamena, EkadhikinaPurvena, Yaavadunam, Sopaantyadvayamantyam, Sankalanavyavakalanabhyam, Gunitasamuchyah and Urdhva-tiryakbhyam.

These formulae deal with Algebra, Analytical Geometry, Algebra, Trigonometry, Geometry etc.

The ease in the Vedic mathematics sutras covers way for its application in several prominent domains of engineering like Signal Processing, VLSI andControl Engineering.

4.2 UrdhwaTiryakbhyam Algorithm

Let us consider two eight bit numbers X(7:0) and Y(7:0) , where 7 signify Most Significant Bit and 0 represent Least Significant Bit. P0 to P15 signify each bit of the final computed product. It can be seen from equation (1) to (15), that P0 to P15 are calculated by adding partial products, which are calculated previously using the AND operation.

The individual bits attained from equation (1) to equation (15), in turn when concatenated produce the final product of multiplication which is represented in equation (16).The carry bits produced during the computation of the individual bits of the final product are corresponded from C(1) to C(30). The carry bits produced in equation (14) and equation (15) are ignored while they are redundant[13-15].

$$\mathbf{P0} = A0 * B0 \tag{1}$$

$$\mathbf{C1P1} = (A1 * B0) + (A0 * B1) \tag{2}$$

$$\mathbf{C3C2P2} = (A2 * B0) + (A0 * B2) + (A1 * B1) + C1 \tag{3}$$

$$\mathbf{C5C4P3} = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) + C2 \tag{4}$$

$$\begin{aligned}\mathbf{C7C6P4} = {} & (A4 * B0) + (A3 * B1) + (A2 * B2) + (A1 * B3) \\ & + (A0 * B4) + C3 + C4\end{aligned} \tag{5}$$

$$\begin{aligned}\mathbf{C10C9C8P5} = {} & (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) \\ & + (A1 * B4) + (A0 * B5) + C5 + C6\end{aligned} \tag{6}$$

$$\begin{aligned}\mathbf{C13C12C11P6} = {} & (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) \\ & + (A2 * B4) + (A1 * B5) + (A0 * B6) + C7 + C8\end{aligned} \tag{7}$$

$$\begin{aligned}\mathbf{C16C15C14P7} = {} & (A7 * B0) + (A6 * B1) + (A5 * B2) + (A4 * B3) \\ & + (A2 * B5) + (A1 * B6) + (A0 * B7) + C9 + C11\end{aligned} \tag{8}$$

$$\begin{aligned}\mathbf{C19C18C17P8} = {} & (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + \\ & (A3 * B5) + (A2 * B6) + (A1 * B7) + C10 + C12 + C14\end{aligned} \tag{9}$$

$$\begin{aligned}\mathbf{C22C21C20P9} = {} & (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) \\ & + (A3 * B6) + (A2 * B7) + C13 + C15 + C17\end{aligned} \tag{10}$$

$$\begin{aligned}\mathbf{C25C24C23P10} = {} & (A7 * B3) + (A6 * B4) + (A5 * B5) + (A4 * B6) \\ & + (A3 * B7) + C16 + C18 + C20\end{aligned} \tag{11}$$

$$\begin{aligned}\mathbf{C27C26P11} = {} & (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + \\ & C19 + C21 + C23\end{aligned} \tag{12}$$

$$\mathbf{C29C28P12} = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 + C26 \tag{13}$$

$$\mathbf{C30P13} = (A7 * B6) + (A6 * B7) + C25 + C27 + C28 \tag{14}$$

$$\mathbf{P14} = (A7 * B7) + C29 + C30 \tag{15}$$

$$P15 = (A7 * B7) \tag{16}$$

Graphically exemplifies the step by step procedure of multiplying two eight bit signals using the Urdhwa Tiryakbyam Vedic Multiplication Sutra[20]. The black encircles state the bits of the multiplier and multiplicand, and the two-way arrows specify the bits to be multiplied in order to arrive at the individual bits of the final product. The architecture of the 8x8 Urdhwa Tiryakbyam vedic-multiplier is shown in Figure 2. Design of 32 X 32 and 64 X 64-bit Vedic Multiplier and Design of 128 bit DKG adder designs is shown in figure 3 and 4.

5. Design of Adder using Reversible Logic DKG Gate

Reversible logic is a distinct method diverse from other logic. Loss of information is not probable here. In this

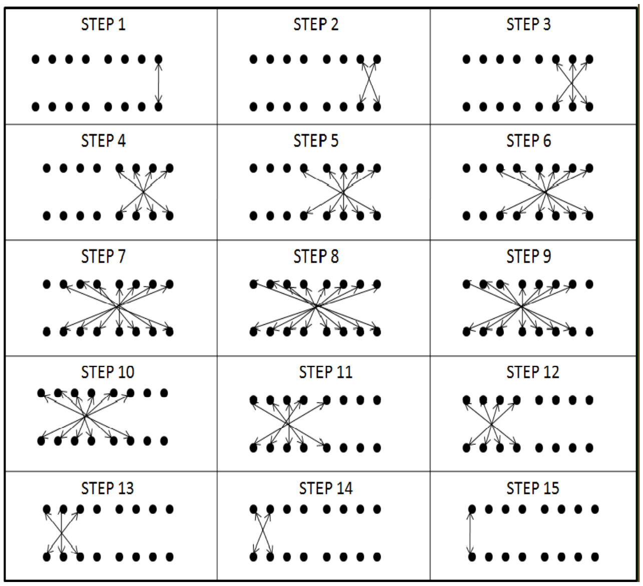


Figure 2. Pictorial illustration of UrdhwaTiryakbhyam Sutra

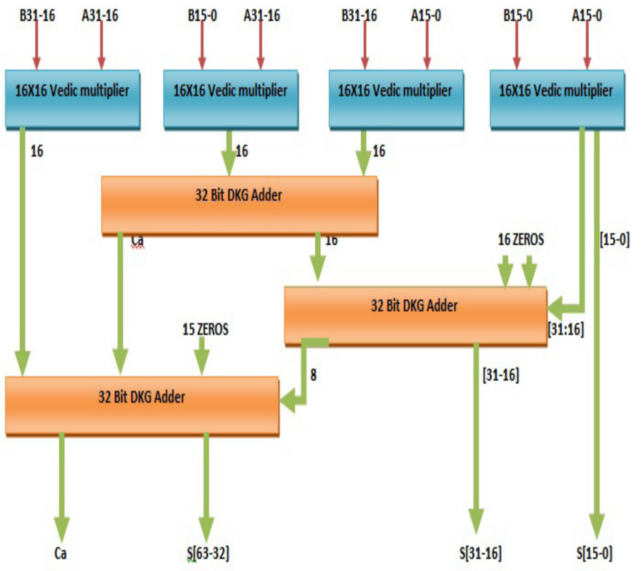


Figure 3. 32 ×32 vedic multiplier using 16 × 16 vedic multiplier.

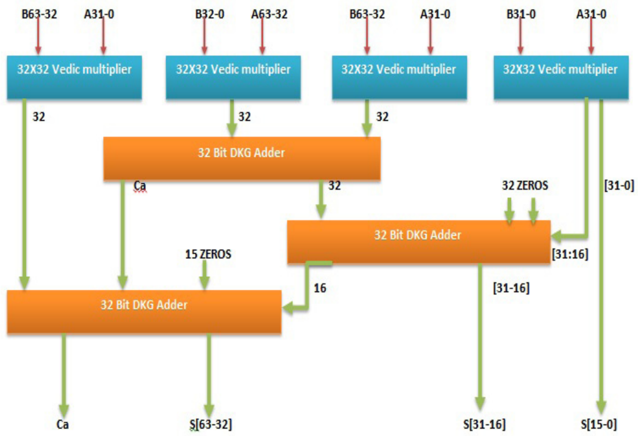


Figure 4. 64× 64 vedic multiplier using 32x32vedic multiplier.

logic, the numbers of output signals are identical to the number of input signals.

A Boolean function is reversible if and only if all the values in the input signal set can be mapped with a single value in the output position. Landauer and Bennet both demonstrated that the usage of conventional irreversible circuits will construct us to power dissipation a circuit consisting of only reversible gates does not dissipate power. The following points necessity be reserved in mind to realize an optimized circuit:

- Loops are not authorized
- Minimum delay

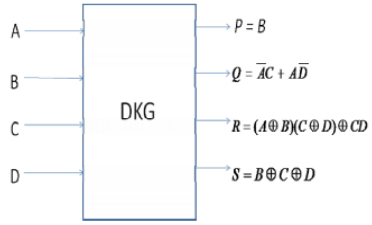


Figure 5a. DKG gate.

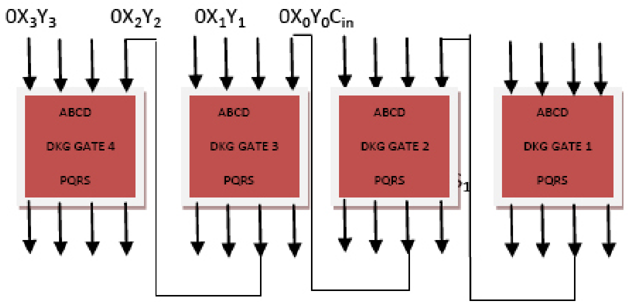


Figure 5b. Parallel adder using DKG gate.

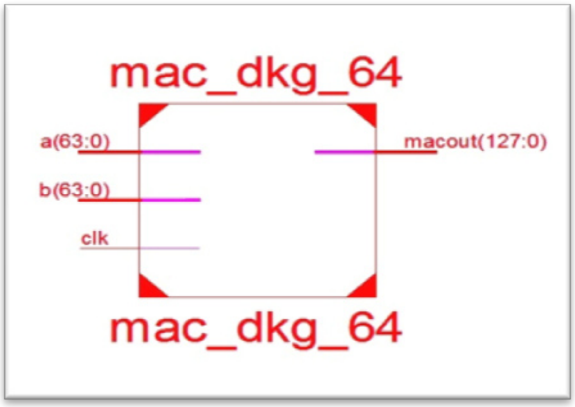


Figure 6a. RTL schematic of MAC unit.

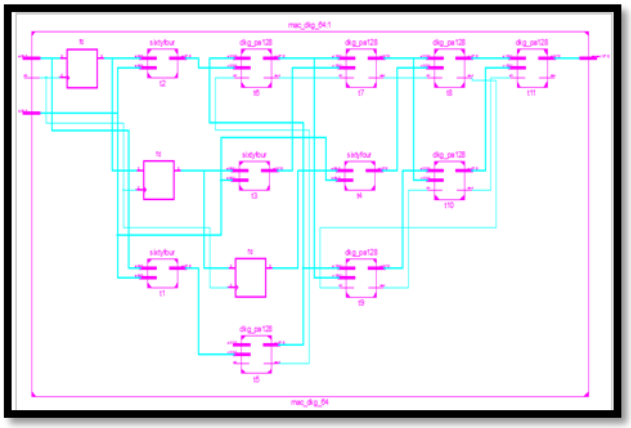


Figure 6b. RTL schematic of MAC unit.

Figure 6c. Technology schematic of64 X 64 MAC

- Zero energy dissipation
- Fan-out is not authorized
- Garbage outputs must be small
- Lowest quantum cost

5.1 DKG Gate

A 4 X 4 reversible DKG gate that preserve work singly as a reversible full adder and parallel adder is shown in below Figure 5[21]. If input A is zero, the DKG gate performed Full adder operation, and if input A is 1 then reversible logic gate performed Full subtractor operation[10,19].

5.2 Accumulator Stage

Accumulator is also one of the most important block in MAC design. In this method the result of the multiplier

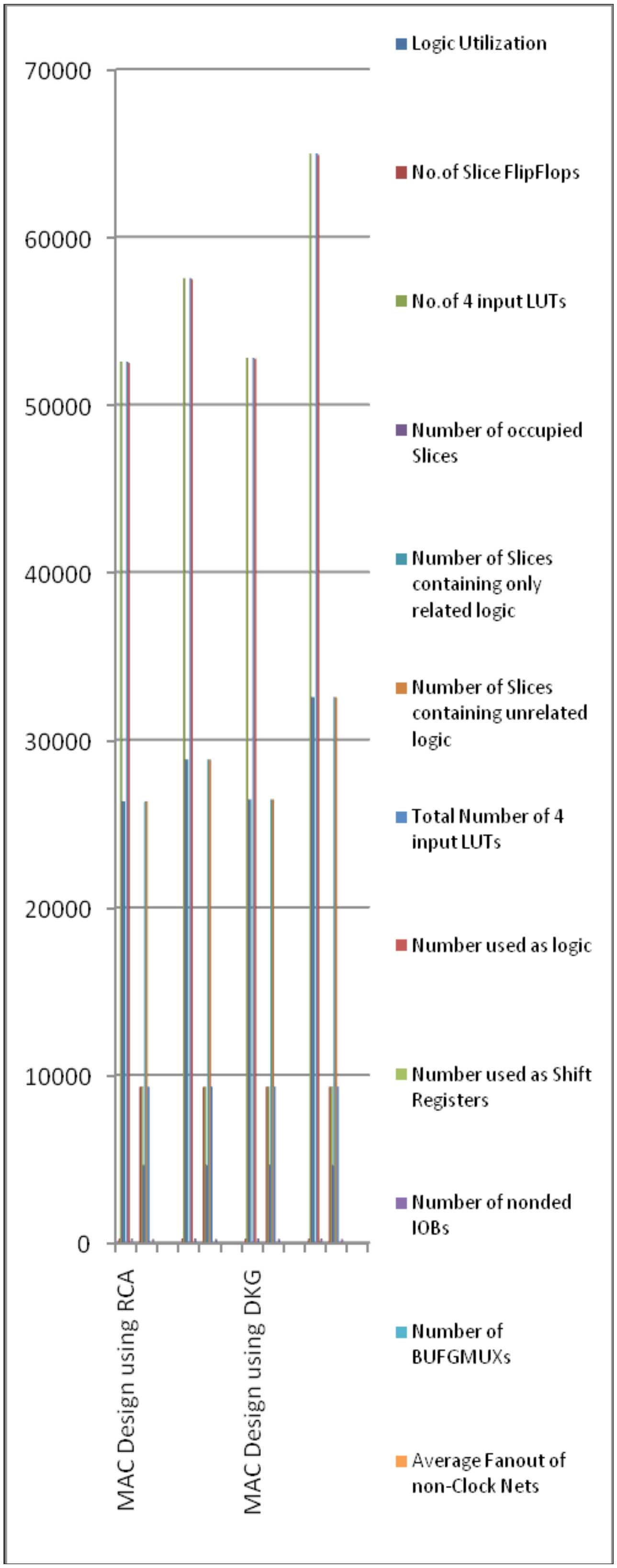


Figure 7. Synthesis report of 64-bit MAC using Vedic Multiplier using RCA,DKG and KSA Reversible logic gates.

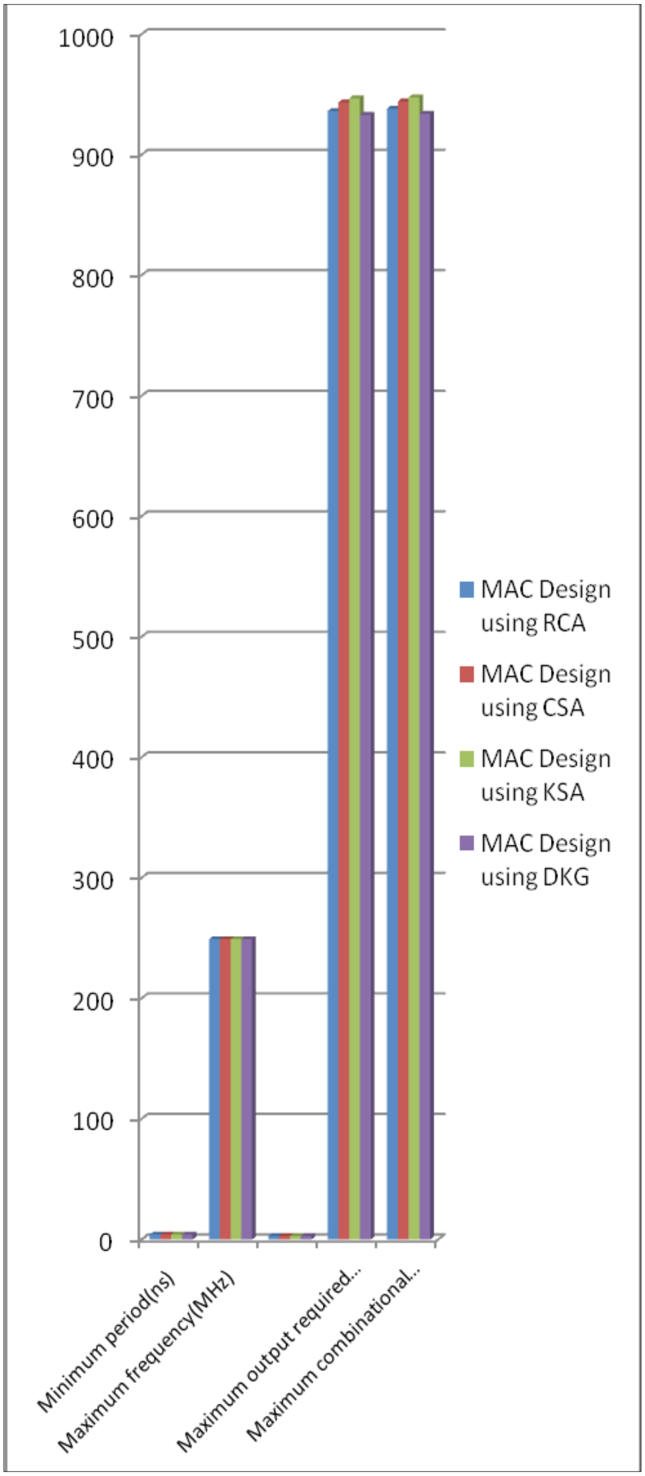


Figure 8. Delay Analysis report of 64-bit MAC using vedic multiplier using RCA,DKG and KSA reversible logic gates.

is stored in accumulator.64 X 64 multiplier gives result of 128-bit output. Sometimes if carry generated it will give 129 bit output. So 129-bit accumulator designed to store result of the multiplier.

6. Results and Discussion

The modified 64-bit multiplier using Vedic multiplier and DKG adder is fast and design of MAC done using Xilinx. This design is implemented in Verilog code using Xilinx. The below Figure 6(a) and 6(b) shows the RTL Schematic of the proposed design.

Figure 6(c) shows 64 X 64-bit MAC unit design using Vedic Multiplier and DKG gates.

Figure 7 shows comparison between MAC design unit using different Adders. The number of LUTs and utilization of logic blocks in MAC design using CSA, RCA, KSA will be greater than DKG and speed is also more in MAC design using DKG. But it will take more area.

Compare to array multipliers, baugh wooley multipliers and booths multipliers Vedic multipliers requires less area and performs operations at high speed.

Figure 8 shows the statistics results of MAC design Vedic Multiplier with different adders. In which DKG Adders has moderate delay. But it consumes very less power and it can be designed in small area.

Table 1 describes the number of adders and multipliers requires in different approaches.

Table 1. Comparison of no of additions and multiplications required in various multipliers

Multiplier	8 X 8 Bit	16 X 16 bit	32 X 32 Bit
Conventional	64M	256M	1024M
	56A	240A	1022A
Vedic Multiplierusing RCA	8M	16M	32M
	4A	8A	16A
Booth Multiplier	40M	96M	288M
	26A	72A	243A
Vedic Multiplier with KSA	8M	17M	35M
	4A	7A	13A
Vedic Multiplier with DKG	8M	17M	35M
	2A	5A	11A

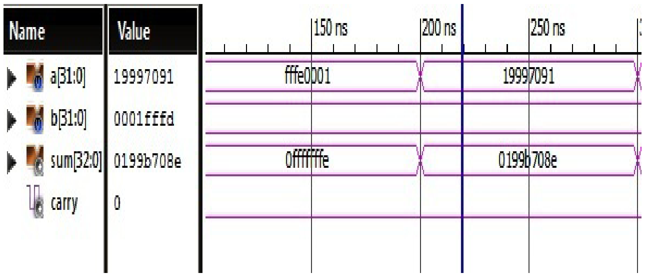
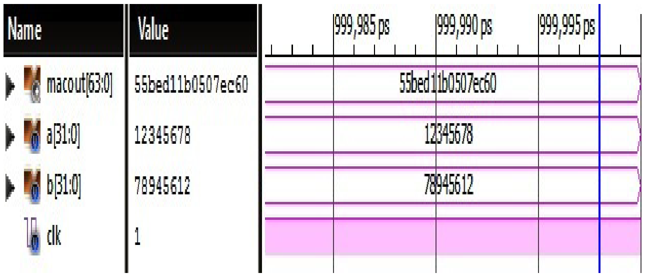


Figure 9. Simulation result of Adder.



Name	Value
macout[63:0]	55bed11b0507ec60
a[31:0]	12345678
b[31:0]	78945612
clk	1

Figure 10. Vedic multiplier result of 64-bit MAC unit.

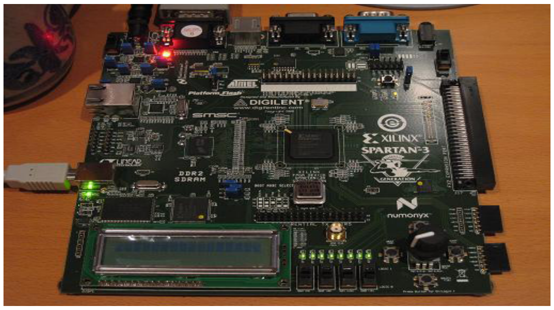


Figure 11. Vedic Multiplier result of 64 bit MAC unit on FPGA.

Figure 9 shows that simulation result of DKG adder. It is a 32-bit adder. In this design we used two 64 bit adders. This adder has two inputs a and b, two outputs sum and carry. For adder a =19997091 and b= 0001fffdapplied.Which results sum is 0199b708e and carry is 0.

Figure 10 shows the simulation result of 64-bit MAC design unit. For this design we applied two inputs. In which values are a=12345678 and b=78945612 and it will give result of 55bed11b057ec60.

7. Conclusion and Future Scope

The results of this proposed 64 bit Urdhava Triyagbhayam Vedic multiplier with DKG adder are quite good. Design of MAC unit structure and its performance has been scrutinizing for all the blocks. Therefore, the 64-bit Urdhava Triyagbhayam sutra Multiplier and reversible logic is the best in all aspects like speed power product, delay, area and complication as compared to all other architectures which are shown in table 2. By Combining the Vedic and reversible logic will direct to new and competent attainments in developing various fields of digital signal processing Applications.

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