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A Comparative Study of High Speed CMOS Adders using Microwind and FPGA

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Abstract

In the current semiconductor technology evolution, there is a huge demand in designing a low power, high speed adders with less area. As adders are essential components in the data-path of any computer system, adder modules are needed to be enhanced for better performance. One such efficient adder implementation is the Carry Look-Ahead Adder (CLA) which is designed to overcome the latency introduced by rippling effect of carry bits in a conventional Ripple Carry Adder (RCA). Further, the use of this CLA module in the place of Ripple Carry Adder module inside a Carry Select Adder (CSEA) is proposed for increased speed. Also, a novel implementation of adder, making use of the fact that the sum and carry are compliment of one another, except when all the inputs are same is presented. Simulation results show that a 4-bit carry select adder provides a better performance at the cost of power dissipation as 89.211 µW compared with 38.414 µW by a ripple carry adder with 0.12 µm technology processes. In this study, these high speed adders are implemented with the help of the Digital Schematic (DSCH) software tool, Micro wind layout editor tool and Quartus II synthesis software tool. This Quartus II synthesis tool is used for the implementation of adders on Altera EP2C20F484C7 FPGA device. These kinds of adders are further to be extended to build high-speed multipliers which are most important for the applications like digital signal processors, microprocessors, etc.

Keywords: Altera FPGA, Carry Look-Ahead Adders, High Speed Adders, Reduced Full Adder, VLSI

1. Introduction

Very-Large-Scale Integration (VLSI) is the process of creating an Integrated Circuit (IC) by combining thousands of transistors into a single chip[1]. Most chips are built from a collection of subsystems: adders register files, state machines and so on. For designing a chip, we must properly design each of the major components. It is hence essential to study the individual sub-systems. For most sub-systems, there exists a family of designs, each of which performs the same basic function, but with different area or delay trade-offs. Having access to a variety of ways to implement a function gives us architectural freedom[2].

Arithmetic components are fundamental to many systems such as addition and multiplication. The differing requirements within various applications have resulted in existence of a number of architectures. The choice of algorithm and hence the architecture followed by the identification of suitable circuits that matches the algorithm requires careful selection of basic primitives[3].

It is important to optimize adder circuits for enhanced performance. This optimization can be either done at logic or at circuit level. Logic-level optimizations try to rearrange the Boolean equations so that a faster or smaller circuit is obtained. One such method is the Carry Look ahead Adder (CLA), which is presented in this study. Circuit level optimization manipulates transistor sizes

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and circuit topology optimizes speed[3]. Our work presents the design and performance of various high speed adders using CMOS, transmission gates and pass transistor circuits. The schematic design is further converted into prefabrication layout. Simulation of the schematic and layout realizations of the adder is performed and results are discussed using Micro wind and DSCH[4,5].

The principal objective of this study is to introduce novel methods of building high speed adder architectures. The Section 2 deals with the basic structures of various high speed adders used in general. This basic analysis allows us to compare their efficiencies. The Section 3 deals with the efficient implementation of these modified adders in the construction of various adder circuits. Simulation results and the conclusion are obtained in the Section 4 and 5 respectively.

2. High Speed Adders

2.1 Carry Look Ahead Adder (CLA)

The linear growth of adder carry-delay increases as the number of input bits increases. This limitation is overcome by the Carry Look Ahead adder where the carry bits are computed directly from the adder inputs[6]. Carry Look ahead Adder is based on the two additional signals that must be computed for every node. The general block diagram of a CLA is shown in Figure 1[3]. The G signal means that the section will generate the carry bit for the next section, regardless if it gets the carry bit from the lower section or not. G signal can be computed with AND logic gate. The carry propagation signal P means that the section would not generate the carry bit itself but will pass through the carry bit (if any) from the lower section.

G_i is known as the carry Generate signal since a carry (C_{i+1}) is generated, whenever $G_i = 1$, regardless of the input carry (C_i)[7], as in

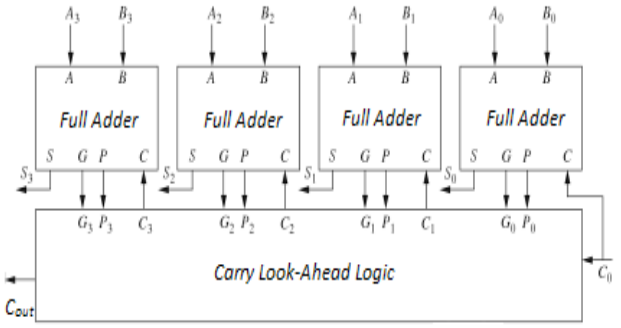

Figure 1. Block diagram of 4-bit CLA.

$$Gi = A_i . B_i \quad (1)$$

P_i is known as the carry propagate signal since whenever

$P_i = 1$, the input carry is propagated to the output carry, i.e., $C_{i+1} = C_i$[7], as in

$$Pi = A_i \oplus B_i \quad (2)$$

2.2 Carry Select Adder (CSLA)

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. The construction of CSLA is such that two ripple-carry adder structures are built, one with a zero carry-in and the other with a one carry-in. This is repeated for a certain sized adder. The general block diagram of a CSLA is shown in Figure 2[6]. The previous carry then selects the appropriate sum using a multiplexer. The main advantage of proposed CSLA is its reduced propagation delay characteristics. This is realized by the use of parallel stages that results from multiple pairs of ripple carry adder[8].

2.3 Carry Save Adder (CSA)

A Carry Save Adder is a set of one-bit full adders, without any carry-chaining, is constructed as shown in Figure 3[6]. An n-bit CSA receives three n-bit operands and generates two n-bit result values. Its two outputs are then summed by a traditional carry-look ahead or ripple-carry adder, thus the sum of all three inputs is obtained[2,9]. Doing this way, addition can be implemented in log m sums, where m is the number of input bits. The amount of circuitry

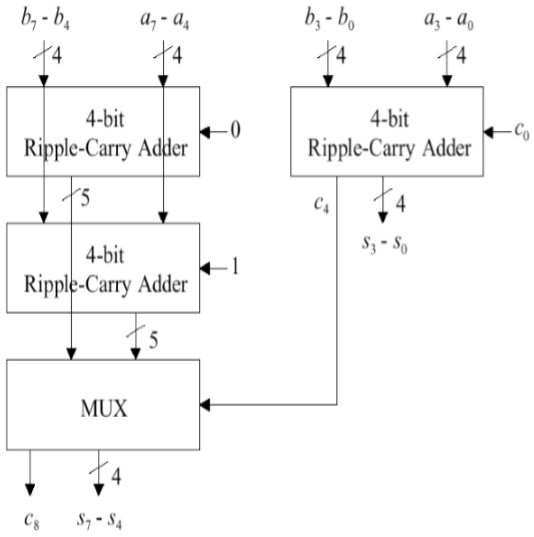

Figure 2. Block diagram of 8-bit CSLA.

is much less than a carry-look-ahead adder. The most important application of a carry-save adder is to calculate the partial products in integer multiplication[10,11].

2.4 Reduced Full Adder (RFA)

In Ripple Carry Adder there is a need to compute carry at each stage which increases the delay time. Whereas the CLA which eliminates the increase in delay, there is a logarithmic ordered delay at the expense of more gates. We use recursive algorithm in implementing the CLA which reduces the number of gates by eliminating the need to compute carry at each stage. This new implementation is called Reduced Full Adder, which is shown in Figure 4.

3. Implementation using DSCH and Microwind

Here we have implemented various adders such as Carry Look-Ahead Adder using Reduced Full Adder, Carry Select Adder using Carry Look-Ahead Adder, determination of sum and carry using multiplexers. Such implementations help in enhancing the performance of the general adder systems.

3.1 Sum and Carry using Multiplexers

In the determination of sum and carry expression we have introduced a novel method by using multiplexers as a key component. For various combinations of inputs we have established logic such that sum and carry can be determined in a much efficient manner. The initial step involves considering the two special cases in which all the three inputs are the same as the sum and carry. Then, general expression for sum is determined using the EXOR logic of any two inputs followed by the multiplexers. The carry is generally the inverse of sum expression. The schematic of this circuit, constructed in DSCH[10], using logic gates is shown in Figure 5.

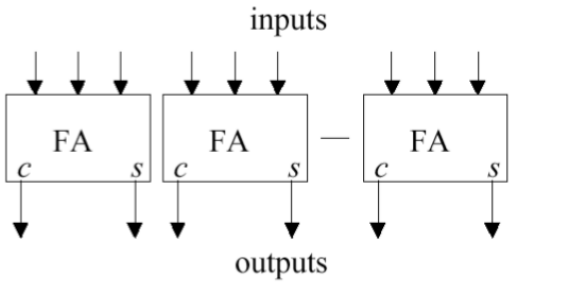

Figure 3. Block diagram of CSA.

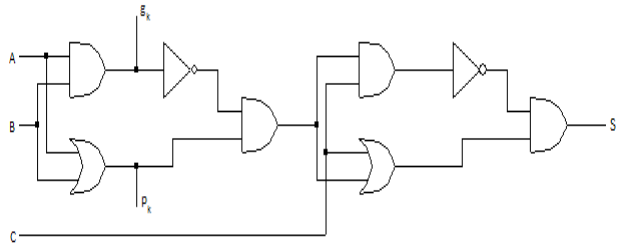

Figure 4. RFA using Logic Gates.

3.2 Carry Look Ahead Adder using Reduce Full Adder

The conventional Carry Look Ahead Adders using a ripple carry adder involves the computation of carry in each stage along with the generate and propagate terms[11,12]. By using reduced full adder we compute the generate and propagate terms alone. The carry term is computed using a separate logic circuit called the Carry Look Ahead Generator (CLG). This carry generator circuit is shown below in Figure 6.

3.3 Carry Select Adder using Carry Look Ahead Adder

The Conventional Carry Select Adder uses two ripple carry adders for the zero and one carry bits[13]. Instead, we use Carry Look Ahead adders in place of the ripple carry adders, as shown in Figure 7. This increases the efficiency and reduces the propagation delay time as well. When a CLA using reduced full adder is used, the propagation delay is further reduced.

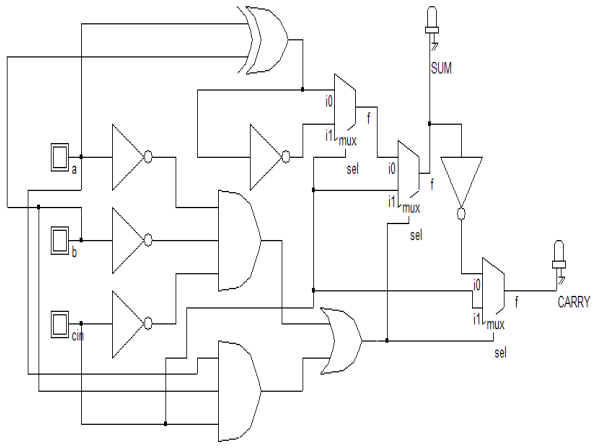

Figure 5. Full Adder using Multiplexers.

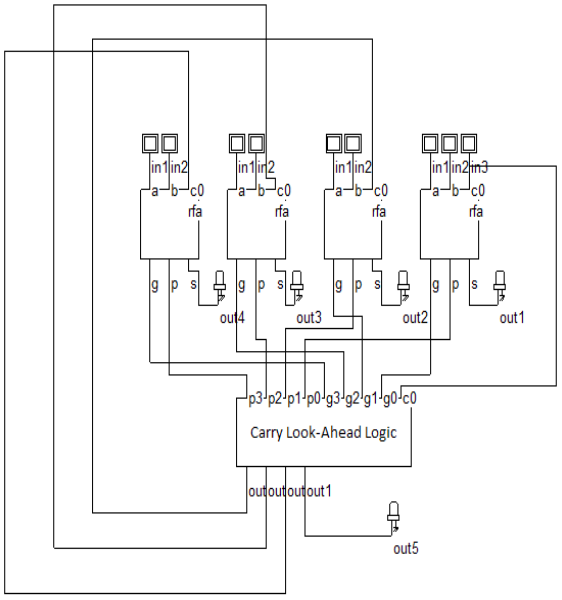

Figure 6. 4-bit CLA using RFA block.

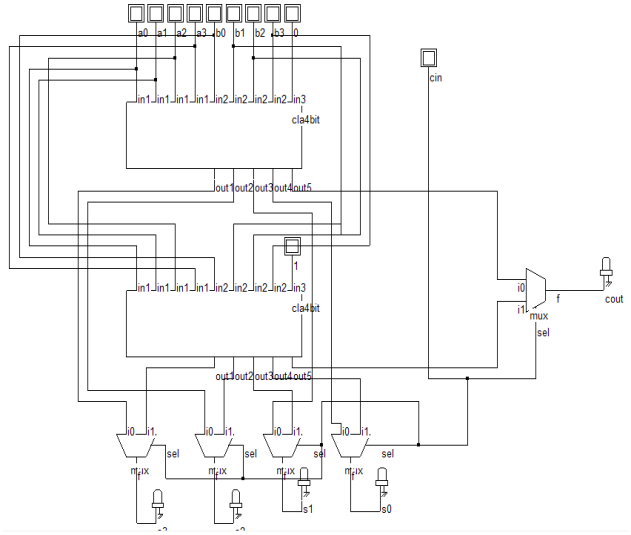

Figure 7. 4-bit CSLA using CLA block.

4. Simulation Results

Logic level implementations are done using the software DSCH which is a schematic editor. The functional verification is done even on the layout generated by a Micro wind tool, which is a layout editor tool. The determination of power dissipation and the number of transistors are done using the Micro wind tool.

The simulation results of the adder circuits are shown in the following figures from which we can estimate various parameters such as power dissipation, number of transistors used in the system, total surface area etc. which helps in determining the performance of the system.

Figure 8 shows the simulation result of a 4-bit CLA in Altera DE1 FPGA board. The two inputs applied were 3 and 2 in four bits in binary (0010 and 0011) respectively. The adder's final output in binary is 0101 which has been converted to a numeral and displayed using a 7 segment display. Figure 9 shows the timing diagram result of a full adder using mux and the Figure 10 shows the functional verification result of 4-bit CLA using RFA.

The RTL view of a 4-bit CLA is generated using Quartus II tool and is shown in Figure 11. The compilation report of the same is extracted and presented in Figure 12. Similarly, the compilation report of CSLA was also extracted and it is found that it uses 38 logical elements and a total of 21 pins. The number of logic elements used here are less due to the simple design. The functional verification of a CSLA using CLA is depicted as timing diagram in Figure 13 using the DSCH simulation tool.

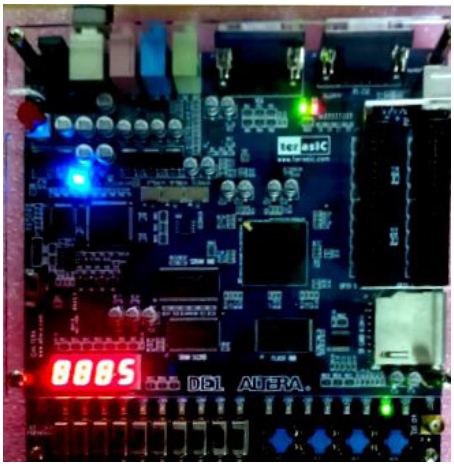

Figure 8. Implementation of 4-bit CLA in ALTERA board.

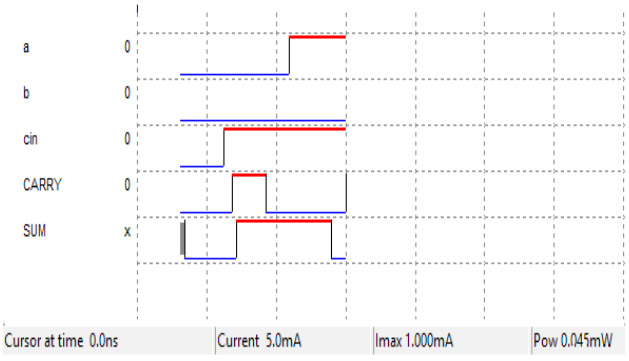

Figure 9. Timing diagram for Full Adder using multiplexers.

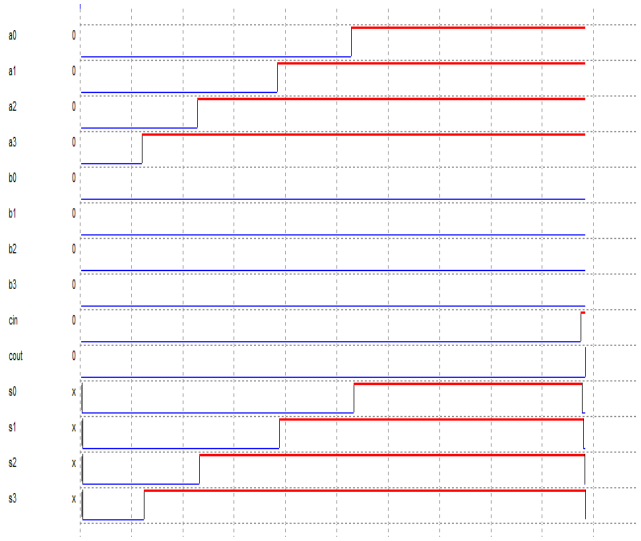

Figure 10. Timing diagram for 4-bit CLA using RFA.

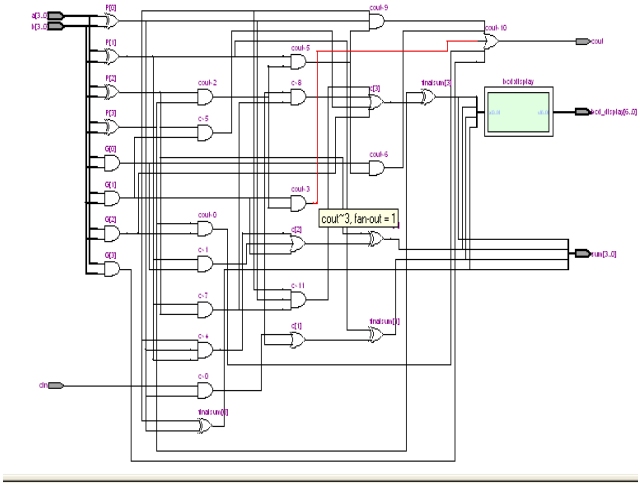

Figure 11. RTL Netlist diagram of 4-bit CLA.

Flow Status	Successful - Tue Feb 03 16:33:42 2015
Quartus II Version	7.2 Build 151 09/26/2007 SJ Web Edition
Revision Name	final
Top-level Entity Name	cla
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	N/A
Total logic elements	33
Total combinational functions	33
Dedicated logic registers	0
Total registers	0
Total pins	21
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Figure 12. Compilation report of 4-bit CLA.

The performance metrics of various adders are determined using Microwind tool and are tabulated. Table 1 contains the surface area and the number of transistors of Ripple Carry Adder, Carry Look-Ahead Adder and Carry Select Adder. As expected, CSLA surface area and the transistors count are higher than the other two. Since all the circuits follow the static complementary design style, nMOS transistor count is the same as the count of pMOS transistors. Table 2 contains the power dissipation of the same for various foundry lengths. Since the layout area and the transistor count are maximum for the CSLA, this circuit consumes more power dissipation than other.

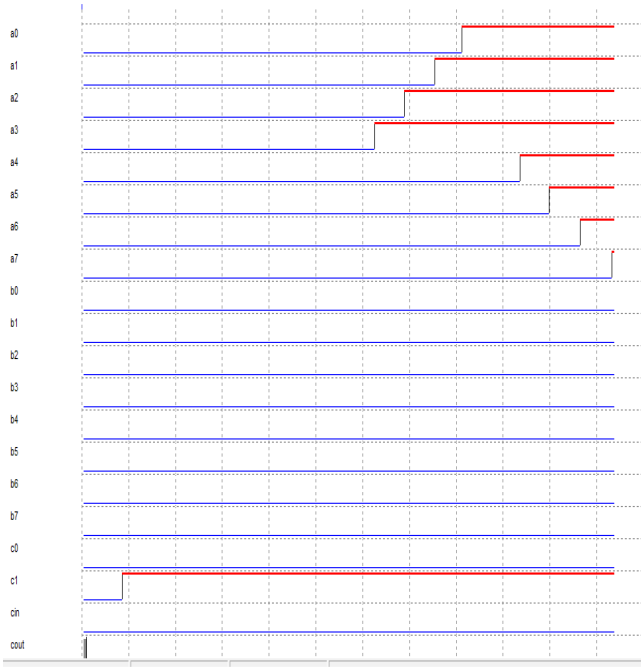

Figure 13. Timing diagram of CSLA using CLA.

Table 1. Surface area and transistor count results

Type of Adder	Surface Area (μm²)	No. of nMOS and pMOS transistors
RCA	1211.5	108
CLA	2077.5	168
CSLA	3665.5	223

Table 2. Power dissipation of various adders

Type of Adder	Power dissipation (μW)		
	0.18 μm	0.12 μm	0.1 μm
RCA	278	38.414	25.593
CLA	226	28.807	26.200
CSLA	694	89.211	64.144

5. Conclusion

In this study, we have designed and simulated various adders like Full Adder, Ripple Carry Adder, Carry-Look-Ahead Adder, Carry-Select Adder using CLA by using DSCH and Micro wind. The simulated results are verified and the functionality of high speed adders and the performance metrics like area and power dissipation are analyzed. These design logics can be used as modules to design higher order adders like 32-bit and 64-bit adders to enhance the performance.

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