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Design and Implementation of Low-Power, Area-Efficient FIR Filter using Different Distributed Arithmetic Techniques

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Abstract

Background: Distributed Arithmetic (DA) technique is a bit serial operation used to perform vector to vector multiplication in convolution, which is an essential operation in digital filters. This paper presents realization of Finite Impulse Response (FIR) filters using six different DA techniques namely conventional DA, Modified DA (MDA), Offset Binary Coding DA (OBC-DA), Offset Binary Coding Modified DA (OBC-MDA) and LUT-Less DA. **Methods:** A novel DA method is also introduced which is a combination of multiplexers and Look-Up-Tables (LUT). In DA based FIR filter architecture the partial products of the FIR filter coefficients are pre-calculated and stored in LUTs. The filtering operation is done by shift-accumulation unit. **Findings:** The designs are simulated using Xilinx ISE and synthesized in Cadence RC using 180-nm technology library. From synthesis reports, it is found that for 4-tap FIR filter, Modified DA consumes 30% less power and 40% less area, whereas for 8-tap FIR filter the saving in power consumption is 30-80% and 35-80% in area. **Conclusion:** Compared to all the DA techniques mentioned, MDA requires least area and least power consumption because of its less memory requirement. All architectures are designed for 4-tap and 8-tap FIR filters.

Keywords: Distributed Arithmetic, FIR Filter, LUT-Less DA, Modified DA, MUX-LUT DA, OBC-MDA, Offset-Binary Coding DA

1. Introduction

Digital filters are used in many applications such as computer vision, audio processing, image processing and communications. FIR filters are important blocks in Digital signal processing systems and used in digital communication because of its simple structure, high stability, linear phase and non-recursive nature. The most power consuming block in FIR filter is multiplier and multiplication operation is nothing but generation and addition of partial products. Generation of partial products in the multiplier consumes huge power as well as area. Reducing the power consumption of the multiplier block, results in reducing the power consumed by FIR filter itself. Distributed Arithmetic[1] (DA) is one of the efficient techniques used to reduce the power consumption in FIR filter by eliminating the multiplier.

DA was first introduced by Croisier in 1973 and later popularized by Peled and Liu. DA is used to compute the inner product of two vectors which includes most of the process workload. DA[2] is a multiplier less technique and it replaces the multipliers with Look-Up-Tables (LUT). The basic operation of DA is to accumulate the pre-computed partial product of filter[3] coefficients, which are stored in ROM look-up-table and shift them sequentially. The number of clock cycles required to produce the output depends on the bit length of the input sample. The memory requirement of DA[4] based implementation of FIR filter increases exponentially with the increase in filter order. Techniques such as OBC-DA[5] method, LUT-Less DA method, ROM decomposition[6] (Modified DA), MUX-LUT DA method can eliminate the large memory requirement problems of conventional DA.

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OBC-DA reduces the memory size to half of the actual memory size because the first half of the LUT values are mirror image of the other half of the LUT values, thus OBC-DA can reduce the memory size from 2^N to 2^{N-1}. In LUT-less DA technique LUT's are replaced by multiplexers to reduce the memory requirement of conventional DA. The MUX-LUT DA technique structure is a combination of Multiplexers and ROM Look-up-tables to reduce the area and power consumption. In ROM decomposition DA i.e. Modified DA[7], splitting of ROM size is done to reduce the memory size, thus by using these techniques less area requirement and low power consumption of FIR filter is achieved.

The remaining part of the paper is organized as follows, section 2 discusses the background of conventional DA based FIR filter, section 3 explores the MDA, OBC-DA, OBC-MDA, LUT-Less DA and MUX-LUT DA technique, section 4 describes the performance comparison of different DA based implementation of FIR filter, section 5 gives the conclusion.

2. Design of DA based FIR Filter

Distributed arithmetic is one of the most efficient techniques to implement FIR filter. An FIR filter of length N is represented in Equation (1)

$$y(n)=\sum_{i=0}^{N-1} c(i)x(n-i) \tag{1}$$

Where c(i) are the filter coefficients and x(n-i) is input data. The implementation of conventional DA based 4-tap FIR Filter is shown in Figure 1.

The input sample can be represented in B-bit scaled two's complement form as shown in Equation (2).

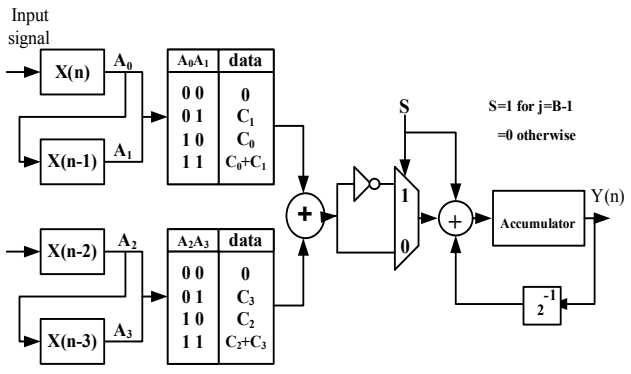

Figure 1. Block diagram of Conventional DA based implementation of 4-tap FIR filter.

$$x(n-i)=-a_{i,B-1}+\sum_{j=1}^{B-1} a_{i,B-1-j}2^{-j} \tag{2}$$

The Equation (3) can be derived by substituting Equation (2) in (1).

$$y(n)=\sum_{j=0}^{B-1} W_{B-1-j}2^{-j} \tag{3}$$

Where

$$W_{B-1-j}=\sum_{i=0}^{N-1} c_i a_{i,B-1-j} \qquad (j\neq 0)$$

$$W_{B-1}=-\sum_{i=0}^{N-1} c_i a_{i,B-1}$$

For c_i(i=0, 1, 2 . . . . N-1), the terms W_{B-1-j} take only one out of 2^N possible combinations, which are precomputed and stored in LUT. The incoming bits of the input sample are stored in input buffer and at any instant of time the most recent bits of the input samples are stored in the top most registers and the previous sample bits are stored in the bottom most register. These input buffers give the address to the ROM Look-up-tables containing the partial products. The addresses are generated by taking one bit from each input sample. At the first clock cycle the least significant bits of all the input samples are taken and then the next higher order bits forms the addresses in the coming clock cycles.

The output of the LUT is shifted and then accumulated for 'B' number of clock cycles to produce one sample of output. The selection signal 'S' of multiplexer is high when the address to the LUT is formed by MSB's (j = B-1) of the input buffers, otherwise zero. The two's complement for the LUT output takes place when selection signal is high.

3. Different DA Techniques

3.1 Modified DA

The hardware requirement for conventional DA increases as the order of the filter increases. One way to reduce the area is by decomposing the ROM of N address bits into N/M groups of M bits, this results in reducing the area from 2^N to (N/M) 2^M. For four tap FIR filter conventional DA technique needs 16-ROM entries but in modified DA technique it needs 8-ROM entries with one extra adder

block. Modified DA gives greater reduction in hardware[8] and power consumption for higher order filters.

The implementation of Modified DA based 4-tap FIR Filter is shown in Figure 2.

3.2 OBC-DA

The size of the ROM is reduced to half compared to conventional DA by rewriting equation (2) as

$$x(n-i)=\frac{1}{2}\left[x(n-i)-(\sim x(n-i))\right]$$

$$x(n-i)=\frac{1}{2}\left[-\left(a_{i,B-1}-\bar{a}_{i,B-1}\right)+\sum_{j=1}^{B-1}(a_{i,B-1-j}-\bar{a}_{i,B-1-j})2^{-j}-2^{-(B-1)}\right] \quad (4)$$

The block diagram of OBC-DA based 4-tap FIR Filter is shown in Figure 3.

Choose

$$d_{i,j}=\begin{cases}-\left(a_{i,j}-\bar{a}_{i,j}\right), & j\neq B-1\\ -\left(a_{i,B-1}-\bar{a}_{i,B-1}\right), & j=B-1\end{cases} \quad (5)$$

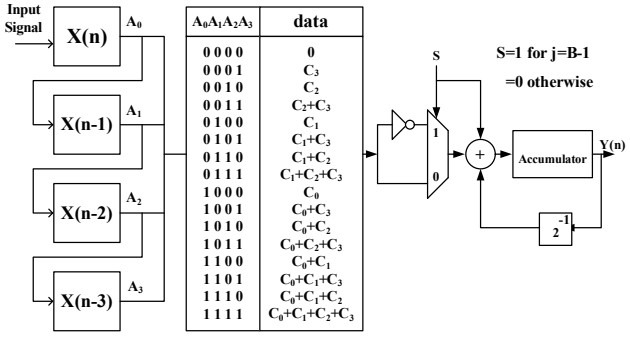

Figure 2. Block diagram of MDA based implementation of 4-tap FIR filter.

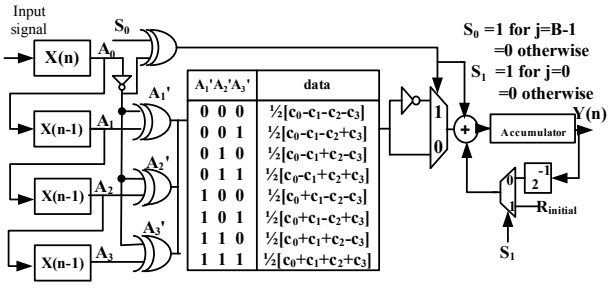

Figure 3 Block diagram of OBC-DA based implementation of 4-tap FIR filter.

By substituting Equation (4) and (5) in Equation (1), the resultant equation is as follows

$$y(n)=\sum_{j=0}^{B-1}\left(\sum_{i=0}^{N-1}\frac{1}{2}c_i d_{i,B-1-j}\right)2^{-j}-\left(\frac{1}{2}\sum_{i=0}^{N-1}c_i\right)2^{-(B-1)}$$

Here

$$R_j=\sum_{i=0}^{N-1}\frac{1}{2}c_i d_{i,j} \qquad 0\le j\le B-1$$

$$R_{initial}=-\frac{1}{2}\sum_{i=0}^{N-1}c_i \quad (6)$$

Final equation is as follows

$$y(n)=\sum_{j=0}^{B-1}R_{B-1-j}2^{-j}+R_{initial}2^{-(B-1)} \quad (7)$$

In OBC[9], the address to the LUT is obtained by the bit-level XOR operation of inverted LSB of first input sample with LSB of all other input samples. The memory requirement for LUT reduces to half compared to conventional DA architecture, but the complexity of the design increases by including XOR stage block.

3.3 OBC-MDA

The area and power consumption of the OBC-DA technique is further reduced by employing Modified DA technique in OBC scheme. The implementation of OBC-MDA based 4-tap FIR Filter is shown in Figure 4.

3.4 MUX-LUT DA

In this DA technique new method is employed i.e. Multiplexer and adder block are introduced to reduce

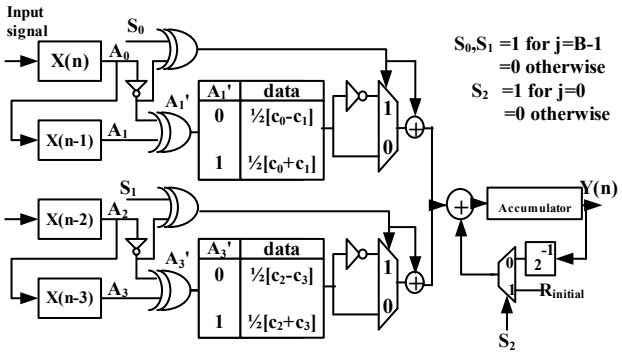

Figure 4. Block diagram of OBC-MDA based implementation of 4-tap FIR filter.

the memory size to half of the conventional DA[10] technique. This combination of multiplexer and LUT results in reducing the area and power compared to all the other DA technique except MDA. The implementation of MUX-LUT DA based 4-tap FIR filter shown in Figure 5.

3.5 LUT-Less DA

In LUT-Less DA[11] technique LUT of conventional DA architecture is replaced by multiplexers. This results in reducing the area and power consumption of the design. The implementation of LUT-Less DA based 4-tap FIR filter is shown in Figure 6.

4. Results and Discussions

In this section the results of six different DA techniques are presented. Figure 7 shows the comparison of power dissipation between all the 4-tap FIR filters.

Compared to all the DA techniques, Modified DA 4-tap FIR filter has least power consumption because it needs less adder blocks and less memory entries than all other DA architectures.

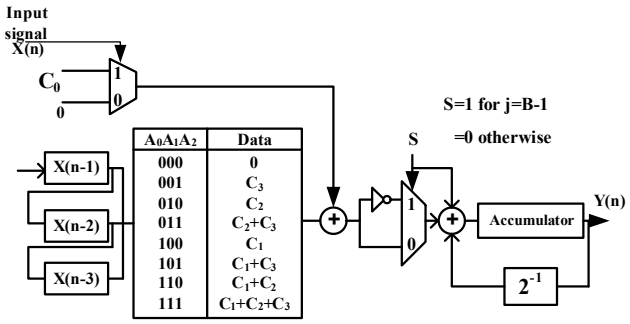

Figure 5. Block diagram of MUX-LUT DA based implementation of 4-tap FIR filter.

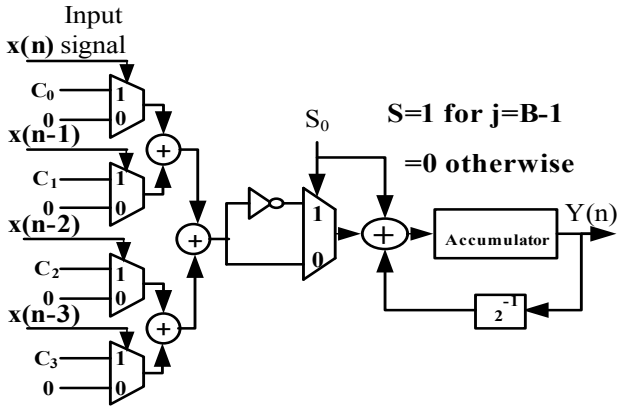

Figure 6. Block diagram of LUT-Less DA based implementation of 4-tap FIR filter.

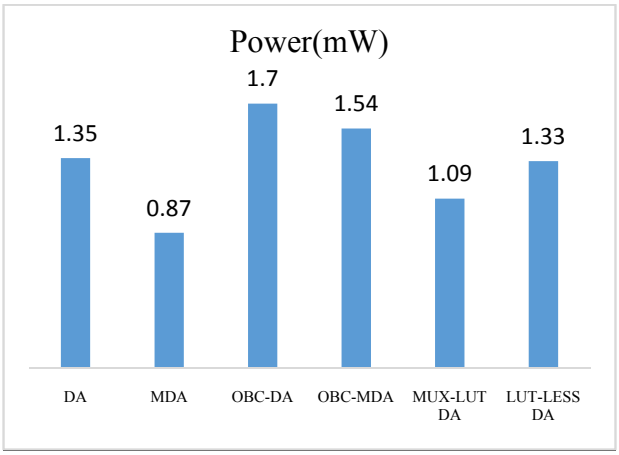

Figure 7. Power report of all DA techniques of 4-tap FIR filter.

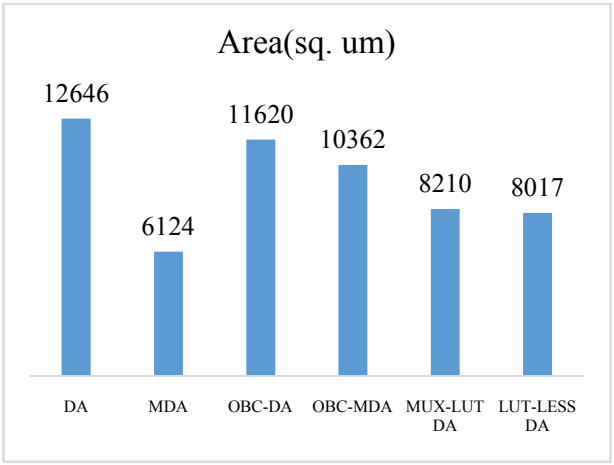

Figure 8. Area report of all DA techniques of 4-tap FIR filter.

Figure 8 shows the comparison of area requirement between all the 4-tap FIR filters.

Modified DA 4-tap FIR filter has less area requirement because it needs less memory entries to store partial products i.e. the LUT size is reduced compared to all other DA architectures.

Figure 9 shows the comparison of power dissipation between all the 8-tap FIR filters.

Modified DA based 8-tap FIR filter has less power consumption because it needs less memory requirement and less hardware among all other DA architectures.

Figure 10 shows the comparison of area requirement between all the 8-tap FIR filters.

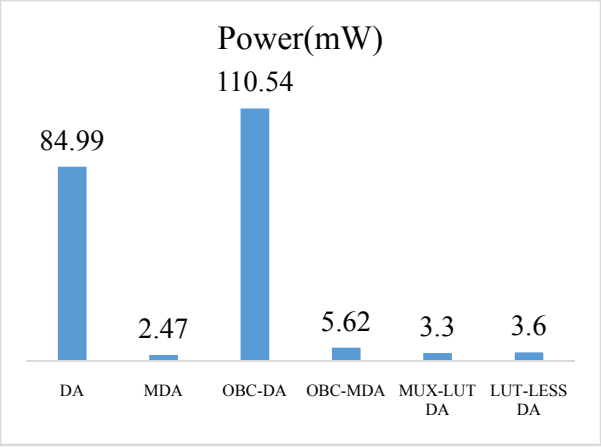

Figure 9. Power report of all DA techniques of 8-tap FIR filter.

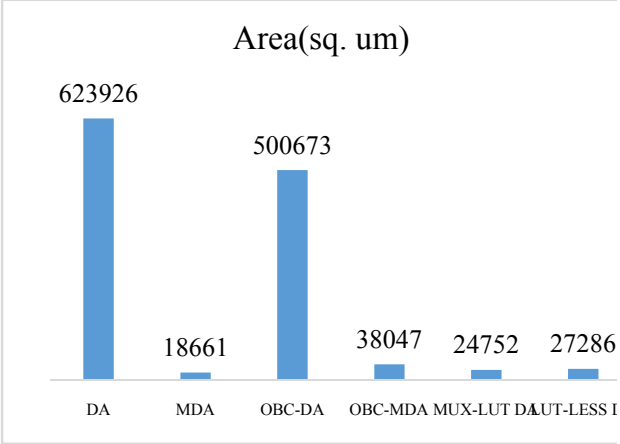

Figure 10. Area report of all DA techniques of 8-tap FIR filter.

Modified DA 8-tap FIR filter is area efficient compared to all other DA techniques because of its less hardware requirement.

5. Conclusion

In this paper, an FIR filter implementation based on DA has been presented. OBC scheme is employed in order to reduce the memory requirement, but the power consumption is increased compared to conventional DA technique. To overcome this problem, OBC-MDA technique is used, which also reduces the area. LUT-Less DA technique is employed to further reduce the area and power consumption. MUX-LUT DA technique uses combination of multiplexers and ROM Look-up tables to reduce the area utilization and power consumption. Among all the DA techniques mentioned above, Modified DA technique occupies least area and power dissipation is less because it needs less memory entries.

6. References

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