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1V Differential Input Stage with Bulk-Driven Current Mirror for Low-Voltage Operational Amplifier

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Abstract

Objectives: This paper presents the design and analysis of differential input stage to design low voltage operational amplifier, where bulk-driven MOSFETs are incorporated in the current mirror. **Methods/Analysis**: To be possible to operate circuit at lower supply voltage, body-driven transistors are used to design current mirror. Circuit is designed using 180nm (Complementary Metal Oxide Semiconductor) CMOS n-well technology and BSIM 3v3 Specter models are used to analyze the design. Performance parameters are validated by simulations. **Findings**: The amplifier shows DC open-loop gain of 44 dB. The Unity Gain Bandwidth (UGB) is 3.3 MHz with a phase margin of 87.8°. The amplifier exhibits Common-Mode Rejection Ratio (CMRR) of 62 dB. The input referred spot noise voltage at 1KHz is 42.46nV/√Hz. These results are obtained with a supply voltage of 1V. Average power consumption of the amplifier is 36.36 µW under 10 pF load condition, which makes it suitable for low voltage and low power applications. **Improvement**: Gain can be further improved by employing cascode current mirror in the presented amplifier as it will increase output impedance.

Keywords: Analog and Mixed-signal system, Bulk-driven Current Mirror, Differential Input Stage, Low-voltage Operational Amplifier, CMOS

1. Introduction

With the advancement in Integrated Circuit (IC) design and manufacturing technology, the size of electronic systems is reducing significantly. Today, most of the consumer electronic products are portable and battery operated. E.g. mobile phones, laptops, tablets, pacemakers etc. These products require low supply voltage to reduce battery power consumption and to keep battery size smaller and light weight.

Operational Amplifier (Op Amp) is the basic and most versatile building block of any analog and mixed-signal system. In last few decades, many researchers have proposed various low-voltage circuit design techniques and low-voltage architectures of Op Amp. The most prominent

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technique proposed by many researchers is bulk-driven technique[1-2], in which input signal is applied to the bulk terminal of Metal Oxide Semiconductor (MOS) transistor rather than gate terminal to mitigate the requirement of threshold voltage. Major drawback of bulk-driven circuits is, bulk-driven transistors has low Transconductance. In recent years, researchers proposed partial positive feedback incorporated in bulk-driven circuits to enhance the Transconductance of the bulk-driven transistors[3-5]. However, partial positive feedback could cause serious stability issues due to transistor mismatches and process variations[4]. Moreover, a more effective Transconductance improvement technique using quasi-floating rate differential pair for the bulk-driven amplifiers is presented in[5]. Alternate techniques to lower the supply voltage requirement includes: Dynamic level shifting[6], floating gate transistors[7], and biasing transistors in weak inversion region[8].

This paper presents design and analysis of bulk-driven current mirror and differential amplifier designed using bulk-driven current mirror. Circuit explanation and analysis of bulk-driven current mirror is given in section 2. Section 3 describes the working and analysis of differential amplifier designed using bulk-driven current mirror. Section 4 presents simulation results and work is concluded in section 5.

2. Bulk-Driven Current Mirror

Current mirror is fundamental circuit, used in analog and mixed-signal systems for copying or amplifying current. It is also widely used for biasing and as an active load for differential amplifiers, nevertheless it converts differential input signal into a single ended output signal. It has high impedance output node. Even if there is variation in load, output current of current mirror remains constant.

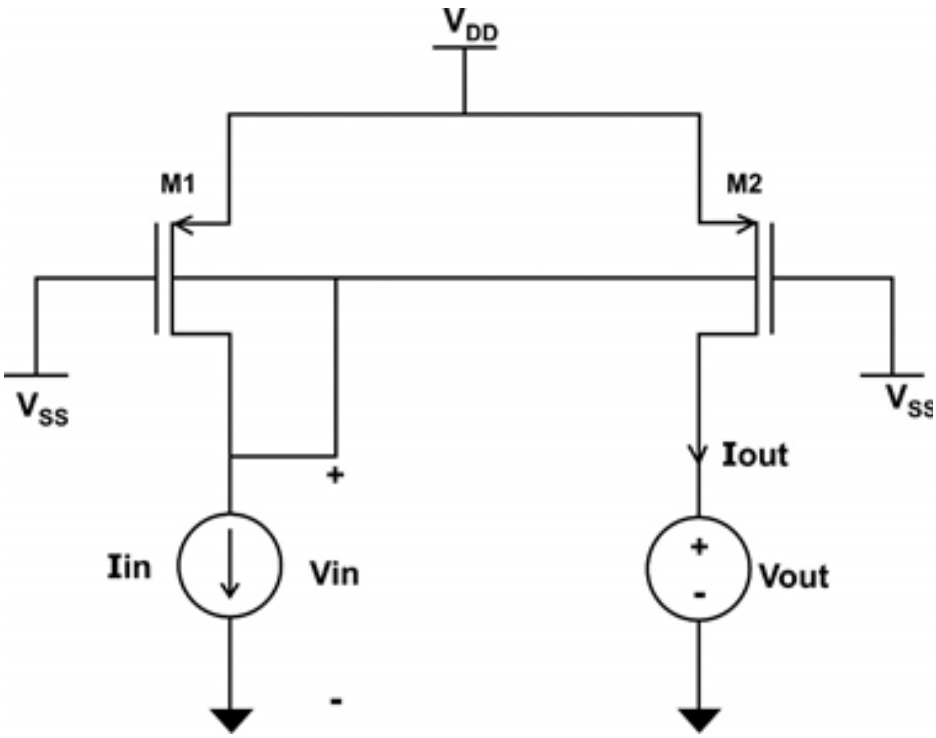

Figure 1. PMOS bulk-driven current mirror.

Input and output current linearity of gate-driven current mirror is good as both transistors are operated in strong saturation region. However, in this topology, an input voltage (V_{GS}) must be greater or equal to threshold voltage (V_T) to switch-on the input transistor. Thus one V_T drop occurs in the signal path. If we apply input signal to the bulk terminal of the MOSFET instead of gate terminal, then NMOS transistor can even switch-on with zero or negative gate-to-source voltage (V_{GS}). Thus additional threshold voltage requirement can be removed from signal path. This technique thus helps to design low-voltage CMOS circuits.This method can also be used to design low-voltage current mirror, where we can apply input to the bulk terminal of the transistors in the current mirror. Thus this configuration can work at lower supply voltage compared to its gate-driven counterpart. In recent years, several bulk-driven current mirror architectures are presented and analyzed by the researchers[9-10].

A simple PMOS bulk-driven current mirror[9] capable to work on 1V supply is shown in Figure 1. In this, bulk and drain terminals of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are shorted instead of gate-drain terminals, which helps to operate it at lower supply voltage.

Bulk terminal of M1 and M2 are also shorted together. As M1 and M2 are PMOS transistors, their gates are tied to the most negative potential in the circuit in order to form a conduction channel between source and drain. It is necessary to use CMOS n-well technology to fabricate PMOS bulk-driven transistor.

To derive the output current expression of the current mirror shown in Figure 1, let us first consider the region of operation of both the transistors. As M1 is bulk-drain connected and bulk of both transistor are shorted together, $V_{SB1} = V_{SB2} = V_{SD1}$. V_{SB1} must be positive and small enough to ensure negligible amount of current flows through the

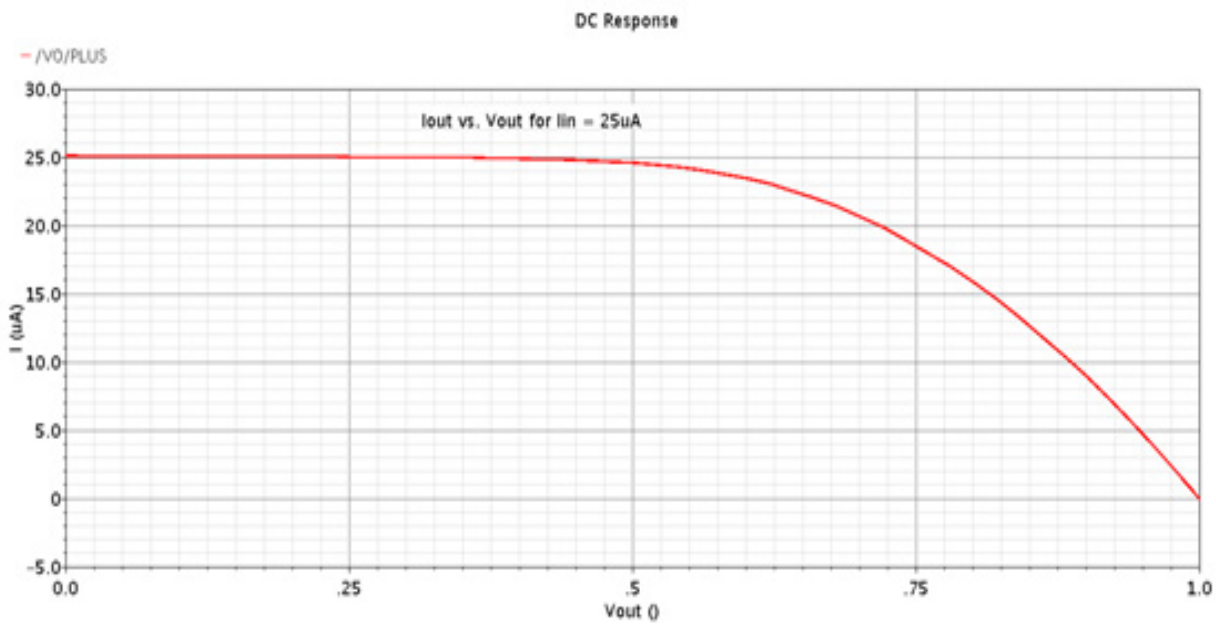

Figure 2. Output current characteristics of PMOS bulk-driven current mirror.

bulk. Thus, M1 operates in linear region as V_{SD1} is less than $V_{SD, sat}$. However, M2 can operate in saturation region as V_{SD2} can exceed $V_{SD,sat.}$ Aspect ratio of M2 has to be chosen carefully to ensure saturation mode operation of M2.

The dependency of output current on input current is given as[9]

$$I_{SD2} = I_{out} = \frac{\beta_2}{2}\left(\frac{I_{in}^2}{\beta_1^2 V_{SD1}^2} + \frac{I_{in}}{\beta_1} + \frac{V_{SD1}^2}{4}\right)(1 + \lambda V_{SD2}) \quad (1)$$

Where $\beta = \mu C_{ox} W/L$

Equation (1) shows that if sizes of M1 and M2 are chosen equal, then output current is not equal to the input current. Hence, better current matching can be achieved by proper selection of unequal sizes of M1 and M2.

The small-signal input and output impedance of bulk-driven current mirror is given by equation (2) and (3) respectively[9].

$$r_{in} = \frac{1}{g_{mb}} = \frac{1}{g_m}\left(\frac{2\sqrt{2\phi_F - V_{BS}}}{\gamma}\right) \quad (2)$$

$$r_{out} = \frac{1}{\lambda I_{DS}} \quad (3)$$

Figure 2 shows simulated output voltage as a function of output current of the bulk-driven current mirror. Output voltage is swept from 0 to 1V. As indicated by equation (1), aspect ratios of transistors M1 and M2 should be unequal to have equal input and output currents. Hence, the channel width to length ratio of M1 and M2 are chosen 10 and 2.6 respectively. Channel length of M2 is chosen double than the length of M1 to mitigate the effect of channel length modulation.

It can be observed from Figure 2, for V_{out} greater than 0.5V, output current does not follows the input current and drops significantly as M2 enters into the linear region.

3. Differential Input Stage with Bulk-Driven Current Mirror

Differential input stage is the basic analog building block and the first stage of the operational amplifier or operational transconductance amplifier. This stage decides primary gain and unity gain bandwidth of the operational amplifier. Transconductance of the input transistors plays an important role in achieving large gain and unity gain bandwidth. However, to have any input common mode range, the effective minimum supply voltage required for the proper operation of differential amplifier with conventional current mirror is

$$V_{DD}(min) = V_{GS} + V_{DS}(sat) = V_T + 2V_{DS}(sat) \quad (4)$$

The threshold voltage (V_T) factor given in equation (4) can be removed from minimum supply voltage requirement, if we employ bulk-driven current mirror as a load of the gate-driven differential amplifier instead of gate-driven current mirror. Thus, this architecture can work at lower supply voltage. The schematic of differential input stage with bulk-driven PMOS current mirror as a load is shown in Figure 3.

The circuit is designed with a bias current of 25 µA and supply voltage of 1V. Table 1 shows channel width to length ratios of each transistor in differential input stage.

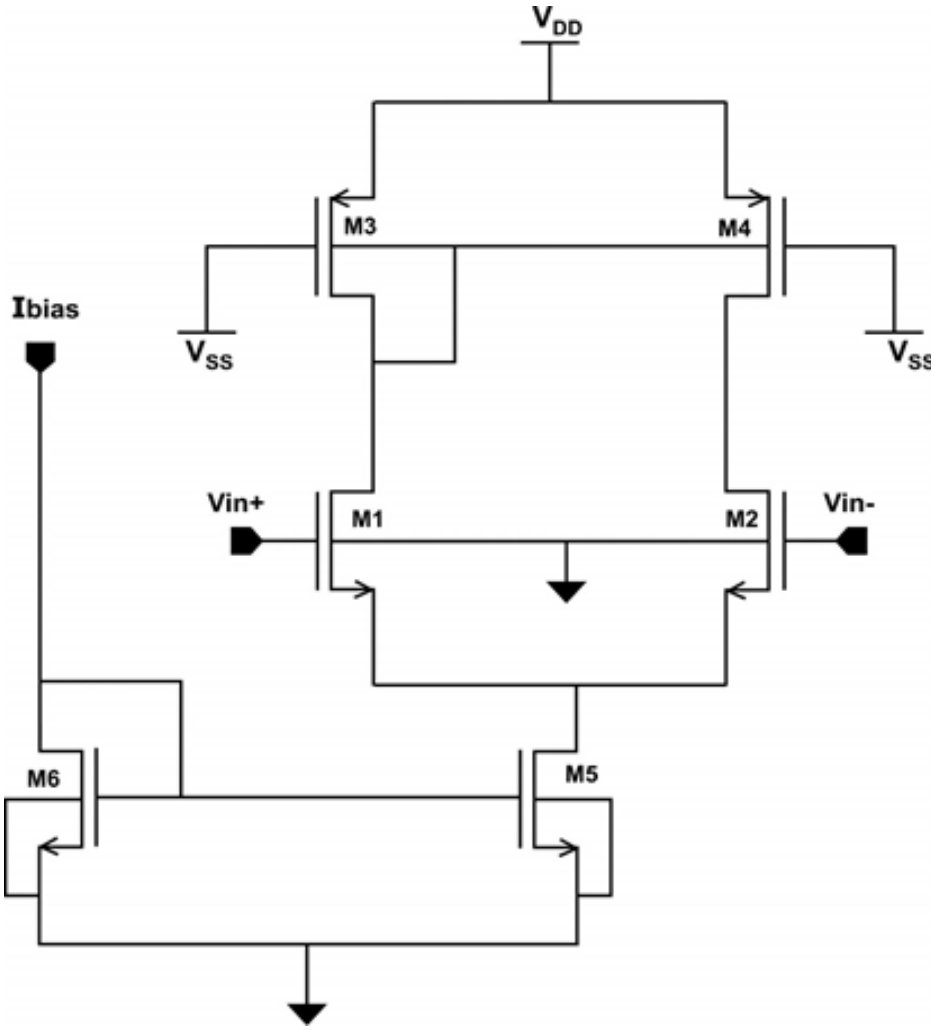

Figure 3. Differential input stage with bulk-driven current mirror.

Table 1. Channel width to length ratios of the transistors

Transistor	Channel width (μm)	Channel length (μm)
M1, M2	10	1
M3	20	2
M4	10	4
M5, M6	12	1

4. Simulation Results

The differential amplifier with bulk-driven current mirror is designed using 180 nm standard n-well CMOS process. Circuit simulations are performed using BSIM3v3 Spectre models. Circuit is simulated with a load capacitance of 10 pF.

4.1 Open-Loop Configuration Results

Figure 4 shows small-signal AC analysis characteristics of the differential input stage. It can be inferred from the response, small-signal gain of the amplifier is 44 dB, which is high enough for any single stage amplifier working with

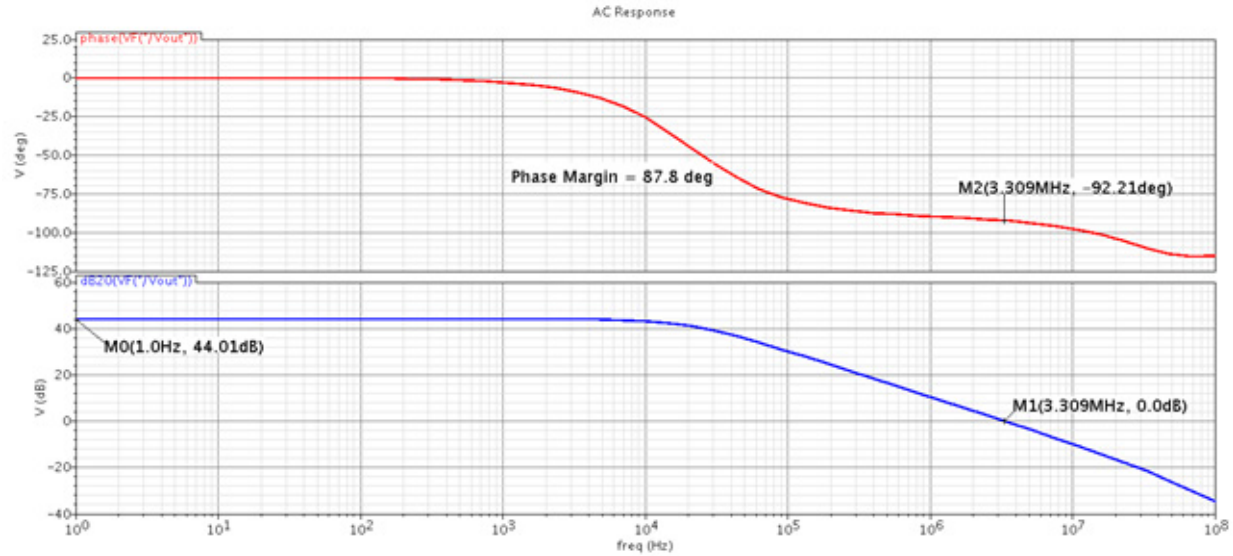

Figure 4. AC response of the differential input stage.

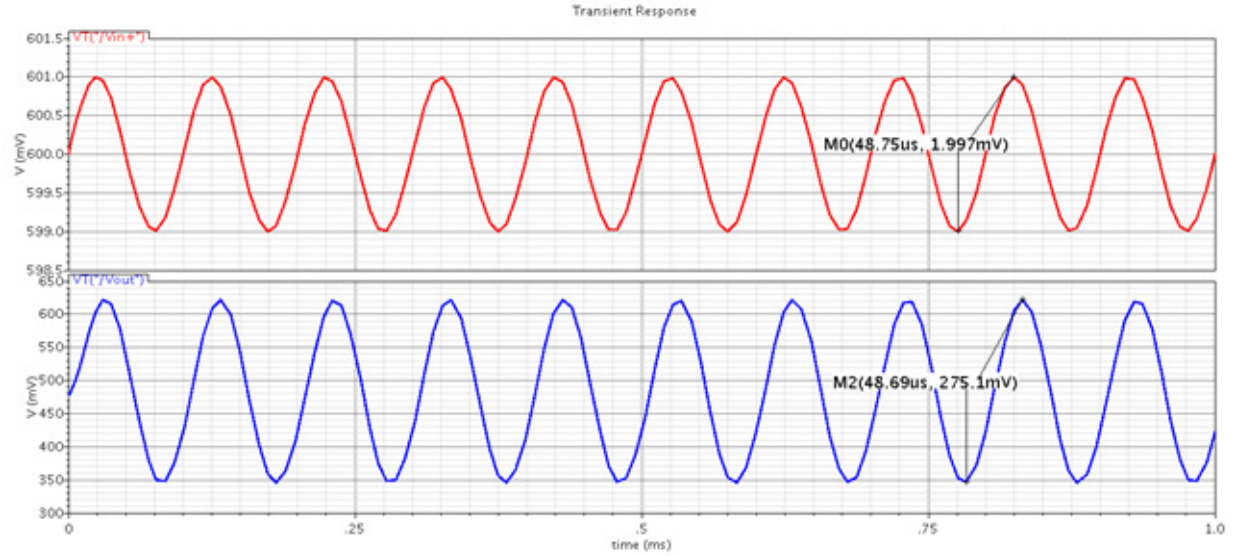

Figure 5. Transient analysis of the differential input stage.

1V supply voltage. Plot shows that unity gain bandwidth (UGB) is 3.3 MHz while phase margin is 87.8°.

Transient analysis is performed on the circuit by applying sinusoidal signal of 10 KHz with 2 mV peak-to-peak amplitude to non-inverting input of the amplifier. Simulation result is depicted in the Figure 5, which indicates, output signal amplitude is amplified to 275 mV peak-to-peak. Average power dissipation of the amplifier is 36.36 µW.

Differential and common-mode AC magnitudes of the amplifier are plotted in the same simulation window to measure Common-Mode Rejection Ratio (CMRR)

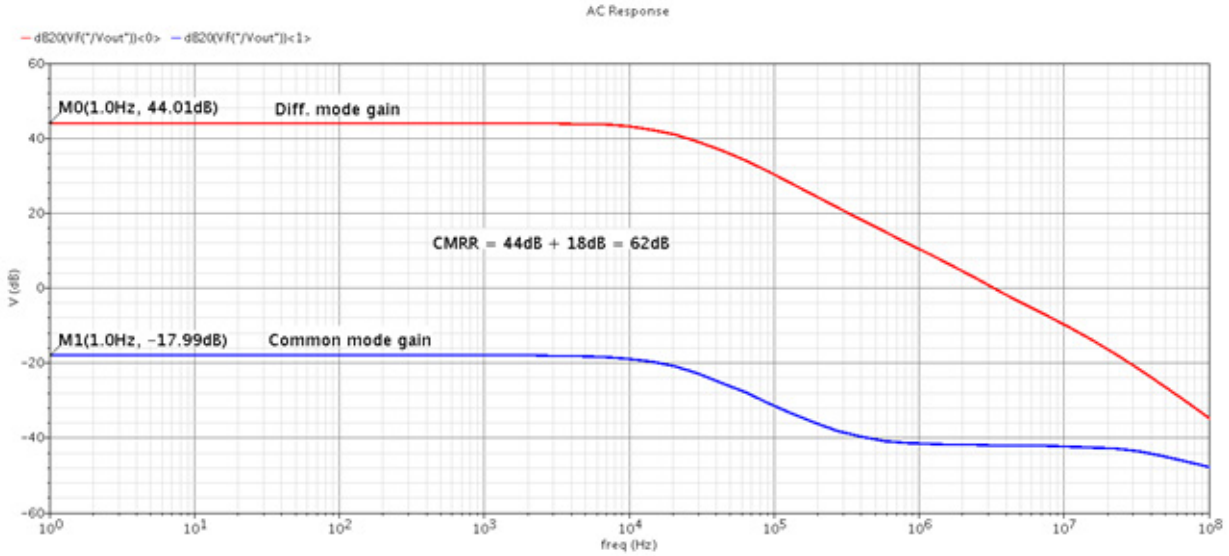

Figure 6. CMRR measurement of the amplifier.

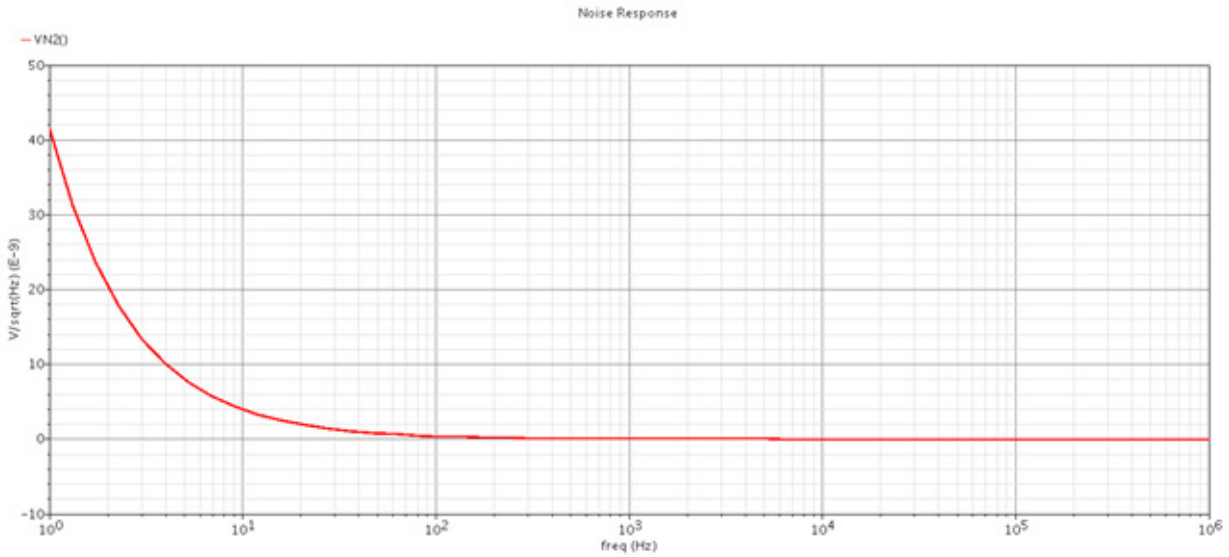

Figure 7. Input referred noise of the amplifier.

of the amplifier. These plots are presented in Figure 6. It shows differential-mode magnitude is 44.01 dB whereas common-mode magnitude is -17.99 dB. Thus the simulated CMRR is 62 dB.

Input referred noise voltage of the amplifier with respect to input signal frequency is shown in Figure 7. It can be inferred from the result that at lower frequency noise floor is higher as it is mainly dominated by 1/f noise. The input referred spot noise voltage at 1 KHz is 42.46nV/sqrt(Hz) and at 1 MHz is 13.82nV/sqrt(Hz) exhibiting very low noise performance.

4.2 Unity Gain Configuration Results

Positive and negative slew rate is measured by configuring differential amplifier as a unity gain buffer. Rail to rail (0

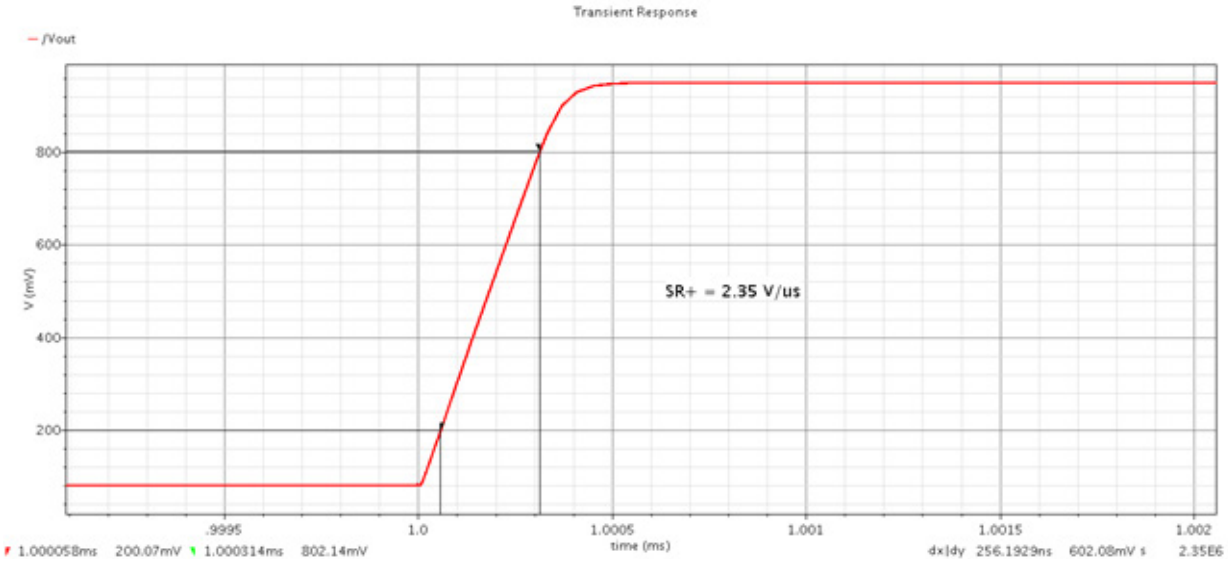

Figure 8. Positive slew rate measurement.

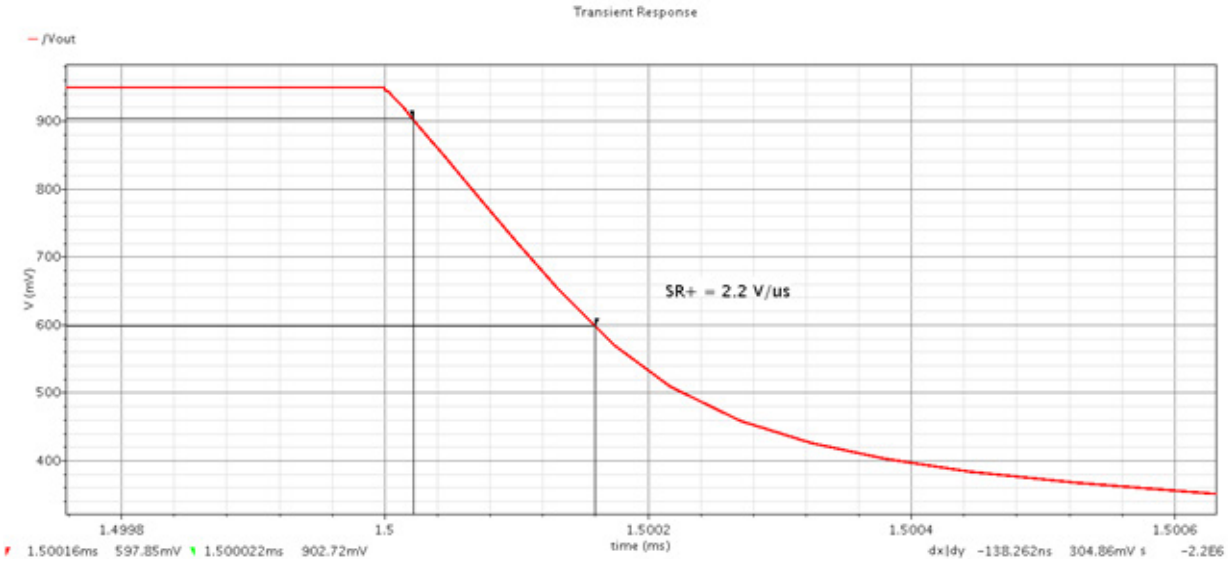

Figure 9. Negative slew rate measurement.

Table 2. Differential input stage performance comparison

Parameter	(3)	This work
Supply voltage (V)	1	1
Process (nm)	350	180
DC gain (dB)	56. 3	44
Unity gain bandwidth (MHz)	0.8	3.3
Phase margin (°)	87.7	87.8
CMRR (dB)	N.A.	62
Power dissipation (μW)	77	36.36
Input referred noise (f = 1 KHz) nV/sqrt(Hz)	436.8	42.46
Input referred noise (f = 1 MHz) nV/sqrt(Hz)	94.6	13.82
Slew rate + (V/μs)	1	2.35
Slew rate - (V/μs)	0.8	2.2

to 1V) square wave signal is applied to the non-inverting terminal of the amplifier to measure slew rate. As shown in Figure 8 and Figure 9, positive slew rate is 2.35 V/μs whereas negative slew rate is 2.2 V/μs.

Table 2 depicts the performance comparison of this work with prior work[3], in which bulk-driven technique is employed in differential pair. Bulk-driven input stage with no partial positive feedback design presented in[3] is considered for comparison.

5. Conclusion

A 1V differential input stage with bulk-driven current mirror as a load is presented, suitable for low voltage analog and mixed-signal portable appliances. Circuit is designed using 180 nm CMOS technology and simulated using BSIM 3v3 Spectre models. Bulk-driven PMOS transistors are used in current mirror to remove the extra threshold voltage requirement from the supply voltage.

The amplifier exhibits DC gain of 44 dB with gain bandwidth product of 3.3 MHz and phase margin of 87.8°. Amplifier consumes very less power and works properly at a supply voltage of 1V making this differential amplifier very useful as an input stage of any Op Amp or OTA.

6. References

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