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Driver circuit implementation for source in optical communication-a review

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Abstract
There are many techniques in designing the driver circuit for the sources such as laser and LEDs in optical fiber communication. However, in this paper, we discuss different types of driver circuits with the help of MESFETs, HFETs, BJTs, HBTs and CMOS technologies.

Keywords: Driver circuit, MESFETs, HFETs, BJTs, HBTs, CMOS.

Introduction
In the following we examine some representative transistor-level laser and modulator-driver circuits that have been reported in the literature. These circuits illustrate how the design principles can be implemented in a broad variety of technologies using different types of transistors such as the metal-semiconductor field-effect transistor (MESFET), the heterostructure field effect transistor (HFET), the bipolar junction transistor (BJT), the heterojunction bipolar transistor (HBT), and the complementary metal-oxide-semi conductor transistors (CMOS)

MESFET and HFET technology
Open drain modulator driver shows the schematic of the GaAs-FET output stage reported in Suzuki (1992) (Fig.1). This stage is part of a 10-Gb/s EAM driver and is implemented in a 0.35 pm GaAs-PHFET technology. The transistors in this circuit are depletion-mode FETs, which means that they conduct current when the gate-source voltage is zero. The output stage consists of an FET current-steering circuit MI and Mi which dumps the tail current from M2 either into the positive power supply (no dummy load is used) or into the EAM load. The driver has an open drain output (no back termination) and connects to the EAM load either directly as shown in the figure or through a transmission line.

The external load consists of a single-ended EAM with a 50Ω resistor, Rp in parallel. In Fig. 1 all subsequent driver schematics we make a distinction between the on-chip supply, VDD and the off-chip supply, VhD, to which external components, such as the load, connects. This distinction clarifies the flow of on-chip and off-chip supply currents. The output voltage swing of the modulator driver can be adjusted with the voltage VSCw, which controls the tail current from M2. The output bias voltage of the modulator driver as shown is zero, but it can be made non-zero by injecting a DC current into the EAM load. The FETs MJ and Mi in the output stage have a channel width of 400 μm and present a considerable input capacitance. Thus a two-stage pre-driver is used to drive this output stage. Each predriver stage consists of a current-steering circuit followed by a source-follower pair (only the source-follower pair of the second stage M3 & M3' is shown in Fig. 1).

The chip further includes an input buffer with an on-chip 50Ω termination. In a similar open-drain output stage has been reported, which is part of a 10 Gb/s EAM driver implemented in a 0.2 μm GaAs-PHFET technology (Miyashita *et al.*, 1997). In contrast to Fig. 1 this implementation brings both drain outputs off chip. When driving a single-ended EAM load, an extemal dummy resistor must be connected to the unused drain.

Modulator/laser driver with back termination

Fig. 2 shows a simplified schematic of the GaAs-FET output stage reported in (Lao *et al.,* 1998). This stage is part of a 40 Gb/s EAM driver and is implemented in a 0.2 μm GaAs-HFET technology with enhancement and depletion mode devices. The driver is connected to the EAR4 load through a 50Ω transmission line. To avoid double reflections on the transmission line, both sides are terminated. The termination on the modulator side is provided by the external 50Ωresistor Rp and the termination on the driver side, the back termination, is implemented with the on-chip resistor R;. The value of R1' is chosen to be 100Ω, rather than 50Ω, to reduce the power dissipation while still achieving an effective back termination. To balance the output stage and to keep the on-chip supply voltage, VDD, quiet, the dummy load in the left branch of the current-steering circuit exactly mirrors the load in the right branch, that is, it consists of an on-chip 100Ωresistor, R1 and an external 50Ω resistor, RD. The peaking inductors, L1 and L1', improve the rise and fall times of the output signal. This output stage is preceded by a predriver, which consists of a cascade of three source-follower pairs, followed by a current-steering circuit, followed by another cascade of three source-follower pairs (only the last pair, M3 and Mi, is shown in Fig. 2). Both cascades of source followers include R-C high-pass coupling networks to speed up the signal transitions, similar to the MA stage shown in Fig. 2. Two on-chip resistors connecting to the output nodes (not shown in Fig. 2) can be used to introduce a bias voltage across the modulator. The driver chip in also contains a retiming flip-flop, which operates from a half-rate clock

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(20 GHz) (Lao *et al.,* 1998). The modulator driver circuit in Fig. 2 also is capable of driving a single-drive or dual-drive MZM. In the latter case the external dummy resistor RD is removed and each output is used to drive one port of the MZM. The same circuit also can act as a laser driver if a bias current source similar to Q5 in Fig. 5 is added.

Modulator/laser driver with active back termination

Fig. 3 shows a simplified schematic of the GaAs-FET output stage reported in (Ransijn *et al.,* 2001). This stage is part of a 10-Gb/s laser/modulator driver and is implemented in a 0.25 pm GaAs- PHEMT technology.

The modulator driver in Fig. 3 connects to the EAM load through a 50-Ω transmission line. To avoid double reflections on the transmission line, both sides are terminated. The termination on the modulator side is provided by the external 50-Ω resistor Rp, whereas the back termination is implemented with an active circuit. As usual, the driver generates the output signal with a current-steering circuit M1 and Mi. An on-chip dummy resistor RD is included at the drain of MI. A scaled-down replica (IS) of the output stage, M2 and Mi, generates a copy of the intended output voltage (without reflections). The source followers M3 and Mi buffer the replica signal and are sized such that their output impedance (x l/gm3) matches the transmission line impedance. The output impedance of the source follower Mi acts as the back termination and absorbs possible reflections. The current 13 through Mi is kept at the constant value ZO by means of a feedback circuit implemented with an op amp (not shown) that controls the voltage V_C. The power dissipated in this active back termination circuit is P = (VDD-Vss). (I_0 + I M/8), where 10 is the bias current for Mi (e.g., l0mA) and 1~/i8s th e current in the scaled down replica (e.g., 12.5 mA). For comparison, a passive back termination with a resistor equal to the load resistor dissipates the much larger power P = (VDD-Vss). I M, where I M is the modulation current (e.g., 100 mA) and no bias current has been assumed.

The driver IC described in Ransijn *et al.* (2001) also includes on-chip terminated input buffers for the data and clock signals, a retiming flip-flop, and a pulse-width control circuit. The chip can be configured as a modulator driver driving a 50Ω load or as a laser driver driving a 25-52 load. In the latter case, two output stages are connected in parallel. The chip also provides a programmable DC current, which can be injected into the laser or modulator load to add a bias. Note that the feedback circuit that keeps 13 equal to I0 also prevents such a bias current from entering the active back termination (M'3).

BJT AND HBT technology

Open collector laser driver

Fig. 4 shows a simplified schematic of the bipolar output stage reported in (Rein *et al.,* 1988). This stage is part of a 2.3-Gb/s laser driver and is implemented in an 8-GHz Si-BJT technology. The output stage consists of a bipolar current-steering circuit, QI and Q;, with both collector outputs coming off chip. One output is terminated with an external dummy resistor, RD and the other drives the laser load through a 25Ω transmission line. The 20Ωseries resistor, Rs, matches the laser impedance of about 552 to the transmission line. Even in applications without a transmission line, a small series resistor Rs is desirable because it dampens the ringing and jitter caused by parasitic inductances (e.g., due to bond wires) in conjunction with laser and driver capacitances.

The modulation current, IM, is supplied by the tail-current source consisting of Q2 and an emitter degeneration resistor. The magnitude of the modulation current can be controlled with the voltage VMC. Similarly, the laser bias current ZB is supplied by the current source consisting of Q4 and its emitter degeneration resistor; the magnitude of IB can be controlled with the voltage VBC. Note that the modulation and bias currents are provided through two separate terminals (pins). In this way, the bias current can be injected after the series resistor Rs avoiding an unnecessary voltage drop across this resistor and averting a potential headroom problem. This output stage is driven by a cascade of two emitter-follower pairs (only the last pair, Q3 and Q! is shown in Fig. 4). The emitter followers present a low output impedance to the output stage and provide level shifting to increase the collector-emitter voltage of Q1 and Q;, thus boosting their maximum fr. In Runge *et al.* (1992) a similar open-collector output stage has been reported which is part of a IO-Gb/s laser driver implemented in a 55-GHz GaAs-HBT technology. In contrast to Fig. 4, a cascoded current-steering circuit is used and the laser is connected directly to the driver output, avoiding the transmission line and the series resistor Rs. This direct laser connection permits the driver to run from a lower supply voltage, thus reducing the power dissipation. The chip in (Runge *et al.,* 1992) also contains an on-chip terminated input buffer and a predriver based on the Cherry-Hooper stage. Laser/modulator driver with back termination. Fig. 5 shows a simplified schematic of the bipolar output stage reported in (Rein *et al.,* 1994). This stage is part of a 10-Gb/s laser/modulator driver and is implemented in a 25-GHz Si-BJT technology.

For this driver, the characteristic impedance of the transmission line (the load) is chosen to be 50Ω, which permits it to operate as a laser or modulator driver. When used as a laser driver, as shown in Fig. 5, a series resistor, Rs x 45 Q, matches the laser to the transmission line. To avoid double reflections on the transmission line the driver incorporates the back termination resistors R1 and R1;. Ideally these resistors should match the 50Ω transmission line; however, as a compromise between matching quality and power dissipation, they were increased to 100Ω. Note that these resistors add to the power dissipation by absorbing not only a good part of the modulation current from Q2, but also some of the bias

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current from Q5. The emitter degeneration resistors R2 and R$ are distributed among the emitter fingers to ensure an even current distribution within the transistors Q 1 and Q. The peaking inductors, L1 and L;, improve the rise and fall times of the output signal and are realized with over length bond wires. For versatility, for symmetry of the output stage, and to keep the on-chip supplies VCCa nd VCCq~u iet, both outputs are brought off chip: when operating as a laser or EAM driver, one output is terminated with an external dummy resistor, RD;w hen driving a dual-drive MZM, both outputs are used. In Fig. 5, the laser bias current from Qs is applied to the laser cathode through an FWC to minimize the capacitive loading of this high-speed node.

The input buffer and predriver for the output stage consists of a cascade of three emitter-follower pairs followed by a current-steering circuit followed by another three emitter-follower pairs (only the last pair, Q3 and Q with current sources Q4 and Q;, is shown in Fig. 5). To obtain a clean eye diagram over a wide range of modulation currents the tail current of the pre-driver's current-steering circuit as well as the bias currents of several emitter followers are varied with the modulation current. Each bias current has a component that varies proportional to the modulation current (e.g., the currents provided by Q4 & Q4') as well as a component that is constant (not shown in Fig. 5). The input buffer and predriver of this chip also include means to control the pulse-width distortions and to equalize the rise and fall times at the laser/modulator load. The output stage runs from a higher supply voltage (Vcc2 & Vcc2') than the rest of the chip permitting a higher output voltage swing or a higher current into the 50Ω load without increasing the power dissipation of the input buffer and predriver. At the maximum swing, the collector-emitter voltage of Q1 and Q1', exceeds the open-base breakdown voltage of 3.7 V; however, the low output impedance of the pre-driver pushes the breakdown voltage to a higher value, a similar output stage has been reported, which is part of a 4O-Gb/s EAM driver implemented in a 130-GHz InP-HBT technology.

Modulator driver with built-In MUX

Fig. 6 shows a simplified schematic of the bipolar output stage with built-in multiplexer reported in Moller *et al.* (1998). This circuit is part of a 40-50 Gb/s EAM driver and is implemented in a 72 GHz SiGe-BJT technology. The circuit shown in Fig. 6 combines the data-multiplexer and modulator-driver function into a single high-speed stage. Therefore, this circuit also is known as a power MUX. The CML type multiplexer combines two 20 Gb/s data streams into a single 40 Gb/s data stream, which then is used to drive the modulator. A 20 GHz clock signal is needed at the select input of the multiplexer. The power MUX works as follows: the constant current from Q4 (40-50 mA) is steered by a first CML switch, Ql and Q;, to either one of two CML data switches, Q2, Q; or Q3, Q;, depending on the select signal. Then, the selected CML data switch steers the current either into the right or left branch, depending on the input data.

The current from the MUX passes through the cascode transistors Q5 and which prevent breakdown voltage violations and reduce the capacitance at the driver's output. Finally, the MUX current drops over the load R, Q6 or R', Qk, where the driving voltage for the EAM is produced. The inductive load impedance presented by the emitters of Q6 and Qb improves the rise and fall times. The driver chip is directly connected to the EAM with low-inductance wire bonds (no transmission lines). The output voltage swing and output bias voltage can be adjusted with V,Ca nd Vcc-VBC, respectively. The chip in Moller *et al.* (1998) also includes on-chip terminated input buffers and pre-drivers for the two CML data switches, Q2, Q; and Q3, Q. Each buffed pre-driver consists of two emitter-follower pairs, followed by a current-steering circuit, followed by another three emitter-follower pairs.

The advantages of the power MUX approach over a conventional full-rate 4O-Gb/s modulator driver are as follows. (i). Phase shifts and jitter in the input data signals are suppressed by the MUX. Note that the MUX has a similar effect as a retiming flip flop. (ii). The rise and fall times of the output signal are improved and can, to some extent, be controlled by the clock signal swing. (iii). The half-rate predriver for the data signals are less critical.

The circuit in Fig. 6 drives the EAM differentially and thus requires a symmetrical modulator. It must be possible to drive both electrodes of the EAM independently (no shared electrode with the CW laser) and they must have small and similar capacitances to ground. The advantage of driving the modulator differentially is that only half of the voltage swing is required at each output. For eg., a 1-Vpp signal at each output produces a 2-Vpp signal across the EAM. However at the time of writing such modulators do not seem to be commercially available, a similar output stage has been reported which is part of a 40 Gb/s EAM driver implemented in the same 72 GHz SiGe-BJT technology. In contrast to Fig. 6 this driver operates at the full rate of 40 Gb/s and thus has no built in multiplexer.

Modulator driver with distributed output stage

Fig. 7 shows a simplified schematic of the distributed output stage reported in (Thomas *et al.,* 1996). This stage is part of a 10 Gb/s MZ modulator driver and is implemented in a 50 GHz GaAs- HBT technology.

An important speed limitation of the current-steering circuit, especially when used as part of a high-swing MZM driver is the time constant formed by the parasitic output capacitance of the large transistors and load resistor. To circumvent this limitation the large output capacitance can be distributed into an artificial transmission line. This is done by splitting the current-steering transistor pair into n smaller pairs (first pair: Ql & Q1') and connecting them with inductors as shown in Fig. 7. With the appropriate value for the inductors L a pair of artificial transmission

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Fig. 1. MESFET/HFET implementation of an EAM-driver output stage based on (Suzuki, 1992).

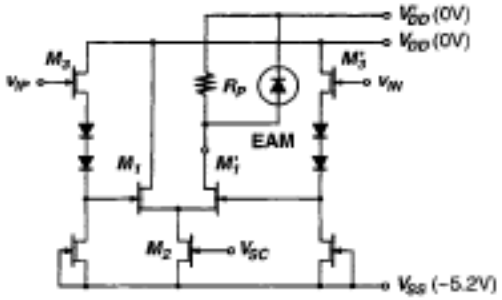

Fig. 2. MESFET/HFET implementation of an EAM-driver output stage with back termination based on (Lao et al., 1998).

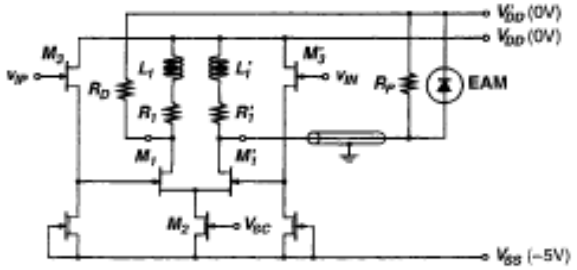

Fig. 3. MESFEWHFET implementation of an EAM-driver output stage with active back termination based on (Ransijn et al., 2001).

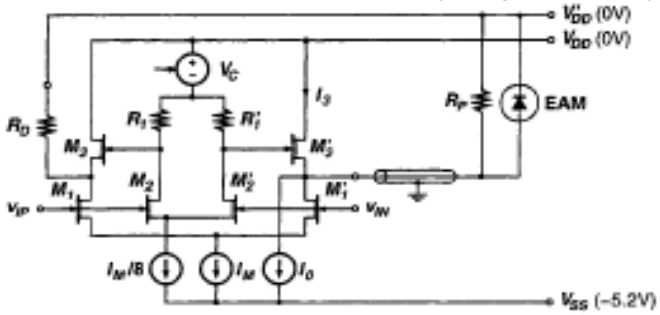

Fig. 4. BJT/HBT implementation of a laser-driver output stage based on (Rein et al., 1988).

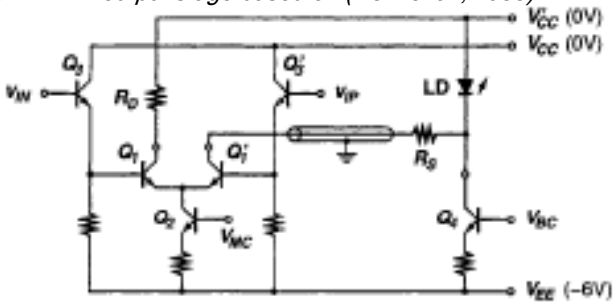

Fig. 5. BJT/HBT implementation of a laser-driver output stage with back termination based on (Runge et al., 1992).

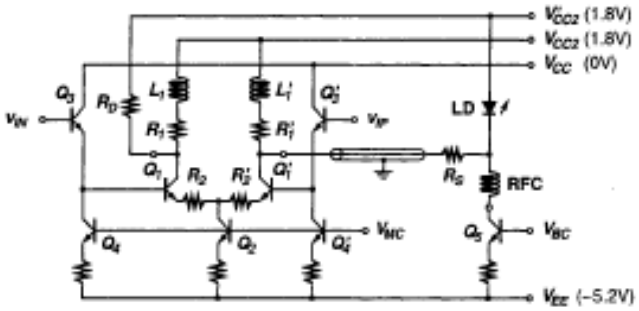

Fig. 6. BJT/HBT implementation of a differential 40 Gb/s EAM-driver output stage with built-in MUX based on (Moller et al., 1998).

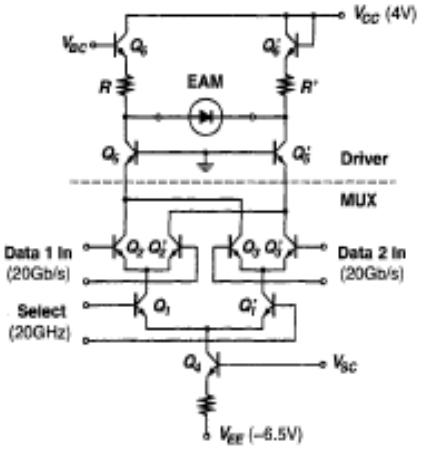

Fig. 7. BJT/ HBT Implementation of distributed MZM driver output.

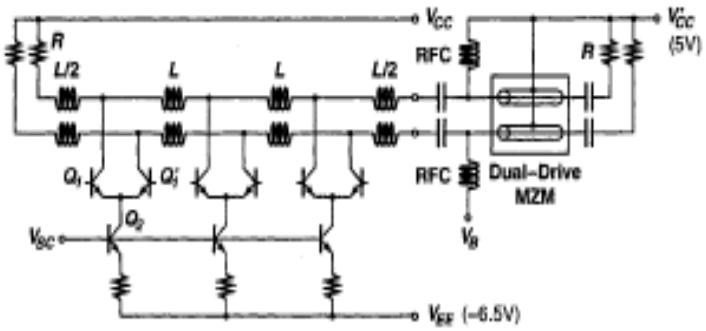

Fig. 8. CMOS implementation of a predriver based on (Galal et al., 2003).

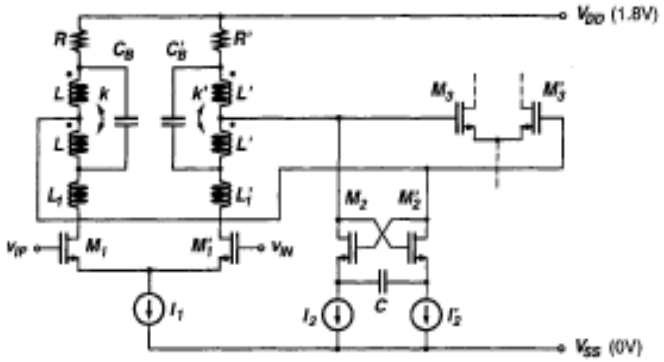

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Fig. 9. CMOS implementation of a low-power burst-mode laser driver based on (Eduard et al., 2000).

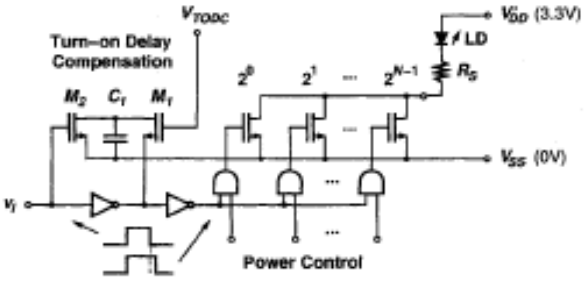
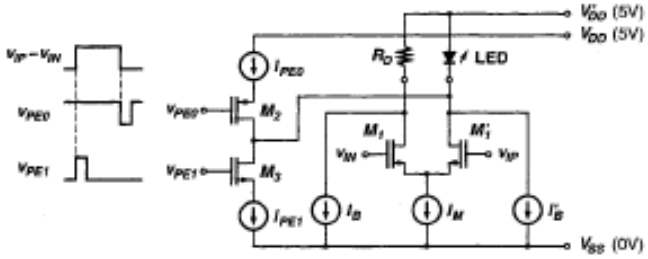


Fig. 10. CMOS implementation of an LED-driver output stage with preemphasis based on (Shieh et al., 2000).



lines matched to the termination resistors R and the impedance of the MZM are formed. Now, the speed is limited by the cutoff frequency of the artificial transmission lines, which can be made high by choosing a large number of sections, n. A second pair of artificial transmission lines (not shown in Fig. 7) provides the differential input signals to the n sections of the distributed output stage.

In Thomas *et al.* (1996) the number of sections was chosen to be five (n = 5). Each section consists of a current-steering circuit (first section: QI and Q) driven by a pair of emitter followers (not shown in Fig. 7). The emitter followers lower the input capacitance to the same level as the output capacitance, permitting the use of the same inductor value for the input and output transmission lines. Furthermore, the emitter followers lower the input conductance and thus reduce the loss of the input transmission lines. The distributed output stage is driven by a lumped pre-driver with two stages. Each predriver stage consists of an emitter-follower pair followed by a current-steering circuit. A further advantage of the distributed output stage is its superior output matching (S22) at high frequencies, which helps to avoid double reflections on the transmission lines to the MZM.

The driver can be AC coupled to a dual-drive MZM as shown on the right-hand side of Fig. 7. Because of the push-pull configuration, a voltage swing of only one half of the switching voltage, V, is needed per output. The output swing can be adjusted with the voltage Vsc, which controls the tail currents (first section: Q2) of the output stage as well as the currents in the predriver. The bias voltage VB is supplied to the MZ modulator through a bias T (RFC with coupling capacitor). The low-frequency pilot tone needed for the ABC can be superimposed on Vsc.

CMOS technology

Predriver: Fig. 8 shows a simplified schematic of the CMOS predriver reported in (Galal *et al.*, 2003). This stage is part of a 10-Gb/s laser/modulator driver and is implemented in a 0.18 pm CMOS technology. The pre-driver consists of a current-steering circuit, Mi and Mi, which is loaded by a combination of the resistors R and R', the T-coil networks L, CBa nd L', Cg and the series inductors L1 and L {. The MOSFETs M2 and Mi form a negative impedance converter (NIC), which inverts the capacitance C and thus present the predriver with a negative load capacitance equal to about C. This negative capacitance compensates about 30% of the output stage's large input capacitance (from M3 & M). The remaining capacitance is driven with the help of the T-coil networks which provide a significant bandwidth boost (cf. Section 6.3.2). The T-coil networks are realized with on-chip coupled inductors. The inductors L1 and L; provide series peaking, which further increases the bandwidth. In Galal *et al.* (2003) this predriver is followed by a current-steering output stage M3 and Mi with passive 754 back terminations. The predriver and the output stage form one of three identical 'driver slices' that constitute the reconfigurable laser/modulator driver chip. When configured as a laser driver, all three slices are enabled and operate in parallel; when configured as a modulator driver, only a single slice is enabled. Burst-mode laser driver. Fig. 9 shows a simplified schematic of the CMOS low-power laser driver reported in (Eduard *et al.*, 2000). This circuit is part of a 155 Mb/s burst-mode laser driver for PON applications and is implemented in a 0.5 pm CMOS technology.

In contrast to the drivers discussed so far, this driver uses current switching instead of current steering. This means that during the transmission of a zero, the modulation current is shut off rather than steered into a dummy load. As a result, the average power dissipation is reduced by a factor two. This scheme is particularly suitable for burst-mode laser drivers because it automatically powers down the output stage during idle periods, that is, when no bursts are transmitted. For eg., if the average burst activity is l0%, the total power savings are 20x. Furthermore, the driver in Fig. 9 operates with zero laser bias current. This mode of operation ensures the high inter burst extinction ratio required for burst-mode drivers and saves additional power. As we know, operating a laser without bias current results in a turn-on delay and turn-on delay jitter. The turn-on delay can be compensated by pre distorting the pulse width of the input data signal. The simple turn-on delay compensation circuit shown in Fig. 9 delays the falling data edge by an amount equal to the laser's turn-on delay. On the falling edge of VI, the output of the first inverter is loaded by C1 (through MI), causing a delay of this edge. The amount of delay can be controlled with the gate voltage of MI, VTODC. On the rising edge of UI, M2 discharges C1 rapidly preventing a similar delay of the latter edge.

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Unfortunately, the turn-on delay jitter cannot be compensated in a similar manner because of its random nature. But in low-speed applications up to about 155 Mb/s, it is unlikely to cause problems.

The laser driver in Eduard *et al.* (2000) also features a p-MOS shunt transistor across the laser diode (not shown in Fig. 9) to suppress an optical tail at the end of the burst. A digital APC circuit controls the output power by selectively enabling some of the N parallel current-switching transistors shown in Fig.9. Because these transistors have widths proportional to 2n with n = 0….N-1, they form a built-in binary D/A converter. The N-bit word is generated with an up down counter controlled by an integrate-and-dump circuit. The chip further includes an end-of-life detector with selectable threshold. LED driver (Fig. 10) shows a simplified schematic of the CMOS LED-driver output stage with preemphasis reported in (Shieh *et al.,* 2000). This stage is part of a 125 Mb/s ethernet transmitter (1OOBase-FX) and is implemented in a 0.5 pm CMOS technology. The current source IM supplies the modulation current of typically 70 mA. This current source has a built-in positive temperature coefficient to compensate for the negative temperature dependence of the light-emitting diode's (LED'S) slope efficiency. A current-steering circuit MI and Mi modulates IM and drives the LED.

An external dummy resistor terminates the unused output of the driver. To enhance the speed of the inherently slow LED a small bias current ZL and a pre-emphasis scheme are used. The pre-emphasis works as follows: during the first 2.5 ns of the 84s bit period, an additional current, Ip~lis, forced into the LED by means of switch M3 to improve the optical rise time. Similarly, at the end of the bit period, M2 turns on to discharge the LED with IpEO, thus improving the optical fall time. The LED driver in Shieh *et al.* (2000) is part of a large mixed-signal chip for Ethernet fiber (100 Base-FX) to twisted-pair (100 Base-TX) media conversion. It also includes the main amplifier and clock and data recovery circuit for the optical receiver.

Conclusions

- The output voltage range (or compliance voltage) for laser drivers. The low end of this range should be as low as possible to permit DC coupling of the laser while maintaining a low supply voltage.
- The modulation and bias voltage ranges for modulator drivers, which must be large enough to operate the desired modulator under worst-case conditions. In particular, high-speed Mach-Zehnder (MZ) modulators require a large modulation voltage (or voltage swing).
- The power dissipation, which should be as low as possible to save power and limit undesirable heat generation.
- The rise and fall times, which must be short compared with the bit period.
- However, the rise time of laser drivers should not be too short to limit the generation of optical chirp.
- The pulse-width distortion, which usually is compensated with an adjustable pulse-width control circuit.

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