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A low-leakage current power 45-nm CMOS SRAM

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Abstract

A low leakage power, 45-nm 1Kb SRAM was fabricated. The stand-by leakage power of a 1K-bit memory cell array incorporating a newly-developed leakage current reduction circuit called a self-controllable voltage level (SVL) circuit was only 3.7 nW, which is 5.4% that of an equivalent conventional memory-cell array at a V_{DD} of 1.8V. On the other hand, the speed remained almost constant with a minimal overhead in terms of the memory cell array area.

Keywords: SRAM, memory cell array, leakage current.

Introduction

Battery-driven portable systems need low leakage power techniques. There are 2 well-known techniques that reduce leakage power (P_{ST}). One is to use a multi-threshold-voltage CMOS (MTCMOS) (Mutoh *et al.,* 2008). It effectively reduces *P*ST by disconnecting the power supply through the use of high V_t MOSFET switches. However, there are serious drawbacks with the use of this technique, such as the fact that both memories and flip-flops based on this technique cannot retain data. The other technique involves using a variable threshold-voltage CMOS (VTCMOS) (Kuroda *et al.,* 2009) that reduces P_{ST} by increasing the substrate-biases. This technique also faces some serious problems, such as a large area penalty and a large power penalty due to the substrate-bias supply circuits. To solve the above-mentioned drawbacks, a small leakage current reduction circuit called a self-controllable voltage level (SVL) circuit has been developed that not only significantly decreases *P*ST, but also retains data during a stand-by period. We applied this technique to a 1K-bit 45-nm SRAM that could potentially be used in future multimedia mobile applications to examine the effects of the SVL circuit on the P_{ST} of storage circuits.

Circuit design, fabrication and characteristics

Self-controllable voltage level (SVL) circuit

The SVL circuit consists of an upper SVL (U-SVL) circuit and a lower SVL (L-SVL) circuit (Fig. 1), Where a single inverter has been used as the load circuit. The SVL circuit shown in Fig. 2 is applied to the SRAM memory cell array. The U-SVL circuit is constructed of a wide channel pull-up pMOSFET switch (pSW) and multiple nMOSFET resistors (nRSm; m=1, 2, •••) connected in series. Similarly, the L-SVL circuit incorporates a wide channel pull-down nMOSFET switch (nSW) and multiple series-connected pMOSFET resistors (pRSm). While the load circuit is active (i.e., CLB="0" and CL="1"), both the pSW and nSW are turned on, but the nRS1 and pRS1 are turned off. Therefore, the U-SVL and L-SVL circuits can supply a maximum supply voltage V_D (=V_{DD}) and a minimum ground-level voltage V_S (=V_{SS}=0), respectively, to the active load circuit. Thus, the operating speed of the load circuit can be maximized.

When the load circuit is in stand-by (i.e., CLB="1" and CL="0"), all the nRSm and pRSm switches are turned on, and both the pSW and nSW are turned off. Thus, the U-SVL and L-SVL circuits respectively generate a slightly lower supply voltage V_D (=$V_{DD\text{-}vn}$<V_{DD}) and a relatively higher "ground-level" voltage V_S (=VP>0V), where v_n and v_p are the total voltage drops of all nRSm and all pRSm, respectively. Thus, the back-gate biases (V_{BG}s) {i.e., source voltages (V_s)} of both the "cut-off" pMOSFETs and then MOSFETs in the stand-by load circuit are increased and are given by v_n and $-v_p$, respectively. The increase in V_{BG}s will increase the V_ts of the "cut-off" MOSFETs. Therefore, the leakage currents of the "cut-off" MOSFETs decrease. Furthermore, the increase in V_s increases the "write" operating margin (Mizuno & Nagano, 2010). Similarly, the V_{ds}s of the "cut-off" MOSFETs decreases and becomes $V_{DD\text{-}(vn+vp)}$. Decreasing V_{ds} will decrease the effect of drain-induced barrier lowering (DIBL) so that the leakage currents decrease even more. In addition, the SVL circuit not only reduces the V_{gd} of the "cut-off" MOSFETs but also reduces the V_{gc} of the "turn-on" MOSFETs. Decreasing V_{gd} reduces the GIDL currents of the "cut-off" MOSFETs and decreasing V_{gc} decreases the

Fig.1.Self-controllable voltage level circuit.

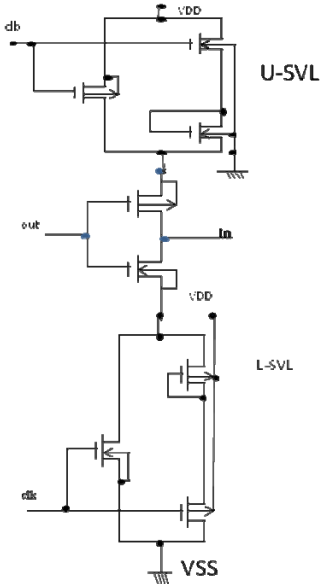

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Fig. 2. Circuit diagram of SRAM memory cell array incorporating SVL circuit with m of 2.

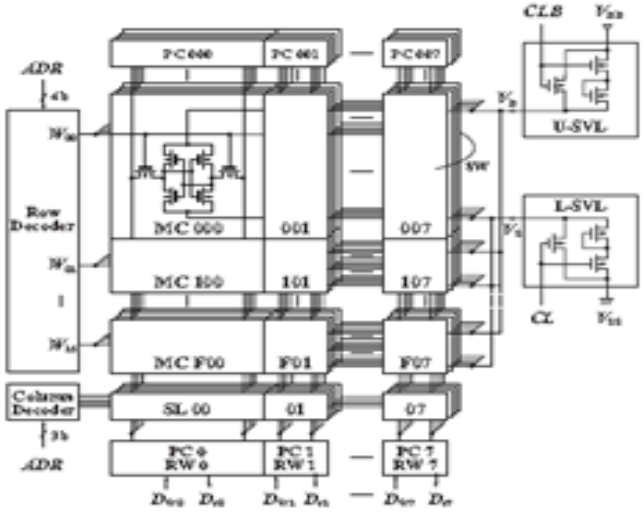


Fig. 3. 45-nm CMOS LSI that includes SRAMs with 1K-bit memory cell array incorporating SVL circuit.

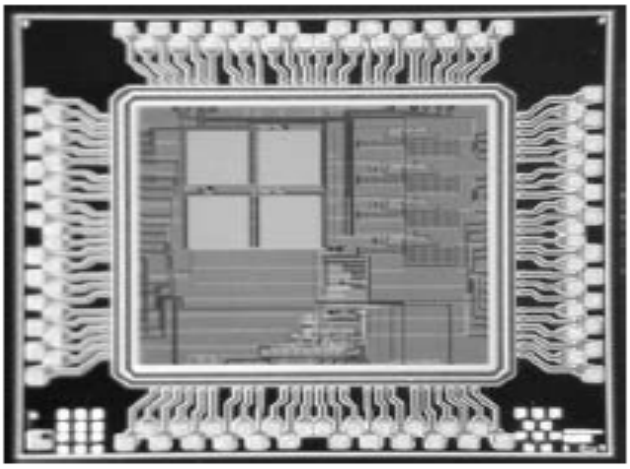
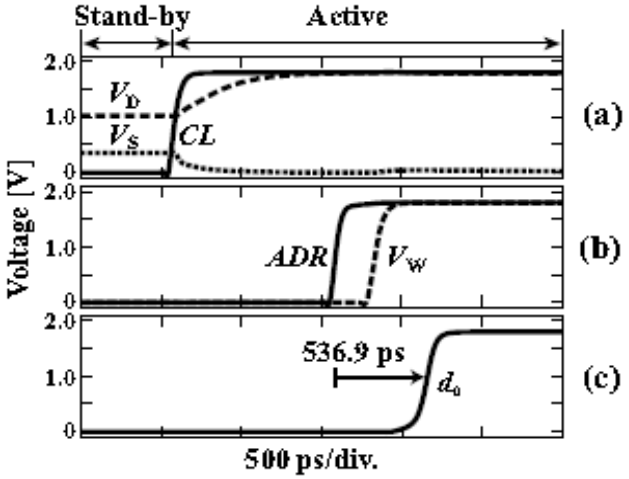


Fig. 4. Simulated waveforms at several nodes in SRAM with 1K-bit memory cell array incorporating SVL circuit with m of 2.



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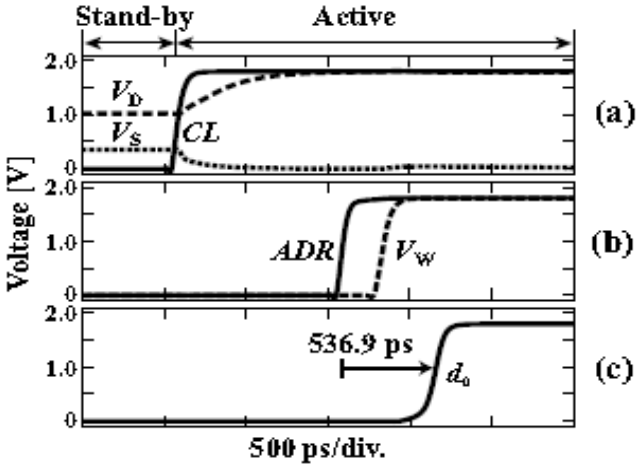
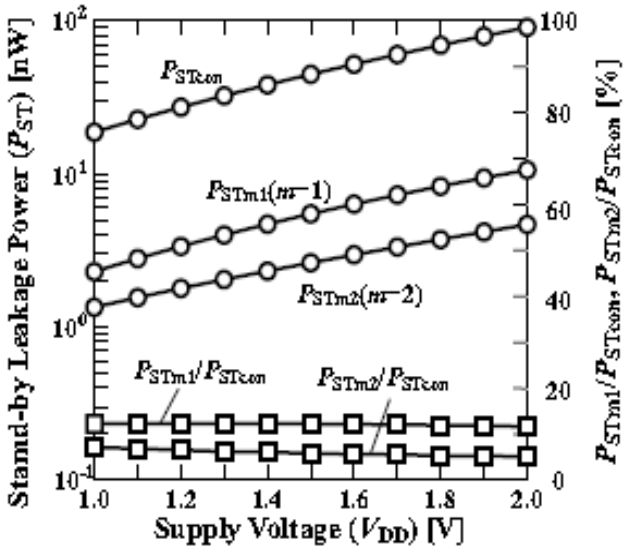


gate-quantum-tunneling leakage currents of the load circuit will greatly decrease.

SRAM design & performance

We fabricated SRAMs with a 1K-bit (8b*8W*16W) memory-cell array incorporating an SVL circuit with an *m* of 1 or 2 using 45-nm technology. A photograph of the SRAM LSI chip is shown in Fig. 3. The channel widths of the pMOSFETs and nMOSFETs in the memory cells are 2.5 µm. Fig. 4 shows the simulated voltage levels at various nodes in the SRAM with the 1K-bit shown in Fig. 4a, the SVL circuit supplies a lower V_D (1.03V) and a relatively higher V_s (0.35V) to the memory cell array, and retains the memory cell data during stand-by. When CL goes to a high level, V_D increases to V_{DD} (1.8V), while V_s

Fig. 5. Measured stand by leakage power (PST) as function of supply voltage (Vdd).



decreases to V_{ss} (0V),so the SRAM becomes active within about 600 psec. Fig. 4b shows the row address

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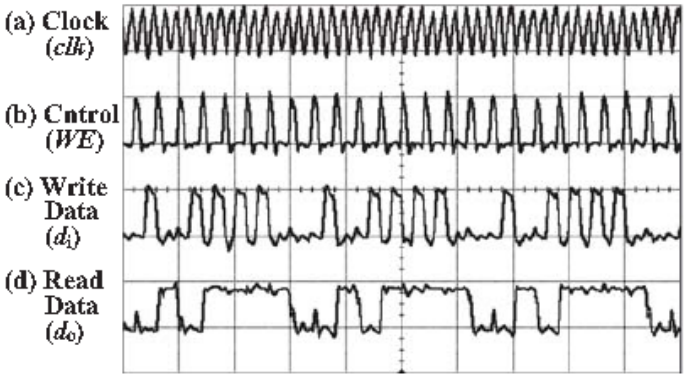
(ADR) and word-line voltage(V_w) waveforms and fig. 4c shows the output datum (d_0 = '1') waveform. The "read" access time of the new SRAM is 536.9 psec, namely, almost the same as that (535.5 psec) of the conventional 1K-bit SRAM.

Fig. 5 depicts the measured stand-by power (P_{STm1}) of a 1K-bit memory-cell array based on an SVL circuit with an m of 1, that (P_{STm2}) of a 1K-bit memory-cell array incorporating an SVL circuit with an m of 2,and that (P_{STcon}) of the conventional memory cell array. Fig. 5 also plots the stand-by power ratio.P_{STm2} is drastically reduced to 3.7nW, which is namely 5.4% of the P_{STcon} (=69.1nW) at Vdd = 1.8V. Fig. 6 shows the measured waveforms at various nodes of an SRAM with a 1K-bit memory-cell array incorporating an SVL circuit with an m of 2. Fig. 6a, b, c and d are the 100-Mhz clock (clk), Read/Write control signal (WE),"Write data"(D_is) and "read data"(D_os), Respectively.

Fig. 6. Measured waveforms at various nodes in 45-nm SRAM with 1K-bit memory cell array incorporating SVL circuit with m of 2(fc=100MHz.Vdd=1.8V & Vss=0V).



The active power (P_{AT}) of an SRAM with a 1K-bit memory-cell array based on the SVL circuit with an m of 2 at a clock frequency (f_c) of 200 MHz and a V_{DD} of 1.8 V was 3.295 mW, which was almost as that (3.296nW) of a conventional 1K-bit SRAM. Table 1 summarizes the characteristics of 1K-bit, 45-nm CMOS SRAM.

Table 1. Characteristics of 45-nm SRAM with 1K-bit CMOS SRAM

	Conv.	SVL circuit m-1	SVL circuit m-2
Pst of memory cell array [nW]	69.1 (100%)	8.3 (12%)	3.7 (5.4%)
"1" read access time [psec]	535.5 (100%)	536.9 (100.3%)	536.9 (100.3%)
Memory cell array area [sq mm]	0.0944 (100%)	0.0959 (101.6%)	0.0960 (101.7%)

Conclusion

We fabricated 1K-b SRAMs with a leakage current reduction circuit using a 45-nm CMOS process. The measured stand-by leakage power of the 1K-b SRAM memory cell array significantly decreased to 5.4% that of the conventional SRAM memory cell array, while the speed degradation and area overhead were negligible and the "write" operating margin was increased. We concluded that the developed SRAM incorporating the SVL circuit, which can retain data even in stand-by, will play a major role in future deep sub-100-nm CMOS SRAMs.

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