Voltage-mode fuzzy logic controller

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Abstract

A voltage-mode fuzzy logic controller on the base of controlling transistor net is introduced in this paper. The inputs and output of total system are digital voltage pulses while inside parts of total circuits are analog voltage mode circuits. Using transistor net in fuzzifier part provides a simple method for implementing a fast and accurate fuzzifying operation. The chip area of resulted controller is 0.22 mm^2 in 0.35um CMOS technology and the inference speed is 14.83 MFLIPS.

Keywords: FLC, Chip designing, fuzzifier, voltage mode, min circuit

1. Introduction

The aim of this paper is designing a two-input one-output fuzzy logic controller in voltage mode using new fuzzifier and new structures for other parts of controller. In this case our inputs and outputs are digital. Digital input and output have important advantage that is high compatibility with other digital systems which is very useful in industrial environment and they provide higher controllability. But digital circuitry especially when a multistage system like fuzzy controller is implemented has various drawbacks such as high circuit complexity, high die area, high power consumption which in analog circuits this drawbacks do not appear (Mohagheghi, S.et al, 2006)(Sanchez-Sinenico, E., et al, 99) (S. Guo, L.et al, 98).

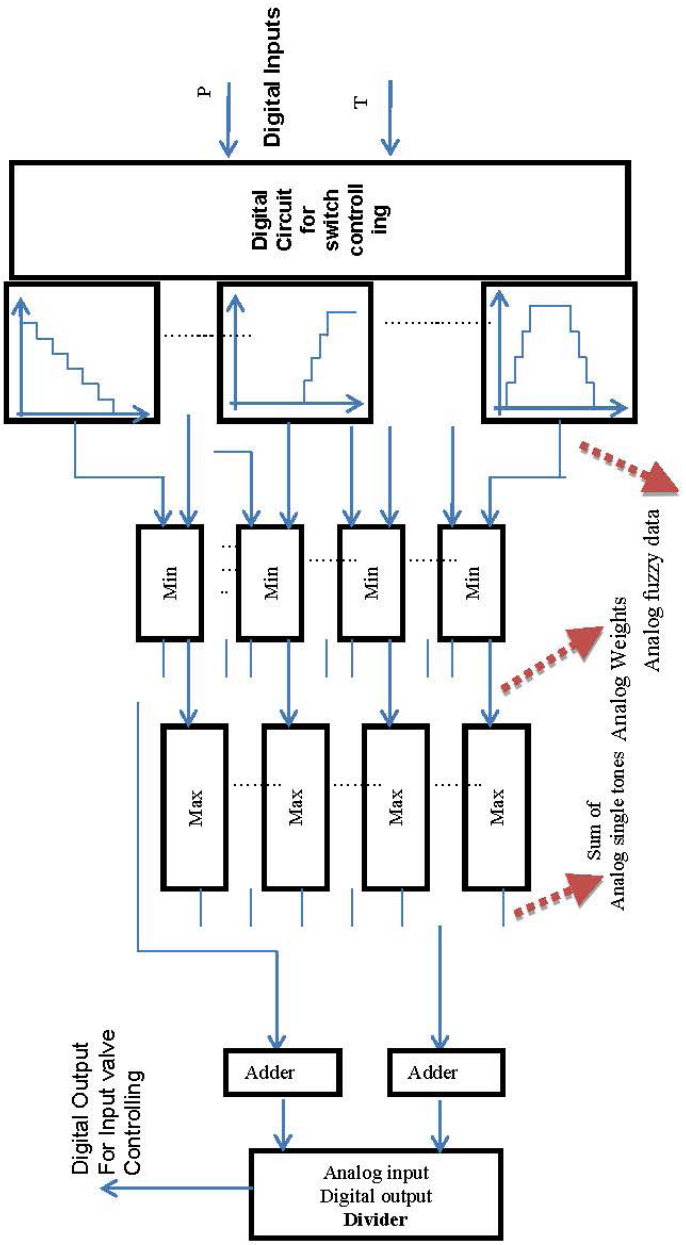
Considering all above circumstances, this work is on a fuzzy logic controller in order to control input valve with digital inputs, digital output and analog internal circuitry. As mentioned above output valve employs simple on-off controller, because of that it works in low and fixed flow and also the number of switching is low.

Sadeq et al. (Sadeq, et al, 2006) did the same work in current mode which its voltage counterpart will be presented here in this paper. This paper uses the same circuits in (Sadeq, 2010, 2011) for defuzzifier part.

In this section, fuzzy functional blocks are described and their performances are discussed. A fuzzy logic controller normally has three stages, fuzzifier, inference engine and defuzzifier. All idea behind of our proposed controller has shown in figure 1.

All input membership functions can take arbitrary shapes. The membership functions are fed into inference block. As shown in figure 1 the main inputs and outputs of all controller system are digital pulses. Two main stages of fuzzy logic controller which involving with outdoor of circuit are fuzzifier and defuzzifier. In order to achieve the idea shown in figure 1, a new fuzzifier with a digital input and analog output, and a new defuzzifier with analog input and digital output has proposed. This proposed circuits allowed us to propose new full analog circuit.

Fig.1. *Proposed Fuzzy Controller Chip*



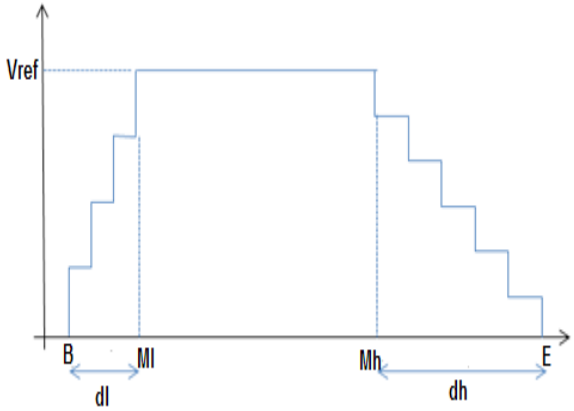
Our designed controller had tested with 2-inputs, one input digital data and another one digital input data. One output as valve movement and 9 rules structure. Figure 1 shows an architectural schematic diagram of fuzzy controller hardware. It consists of three main processor blocks: Fuzzifier block, Inference block and defuzzifier block.

2. Fuzzifier Unit

Fuzzy controllers work based on fuzzy logic. As described in introduction, fuzzy logic provides an ambiguous mapping of the nonlinear systems.

Figure 1 illustrates the different blocks of fuzzifier structure. The proposed desired shape of the membership function in order to obtain the idea proposed for fuzzifier is shown in figure 2. Considering the descriptions mentioned before, and according to the B, MI, Mh, E, parameters,there was a division, which its numerator is reference voltage and its denominator is d1 = M1 - B or d, = E-Mh. The dl and dh parameters enters first to the divider part and considering previous description this action will be done with two separate parts, one for dividing over one to seven and another for eight to fifteen. At last the obtained output of divider circuit enters multiplier circuit, which multiplies the input voltage (base voltage) by one to fifteen, Of course as described before, the multiplication rate depends on the what fraction of reference voltage, Vbase is. For an example, if Vbase = Vref /5, multiplier just does multiplication operation from one to five. Crisp input signal and the chosen parameters for performing favorable membership function, are applied to switch controller block and the output of this block are digital signals which control some switches in both divider and multiplier blocks.

Fig.2. *Proposed membership function*



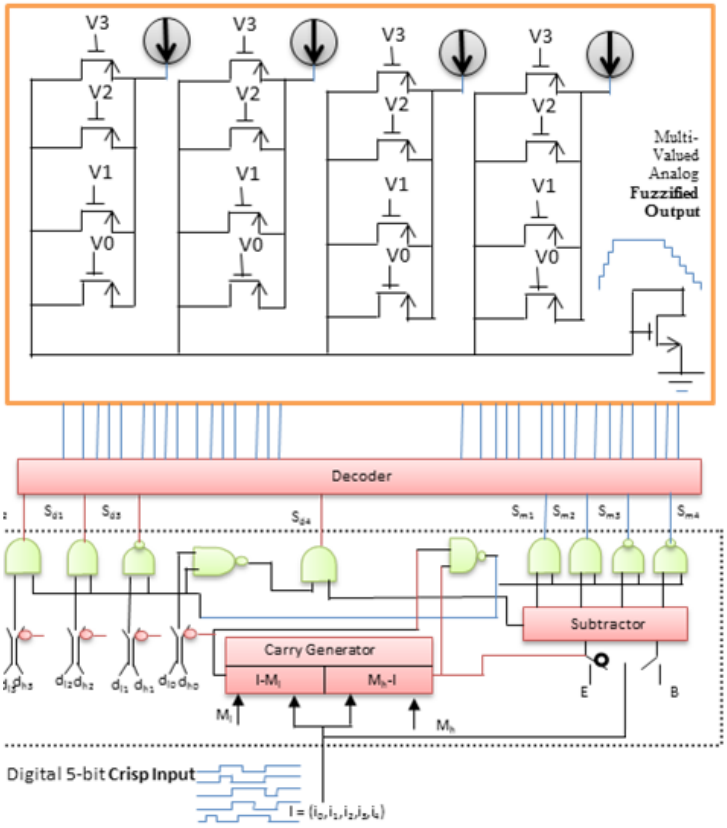
Input parameters are 5-bit numbers (B, Ml,Mh, E, dl, dh) introduced in figure 2. According to these parameters, divider block divides reference voltage over a specific number, the quotient is Ibase. Ibase will be multiplied by ordinal numbers between S and E.

If input signal is smaller than B or greater than E, divider circuit will be disconnected and output voltage will be zero. Figure 3 shows total fuzzifier proposed in this paper which contains two parts one part is transistor- array and switches another part is a digital circuit which controls these switches. The digital input will applied to this block and analog output of fuzzifier will be prepared without using digital to analog converters.

3. Inference Unit

Fuzzy inferences employing minimum function are used in many applications. Minimum block is an important part of a fuzzy controller. We have used minimum circuit in inference engine of designed controller. So we describe a novel two-input minimum circuit.

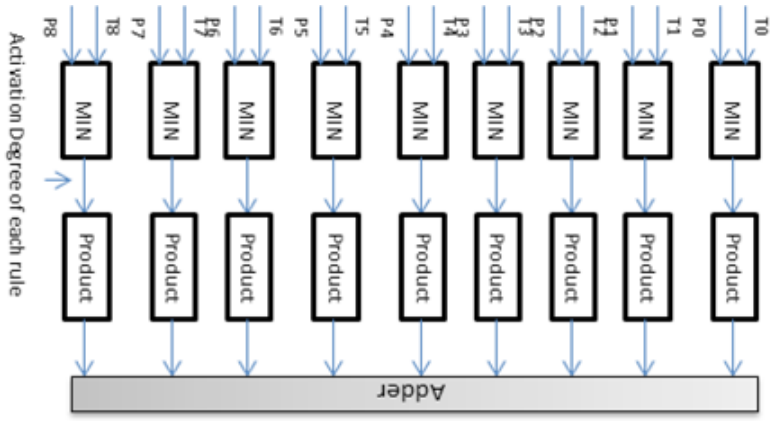
Fig.3. *Proposed circuit for fuzzifier*



The structure of inference engine is shown in figure 4. A new circuit designed at voltage-mode with MOS transistors for the main block of inference engine which is shown in figure 5. Considering that the design is a voltage- mode type, opposite to voltage- mode circuits for implementing adder part is very easy and it will be done with short-connected wiring. Accurate voltage mirrors has used for implementing multiplier.

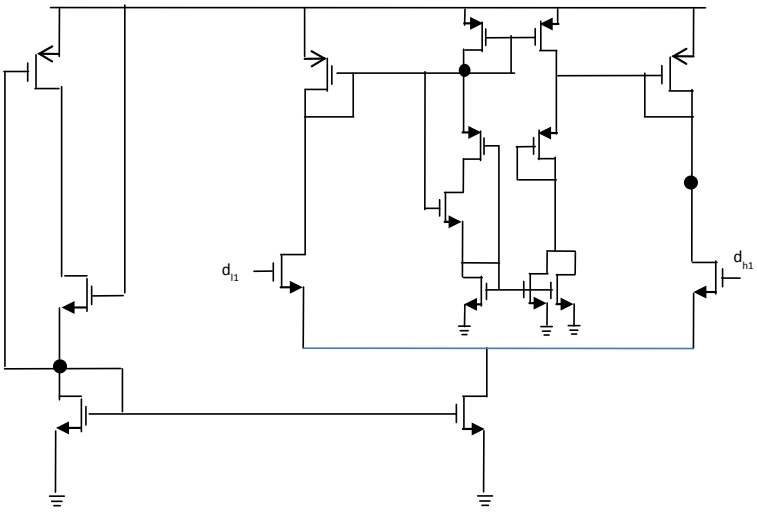
The proposed controller is constructed with trapezoidal membership function generators, Min circuit and a Defuzzifier circuit. In figure 8, NT, MT, PT, NP, MP and PP generators are the same MF generators described in fuzzifier section in previous sections. Also Min block uses the proposed circuit in figure 5. For defuzzifier part we used our proposed hierarchical defuzzifier which is introduced in reference (Sadeq,2010, 2011). S1 to S5 are the singleton values that specify fuzzy rules are
(s1=1, s2=7, s3=16, s4=25, s5=31)

Fig.4. *the inference system of controller*



Remember that for simplicity in hardware design usually output membership functions are considered as singleton form. In other words we use singleton fuzzy computation method. In this method each output membership function is a constant value on output discourse (Jeen-Shing Wang, et al, 2002, Rong-Jong Wai, et al, 2002).

Fig.5. *The proposed Min circuit*

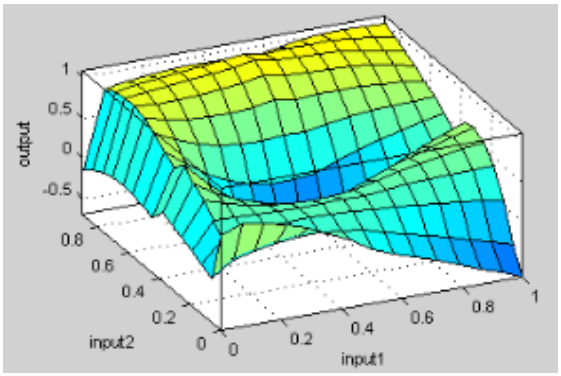


4. Simulations and discussion

The shown surface in figure 6 is a typical output of the multipurpose controller which is proposed in this paper. The aim of this simulation is to compare with HSPICE outputs which are shown in figure 8. Before HSPICE simulation, the systematic model of controller evaluated with MATLAB software. In defined model input membership functions (two T and B inputs in which there are three language terms Negative, Zero, Positive) are assumed to be triangular or trapezoidal. The obtained control-surface graph is shown in Figure 6. T and P represent two input variables in volts.

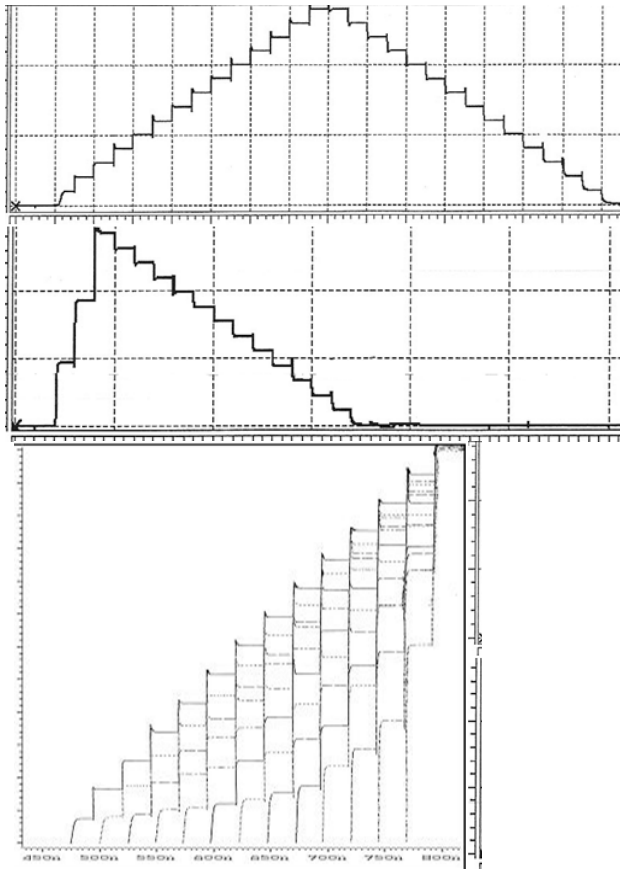
The figure 7 shows 3 different membership functions for both two inputs which are the results of Hspice simulation of fuzzifier circuit.

Fig.6. *Obtained control surface*



Different between the real surfaces and simulated surface, which we call error surface is negligible. It is very difficult to develop an accurate error model for the entirely of the integrated controller data path although possible error sources and their effect on circuit performance are well documented individually for: The error surface is indicative of two dominant systematic error sources. One is the quantization error, which as mentioned previously, is negative due to an error made in capacitance ratio calculation. Theoretically the maximum magnitude of this error is .04v.

Fig.7. *Simulated result of Temperature and pressure fuzzifiers which result the desired control surface*



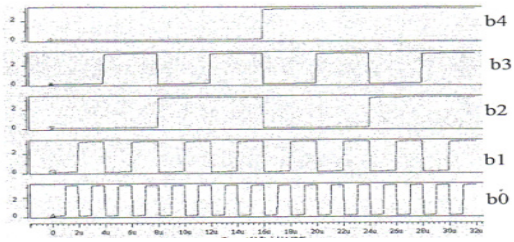
The modeled controller is implemented by MOS transistors in O.35um standard technology (the implementation of each block has described in details in previous sections). For performing language terms the fuzzifier which is described above _with outputs shown

in figure 7 for temperature and pressure_ is used here.

The degree of membership function for each analog inputs (h), obtain from input membership functions. After inferring, minimum of truth values transfer to defuzzifier block, Values of Si at defuzzifier circuit are chosen by output characteristics from expert tables or system considerations.

The layout of all blocks is extracted and extracted file of all system is simulated with HSPICE.

Fig.8. *the last typical output of total controller*



All outputs obtained of HSPICE simulation is compared to MA TLAB output modeling data.

Final output of controller is a crisp value corresponds to input signals as shown in figure 8.

In this paper, design and simulation of a novel fuzzy logic controller considered. The proposed controller is based on a new idea with digital input and output while in all internal parts analog circuitry has been used. Using this idea has added all privileges of analog design to a system with digital inputs and outputs. In previous digital works they have used full digital circuits which caused them high complexity. For achieving this idea, a novel programmable analog output fuzzifier with 5 bit resolution has designed. New min detector circuit is the result of this work, as well. Thanks to this idea it is possible easily implementing adaptive systems.

The precision of voltage-mode design is noticeable, since typical fuzzy logic applications employ current-mode implementations with lower precision.

5. Conclusion

The distinctive features of the proposed digital controller can be summarized as follows: Higher robustness against noise and distortion for input and output signals. Parallel Inference Engine: In this architecture, inference engine, thanks to using analog design, is organized in parallel configuration; therefore the inference speed is independent of the number of rules,

Programmability: By changing input parameters, we can change slope of MFs without changing circuit design. High speed processing: Due to the simple and parallel configuration can reach to a processing speed of 4.6MHz.

6. Acknowledgments

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