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Design of Two Stage CMOS Comparator with Improved Accuracy in Terms of Different Parameters

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Abstract: The well developing industry of electronics is insistent to low power and high speed and less area ADCs (analog to digital converters). Comparator is device that is especially employed in ADCs, used for division method, associated for square measure and chiefly liable for delay created and power consumption by an ADC. A low power and high speed comparator is needed to satisfy the longer term demands. The circuit conferred during this paper is designed using 0.35µm CMOS technology with 1.65V bias voltage and 12µA bias current. Cadence virtuoso tool is employed for the designing and simulation for the comparator circuit. The correct analysis of propagation delay, settling time, speed of the comparator is mentioned very well in detail.

Keywords: CMOS technology, Propagation delay, Settling time, Speed.

I. Introduction

Comparators approximates the distinction between 2 analog signals given as inputs, and assess digital output amplitude supported the polarity of this distinction. Comparators area units are wide employed in deciding circuits, level shifter, oscillators, ADCs etc. [1-7].

The various challenges while comparator design retires, when distinction among the 2 analog inputs signals approaches zero, when some noise on the signal cause change spurious change of the digital output [8-9].

This paper is organized as follows: second section describes comparator features; section three describes the look specification for 2 stage CMOS comparator; section four presents the simulation outcomes and the conclusion is given in section five.

II. Comparator Characteristics

A comparator is basically a circuit that compares 2 associated analog signals and outputs as a binary signal supported on the comparison (It is an operational amplifier without frequency compensation).

The desired (ideal) and realistic (actual) input output characteristic of a comparator are shown in Fig. 1. It's fascinating that the output (of ideal comparator) makes a spiky transition from Logic '0' to Logic '1', or the other way around, whenever the 2 input fast values cross one another. This means infinite gain analog differential electronic amplifier. However, usually a latch is employed because the deciding unit, which may accomplish a piercing, transition. The rise and fall time is set by the choice creating stage.

The decision creating stage - a latch - changes its state once the trigger input exceeds the switch potential. This provides rise to input offset of the comparator. Additionally addition, the PVT (VLSI industrial development, source voltage and temperature) variations, will produce a random quantity of offset voltage at the input of the differential amplifier. The offset affects the accuracy of comparator result. So as to scale back the result of offset, the input signals are amplified significantly before feeding to the choice creating circuit. Usually, the differential signal once rejecting the common mode element is amplified and fed to the Latch. These are the parameters of comparator at which comparator performance depends [10-12].

- *Speed or Propagation Time Delay*: The amount of the time between difference of voltage at inverting and non-inverting terminal is zero and also the output is fifty percent between initial and final value.
- *Resolving Capability:* The input modification necessary to cause the output to form a transition between its 2 stable states.
- *Input Common Mode Range:* The input voltage varies over the range which the comparator can find equal voltage at inverting and non-inverting terminal.
- *Input Offset Voltage:* The value of output voltage mirrored back to the input once the inverting terminal is physically connected to non-inverting terminal.

The input offset of a comparator is that the input voltage at which its output changes from one logic level to the opposite (neglecting noise). In a perfect comparator, this value would be zero. In a practical comparator, input offset could be caused by device mismatches or could be inherent within the style of the comparator [13].

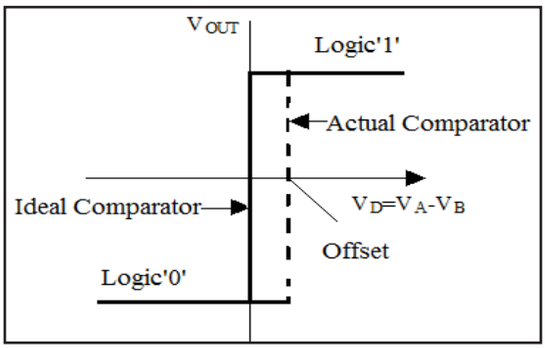

Fig. 1: Transfer Curve of Comparator Including Offset

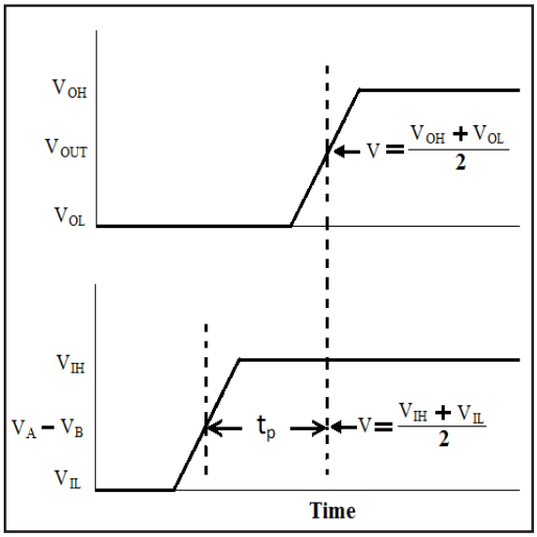

Fig. 2: Time Response of Comparator

Fig. 2 depicts the associated response of a comparator in nursing input as time function. There is a delay in time from input excitation and additionally the output response termed as propagation delay of the comparator. The delay in propagation of a comparator sometimes varies to realize the maximum amplitude of the input. A higher input can ends up in a lesser delay time. A higher limit at that an extra increase within the input voltage cannot have an effect on the delay [14].

III. Design Specification for Two Stage CMOS Comparator

The first basic comparator is two-stage CMOS electronic amplifier used as an electrical converter, shown in Fig. 3. The primary stage is a differential amplifier; the 2nd is a CS amplifier [15-16].

Transistors MN0, MN2, MN8, MP0 and MP4 make the differential stage and transistors MN3 and MP2 for the second stage of comparator, transistor MN9 is used for the bias circuit. These are the following specifications for designing the comparator for the channel length L=1.4µm.

Table I: Transistor Aspect Ratio

Parameters	Values
$(W/L)_1=(W/L)_2$	2
$(W/L)_3=(W/L)_4$	3
$(W/L)_5=(W/L)_8$	10
$(W/L)_6$	13.85
$(W/L)_7$	39.28

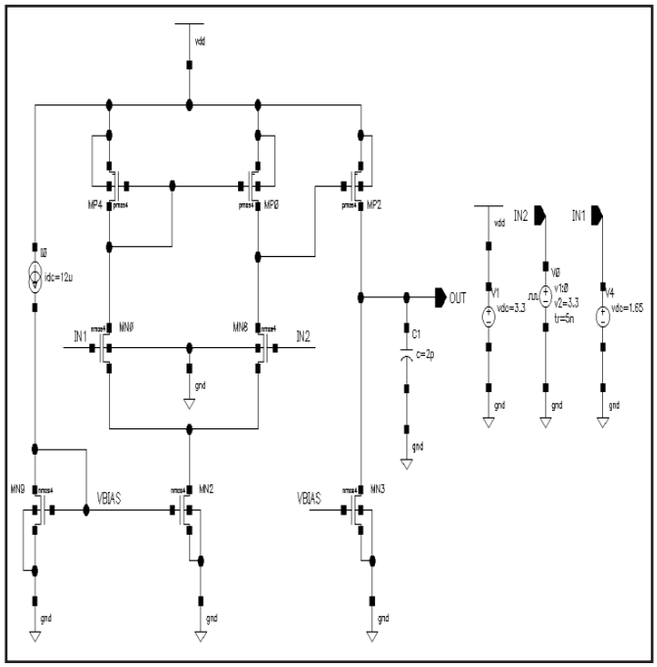

Fig. 3: Schematic of Two Stage CMOS Comparator

IV. Simulation Results

The simulation results of comparator shows that the propagation delay, speed and Settling time remains almost constant with the loss of accuracy. This implies that the loss in accuracy from 1.73% to 25%, leads the variation in the propagation delay from 17.6481ns to 16.1534ns, settling time from 37.3589ns to 23.22ns and speed from 56.66MHz to 61.90MHz for logic high.

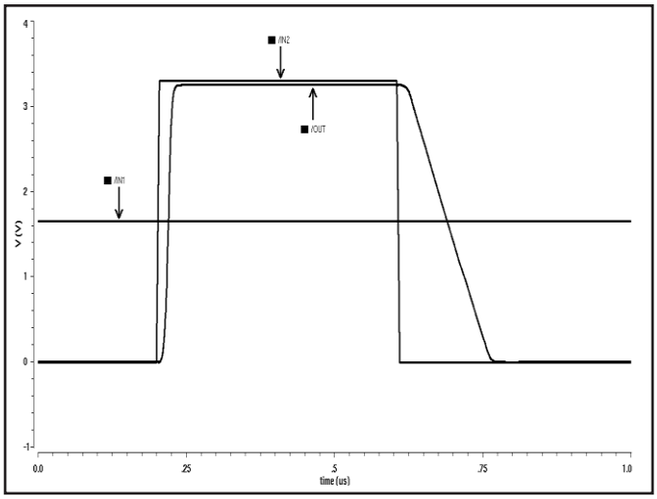

Fig. 4: Transient Analysis of Comparator

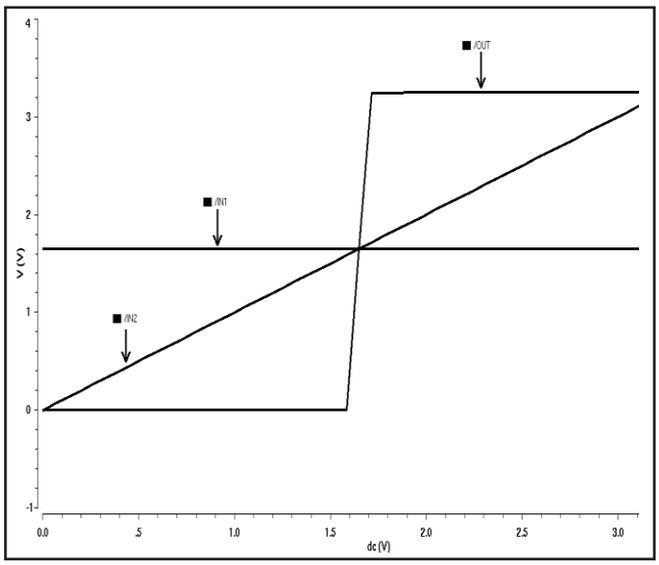

Fig. 5: DC Analysis of Comparator

Similarly for logic low as the loss in the accuracy vary from 1% to 25% leads the variation in the propagation delay from 156.92ns to 134.85ns, settling time from 156.26ns to 120.19ns and speed from 6.37MHz to 7.41MHz. The comparator parameters: propagation delay, settling time and speed is being calculated using the transient analysis over a period of 1µs as shown in the Fig. 4.

Next is the offset and resolution which are calculated by using DC analysis. For this set inverting terminal (IN1) at reference level of 1.65V and vary non-inverting terminal (IN2) from 0 to 3.3V as shown in Fig. 5.

The resolution of the comparator decides the speed of the ADC. Comparator resolution should be less than the ADC resolution. As fast the input changes the speed of ADC will increases.

Furthermore, the input-output waveform is obtained from the transient analysis.

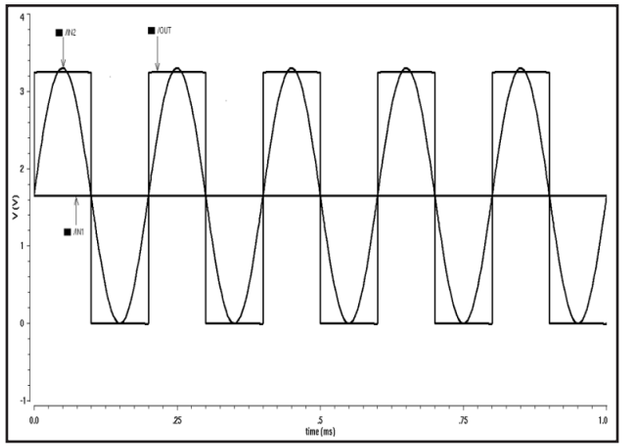

Fig. 6: Input-Output Waveform of Comparator

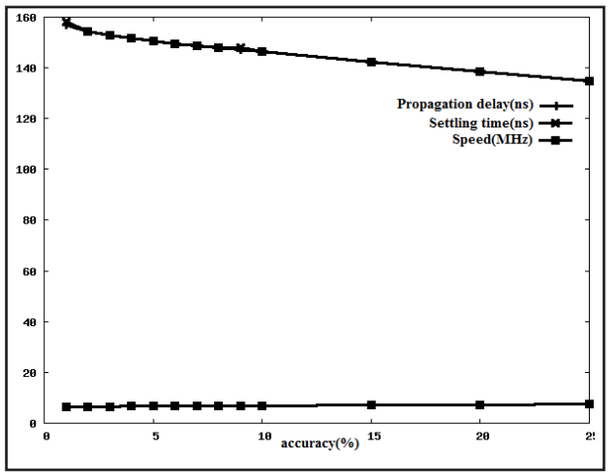

Fig. 7: Variation of Comparator Parameters with Respect to Accuracy for Logic Low

Fig. 7 and Fig. 8 shows that the propagation delay, settling time and speed of comparator are almost constant with the variation in accuracy for logic low and logic high. There is a little variation in the comparator parameters as more loss in the accuracy.

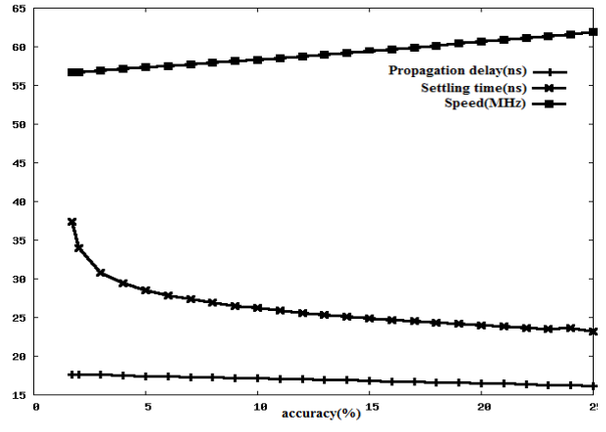

Fig. 8: Variation of Comparator Parameters with Respect to Accuracy for High Logic

TABLE II: SIMULATION RESULTS OF COMPARATOR

Parameters	Values
Resolution	0.78mV
Input offset	1μV
Output offset	2.8mV
Gain	86.23dB
Gain-bandwidth product (GBW)	48MHz
3dB frequency	84KHz
Propagation delay (for logic high with the loss of 1.73% accuracy)	17.64ns
Settling time (for logic high with the loss of 1.73% accuracy)	37.35ns
Speed (for logic high with the loss of 1.73% accuracy)	56.66MHz
Propagation delay (for logic low with the loss of 1% accuracy)	156.92ns
Settling time (for logic low with the loss of 1% accuracy)	158.26ns
Speed (for logic low with the loss of 1% accuracy)	6.37MHz

V. CONCLUSION

In this paper, a two-stage CMOS comparator circuit with their working and simulation results is presented. Table II represents values of various parameters obtained throughout the simulation. It's ended that the 2-stage comparator is superior in terms of many ways which are; lower random offset and power consumption, higher gain and compact space.

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