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A Low-Power Improved-Extended True Single Phase Clock Based Multi Modulus 32/33/47/48 Circuit for High-Speed Multiband Dividers

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Abstract: Multiband dividers are used in frequency synthesizer with variable channel spacing. In this paper low power Multi-Modulus 32/33/47/48 circuit is proposed at 6.5GHz frequency for multiband flexible divider application using 0.18um technology. The new Multi-Modulus 32/33/47/48 circuit consumes power of 0.86/087mW, 1.1/1.2mW in 32/33 and 47/48 modes respectively, when worked at 1.2V supply voltage.

Keywords: D Flip Flop (FF), Dual Modulus Prescaler (DMP), Improved Extended-True-Single Phase-Clock (I-ETSPC), Multi modulus.

I. Introduction

Power consuming modern communication system exhibits an issue for longer battery lifetimes. The frequency synthesizer plays a vital role in both receiving and transmitting the signal. Frequency divider is the power hungry block in high speed frequency synthesizer. Frequency synthesizer implemented using Source Coupled Logic (SCL) divider as the first stage, operates at higher frequencies however it suffers from high power dissipation. Dynamic dividers such True-Single-Phase-Clock (TSPC) design is compact compared to SCL dividers. This minimizes the number of interconnections and capacitive load leading to lower power consumption. Also, TSPC divider design minimizes the skew issue as it uses a single clock to drive the dynamic latch however; it has limitation of lower operating speed. The ETSPC logic based divider removes stacked structure i.e. one transistor taken out in each stage as compared with TSPC logic structure. All the Transistors of E-TSPC structure are free from substrate bias effect. Thus they are sustainable for high speed applications but suffer from static and short circuit power dissipation [1]-[6]. Improved Extended True Single Phase Clock (I-ETSPC) logic adds one more transistor in the third branch. It functions at higher speed and diminishes extra power consumption by reducing leakage current in critical path. In this work, a low-power Multi-Modulus 32/33/47/48 prescaler for multiband divider circuit (see Fig. 1) is designed using power efficient I-ETSPC based 2/3 prescaler.

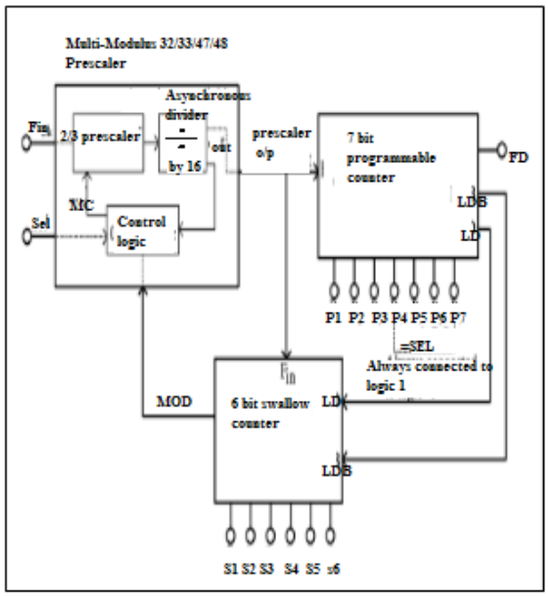


Fig. 1: Block Representation of Multi-Band Divider

II. I-ETSPC Based 2/3 Prescaler

An I-ETSPC design structure is far more refined than that of designs [7-9]. Compared with conventional designs, the I-ETSPC based ÷ by 2/3 design is complete without addition of extra logic. Both operating frequency and power consumption of the circuit remain unaffected, which designates a better performance over the logic inserted flip-flop designs. The circuit

ease, altogether, suggests the development in performances of the circuit.

Schematic of I-ETSPC based ÷ 2/3 prescaler design is depicted in Fig. 2 and working principle is reported in [10] is explained as follows. When high is applied at IN terminal of PMOS transistor, it acts as an open switch. When low is set to IN, the PMOS conducts and acts as a short circuit. An output of first stage I-ETSPC i.e. Q1b is passed to the input of second stage I-ETSPC. In an I-ETSPC FF design, the complemented output is produced at the output terminal 'Q1b'of the first stage.

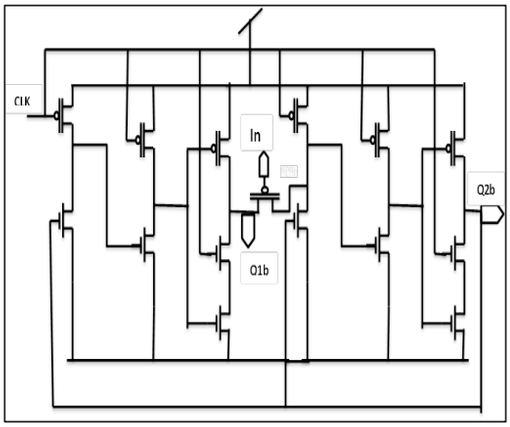


Fig. 2: I-ETSPC Based 2/3 Prescaler

The proposed prescaler can operate at 0.9V which is quiet smaller than the supply voltage of previous prescalers. Moreover, number of transistors in implementation of the proposed design is much lower than the previous prescaler implemented in Design [7], [8] and [9]. This leads to reduced load capacitance and lower power dissipation.

TABLE I: PERFORMANCE COMPARISON OF 2/3 CIRCUITS AT 0.18 µm

Design Parameters	[7]	[8]	[9]	Proposed
Transistor Count	16	16	23	15
Technology (µm)	0.18	0.18	0.18	0.18
VDD	1.499	1.499	1.79	0.9
Power (mW) ÷ by 2 unit	1.77	1.433	0.251	0.132

III. CONVENTIONAL MULTI MODULUS 32/33/47/48 CIRCUIT

Multi Modulus 32/33/47/48 circuit (refer Fig. 3) is essential part of multi band divider and can perform division of input signal frequency by four factors such as 32, 33, 47 and 48. The Multi Modulus circuit operation is basically analogous to operations of 32/33 and 47/48 Dual Modulus Prescalers (DMP) except inclusion of one additional multiplexer to switch the operation between 32/33 and 47/48 [11].

The Multi-modulus circuit apart from ÷ by 32 and ÷ by 33 performs extra divisions i.e. ÷ by 47 and ÷ by 48 without any additional circuitry, thus optimizing circuit complexity and improving power performances. Multi-Modulus circuit comprise of ÷ by 2/3 circuit, ÷ by two units (asynchronous counter), and combinational logic gates to attain more than one fractional divisions. In addition to standard "MOD" input for selecting the fractional ratios N/(N+1), the select line signal "Sel" of multiplexer chooses the operation modes between 32/33 and 47/48.

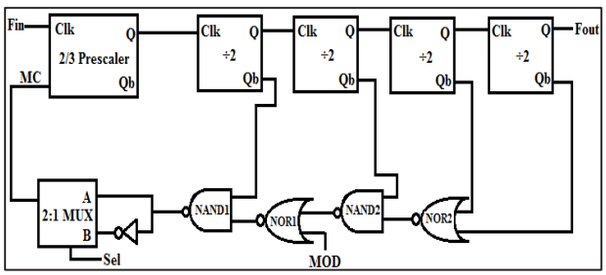


Fig. 3: Multi Modulus 32/33/47/48 Circuit

A. Case I: Sel = 'low'

The Multi Modulus circuit works in 32/33 mode when low is applied at select line "Sel" of multiplexer. The low signal on select "Sel" connects NAND1 gate output to"MC" of 2/3 circuit. The fractional division is switched by the "MOD"input connected to NOR1 logicgate. If "MC"is high, the ÷ by 2/3 circuit performs ÷ by 2 operation and when "MC" is low, the ÷ by 2/3 circuit performs ÷ by 3 operation. In addition if "MOD" is high, the output of NAND1 gate changes to logic '1' (MC= 1) then the prescaler works in the ÷ by two mode for completeaction. The ÷ by 32 (N) ratio is given as:

$$N = (Ad \times n1) + (0 \times (n1 + 1)) = 32 \quad (1)$$

If "n1"=2 and "Ad"=16 and "MOD"=0: For 30 clock periods "MC" goes high and circuit works in ÷ by.2 mode while for 3 input clock periods, "MC" goes low and the circuit works in the ÷ by 3 mode. The divide by 33 (N+1) ratio is given as:

$$N + 1 = ((Ad - 1) \times n1) + (1 \times (n1 + 1)) = 33 \quad (2)$$

B. Case II: Sel = 'high'

The Multi Modulus circuit works in 47/48 mode when high is applied at select line "Sel" of multiplexer. The high signal on select "Sel" connects the inverted output of the NAND1 to the "MC" of 2/3 circuit. The division ratio is changed by the "MOD" input connected to NOR1 gate. If "MC"=1, the ÷ by 2/3 circuit works in a ÷ by. 3. mode and when "MC"=0, the 2/3 circuit operates in a ÷ by 2 .mode and hence performs the opposite action to operation carried out when "Sel"=0. If "MOD" = 1, the output of NAND1 gate changes to logic '1' (MC=1) and the prescaler works in the ÷ by 2 mode for complete operation. The divide by 48 (N+1) ratiois given as:

$$N + 1 = (Ad \times (n1 + 1)) + (0 \times n1) = 48 \quad (3)$$

The divide by 47 (N) ratio is given as:

$$N = ((AD - 1) \times (n1 + 1)) + (1 \times n1) = 47 \quad (4)$$

IV. Proposed Multi Modulus 32/33/47/48 Circuit

In this work, we had designed 32/33/47/48 circuit by using divide by 2 and ÷ by 2/3 circuit using I-ETSPC technique and the NAND and NOR gate using sleepy keeper approach [12]. The block representation of the new Multi-Modulus prescaler on schematic editor has been shown in Fig. 4. The Simulation waveform of the new Multi Modulus circuit is depicted in Fig. 5 and Table II illustrates the simulated performance comparisons of Multi-Modulus circuit with existing design.

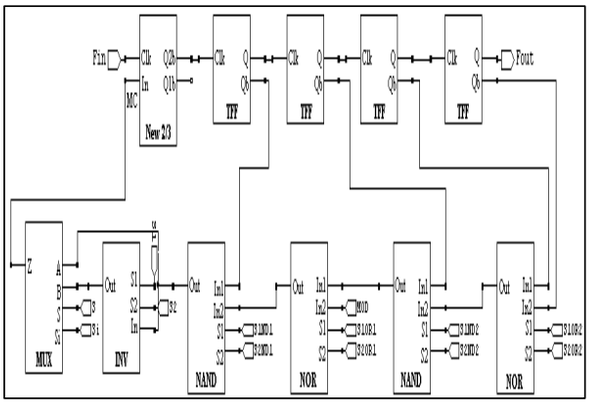
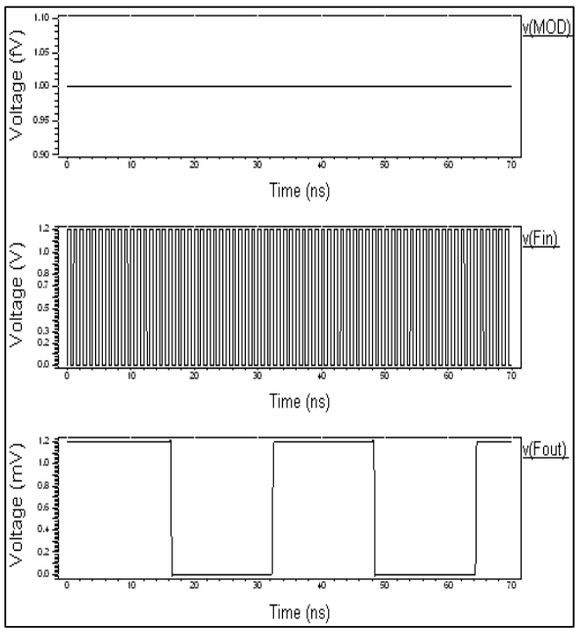
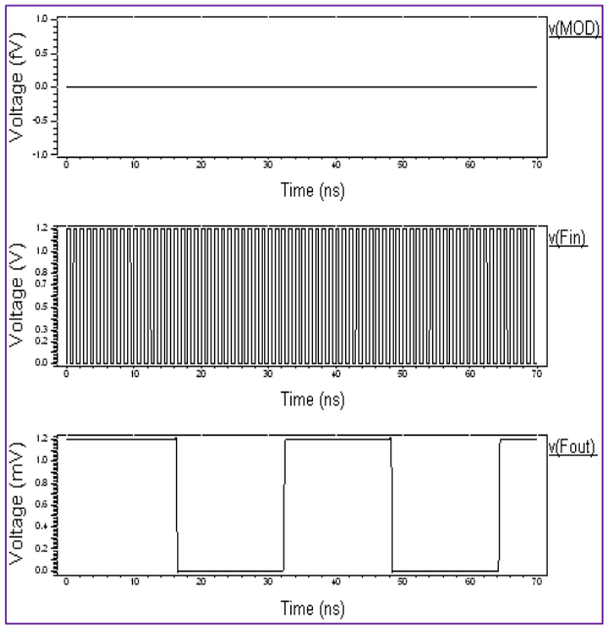


Fig. 4: Schematic View of Multi Modulus 32/33/47/48 Circuit Using Proposed 2/3 Unit



(a)



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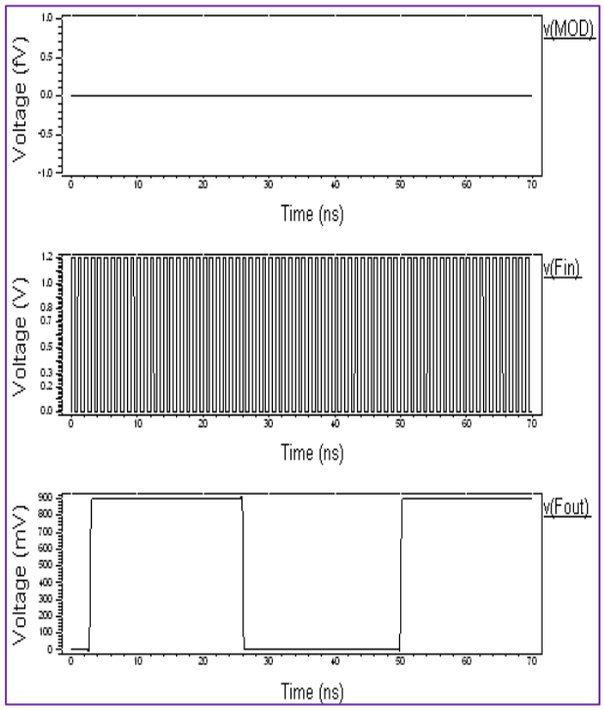

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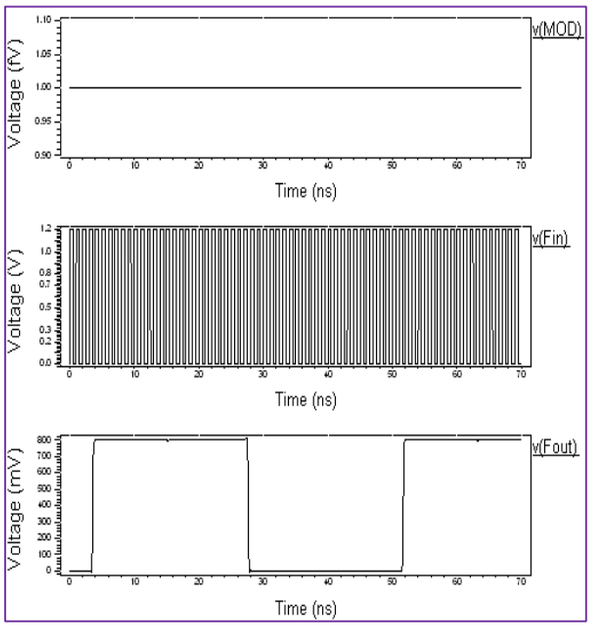

(d)

Fig. 5: Simulation Waveform of the new Multi Modulus 32/33/47/48 Circuit in (a) ÷ by 32 Mode (b) ÷ by 33 Mode [When Si=0] (c) ÷ by 47 Mode (d) ÷ by 48 Mode [When Si=1]

TABLE II: PERFORMANCE COMPARISONS OF PROPOSED MULTI MODULUS 32/33/47/48 CIRCUIT

Design Parameters	Design [11]	Proposed Multi Modulus 32/33/47/48
Technology	0.18um	0.18um
Voltage (vdd)	1.8	1.2
Operating freq.(GHz)	6.2	6.50
Mode 32/33 Avg.power (mW)	1.52/1.60	0.86/0.87
Mode 47/48Avg.power (mW)	2.10/2.13	1.1/1.2

V. CONCLUSION

In this brief, a novel I-ETSPC Multi Modulus 32/33/47/48 circuit has been proposed. The circuit uses sleepy keeper technique to reduce power in NAND and NOR gates. It uses I-ETSPC logic to minimize capacitive load and critical path delay in 2/3 prescaler unit. Comparing with Multi Modulus circuit in [11], the proposed circuit reducespower to ~43% and ~48% in 32/33 and 47/48 operations respectively. The proposed designs of ÷ by 32/33/47/48 prescaler demonstrates high speed of 6.5 GHz that is applicable in frequency synthesizers, Zigbee, WLAN applications. All the proposed design simulations are carried out at 180nm CMOS process at 1.2 V with tanner EDA tool. It is observed that, despite of working at high speed, the new multi modulus circuit has even lower power consumption than design [11].

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