Mody University International Journal of Computing and Engineering Research
Vol. 2 Issue 1, 2018, pp.05-10
ISSN:2456-9607 (Print) 2456-8333 (Online)

Design of Efficient Ring VCO using Nano Scale Double Gate MOSFET

Shruti Suman

Department of Electronics and Communication Engineering,
Mody University of Science and Technology, Lakshmangarh, Rajasthan

shrutisuman23@gmail.com

Received 1 Feb. 2018, Published 23 Feb. 2018

Abstract: In this paper a voltage controlled oscillator (VCO) using MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and Double Gate (DG) MOSFET are compared and analyzed. The comparison has been done on the basis of different parameters: voltage swing, tuning range, power consumption, number of stages and phase noise. Two architectures namely current starved ring VCO and inverter based oscillator are implemented using DG MOSFET. The results of simulation indicated that implementation using DG MOSFET, gives very high tuning range as compared to MOSFET based VCO. The Tuning range in current starved VCO using DG MOSFET is found out to be 16 GHz to 22 GHz compared to MOSFET which is only 3 GHz to 5 GHz. The phase noise performance of DG MOSFET based VCO is also better than MOSFET based VCO for low frequency domain.

Keywords: CMOS Technology, Ring Oscillator, Current Starved Ring VCO, Voltage Controlled Oscillator, Phase Noise, Double Gate MOSFET

1. INTRODUCTION

VCO is the most important and an indispensable part of electronic many electronic systems like frequency synthesizer, phase locked loop (PLL), temperature sensors, delay locked loop (DLL) [1, 6] and telecommunication systems. The growth of industries demands low power and better performance VCO design [7]. The principle behind oscillation is that if signal has a positive feedback to the input it will create a regenerative effect on input side for sus¬taining oscillation. The tremendous growth in wireless communication requires spectral purity, linearity of frequency with respect to control voltage, wide electrical tuning range, less area, low cost, frequency stability are the few requirements for a high quality VCO [9-12].

This paper introduces a ring oscillator and current starved ring VCO implementation using DG MOSFET, ensuring improved functionality when analyzed for prime design constraints such as frequency, technology, power consumption etc.

Further the paper has been structured into seven more sections illustrating CMOS ring oscillator, double gate MOSFET, analysis and design of existing CS ring VCO, implementation of proposed ring oscillator and current starved ring VCO followed by analysis, effect of process technology and control voltage on it, comparative analysis of existing and proposed design, and conclusion respectively.

2. CMOS RING OSCILLATOR

Oscillators are a positive feedback structure which amplifies its own noise at elected frequency. It is used for the purpose of generating periodic electrical output signal of certain frequency with a dc power supply. The frequency is variable with an applied voltage, making the oscillator a voltage controlled device. It is a cascaded loop connection of odd number of inverters depicts in Fig. 1. Output node of the last inverter is connected to the input node of the first inverter. Thus the circuit forms a voltage feedback loop and does not have a stable operating point. Each inverter consists of nMOS and pMOS transistor. In its basic form, the oscillation frequency ( ) mainly limited by the transit response of the pMOS transistor as the mobility of hole is two to three times lower than electron mobility in nMOS transistor.

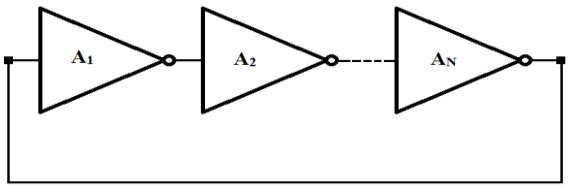

Fig.1. Single ended N stage ring oscillator

In order to design ring oscillator, where transistors are used to perform the voltage or current amplification, the circuit architecture need to be properly configured so as to satisfy the Barkhausen's criteria for oscillation [10,11].

The design of a ring oscillator involves tradeoffs of speed, power, area, and frequency.

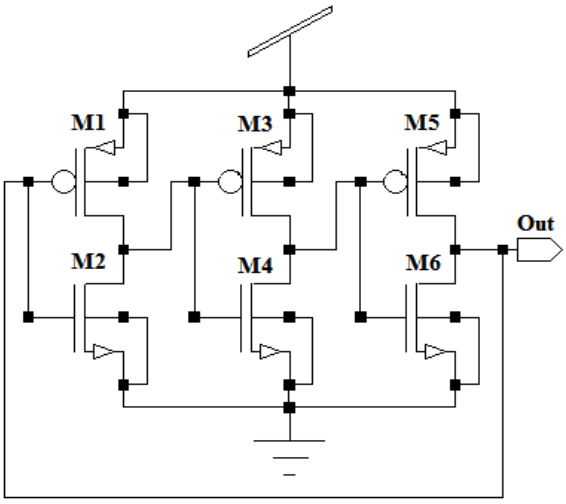

Fig. 2 Schematic diagram of three stage CMOS ring oscillator

The schematic diagram of three stage conventional CMOS ring oscillator is shown in Fig. 2. It works at the frequency in the KHz range at latest technology. To achieve oscillation, the ring must provide a phase shift of 2π radian and should have unity voltage gain. Hence each delay stage should provide phase shift of π / N radian, where N is number of delay stages. The remaining π radian phase shift is provided by dc inversion [11]. This indicates that for an oscillator with single-ended delay stages, an odd number of stages are required for the dc inversion.

3. DOUBLE GATE MOSFET (DG-MOSFET)

DG-MOSFETs are comprised of a drain, source, and two gates with conducting channel surrounded by gate electrodes on either side. Device structure of DG-MOSFETs is shown in Fig. 3 with circuit symbol in Fig. 4.

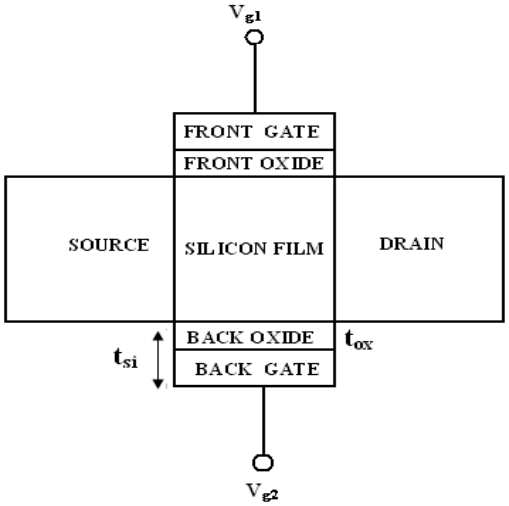

Fig. 3. Structure of DG-MOSFET

The advantages of DG-MOSFETs that it has lower subthreshold slope, the low drain-induced barrier lowering (DIBL), and the possibility of using a lightly doped or an un-doped body. It is proved that one double gate is equal to two single gate MOSFETs in parallel1 DGMOS = 2 SGMOS in parallel [12, 13].

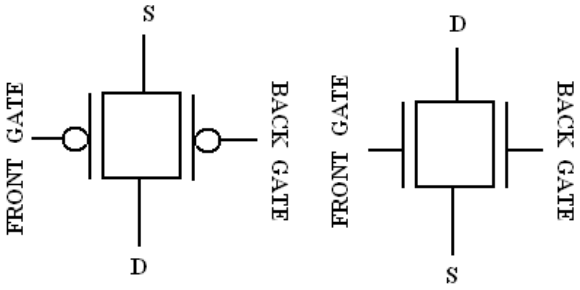

Fig. 4. Circuit symbols for p-type and n-type DG-MOSFET transistors

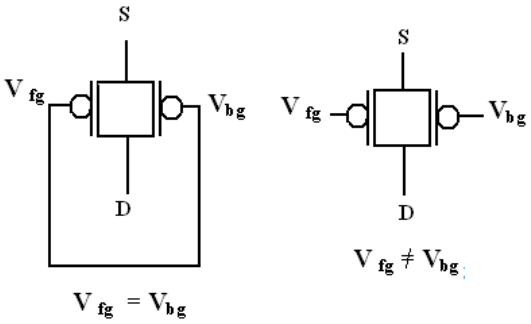

Fig.5. Symmetrical and independent driven double gate MOSFETs

4. SMALL SIGNAL ANALYSIS OF SINGLE GATE AND DOUBLE GATE MOSFET:

As described above, two single gate MOSFETs in parallel forms a one double gate MOSFET, so small analysis of double gate can be done considering this fact. Firstly, small signal analysis for single gate MOSFET has been done. The equivalent small signal circuit for single gate is shown in Fig. 6. Gain equation is observed as in equation (4.1).

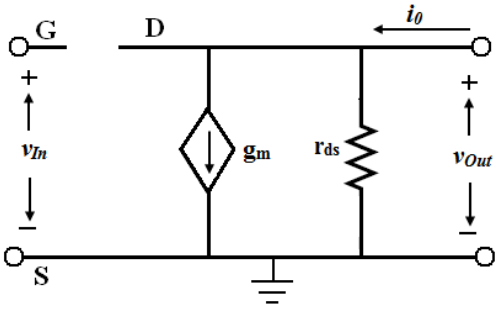

Fig.6 Small signal equivalent model of single gate MOSFET

$$A = \frac{v_o}{v_i} = -g_m r_o \qquad (4.1)$$

Where A, g_m, r_o, v_i and v_o, are gain, trans-conductance, output resistance, input voltage and output voltage of N-MOS transistor respectively.

The double gate MOSFET is shown in Fig.7 and equivalent small signal is given in Fig.8. The small signal model is based on concept that double gate MOSFET is considered as two single gates MOSFETs in parallel.

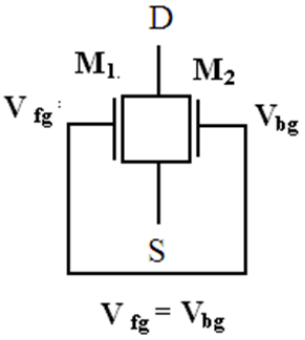

Fig.7. Double gate MOSFET

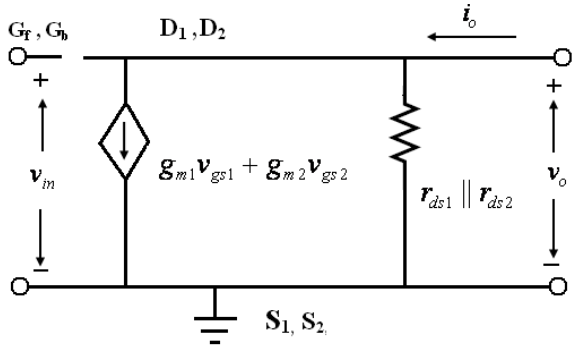

Fig.8. Small signal equivalent model of double gate MOSFET

The gain for above configuration is given in equation (4.5) as

$$A = \frac{v_o}{v_i} = (g_{m1} + g_{m2})(r_{ds1} \parallel r_{ds2}) \qquad (4.2)$$

$$g_m = g_{m1} + g_{m2} \qquad (4.3)$$

$$r_{ds} = r_{ds1} \parallel r_{ds2} \qquad (4.4)$$

$$A = -g_m r_{ds} \qquad (4.5)$$

Where g_{m1}, g_{m2} are and r_{ds1}, r_{ds2} are output resistances of transistor in parallel M1 and M2. A, g_m and r_o are gain, equivalent trans-conductance and equivalent output resistance of transistor. v_i and v_o input and output voltage respectively. The final gain is given by equation (4.6). For independent mode the input voltage at second gate is considered zero for small signal model. Gain equation for independent mode is given as:

$$A = -g_{m1}(r_{ds1} \parallel r_{ds2}) \qquad (4.6)$$

The device structure of DG-MOSFETs has been described in above section and it is suitable to make radio frequency devices. For analog circuits, the independent driven mode is used to design the circuits. The back gate will be used for the tuned circuit performance. Due to analog tunable functionality, these circuits provide extra gains in terms of area, power and speed by using DG-MOSFET in independently driven mode (IDDG) where the two gates are separated and biased in a different way.

5. DG-MOSFET BASED RING OSCILLATOR TOPOLOGY

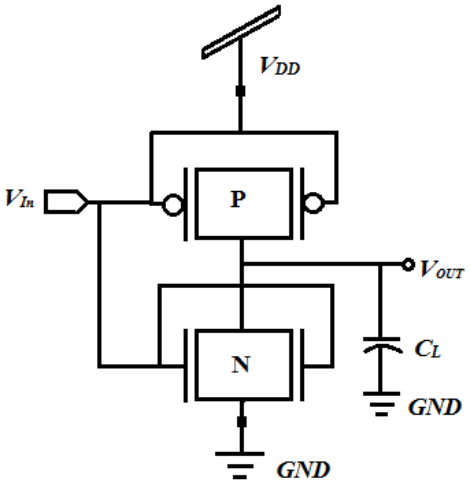

Fig. 9. DG MOSFET based inverter

As each stage of a regular ring oscillator is composed of a CMOS inverter as shown in Fig. 9. The conventional MOSFETs are replaced by the DG-MOSFET equivalents, which make up the single stage of the proposed DG-MOSFET based ring oscillator as shown in Fig. 10. The operating frequency of this oscillator is 8 GHz at 45 nm CMOS technology.

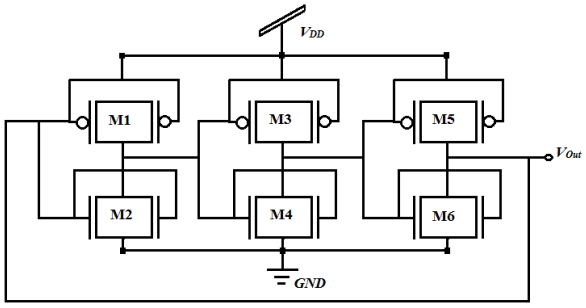

Fig.10. DG MOSFET based three stage ring oscillator

6. DG-MOSFET BASED CURRENT STARVED RING VCO:

In current starved ring VCO, the control voltage V_{Ctrl} modulates the turn-on resistance of the pull-down transistor and pull-up transistors through a current mirror. The variable resistance controls the current to charge or discharge the load capacitance [16-21]. Large control voltage permits more current flow, offering less resistance, less delay and produces high frequency. This class of VCO, thus, employs variable bias currents to adjust its oscillation frequency.

The oscillation frequency is related to the bias current I_D, number of stages N, total capacitance C_{total} and control voltage V_{Ctrl} as [16]

$$f_{Osc} = \frac{I_D}{2NC_{total}V_{Ctrl}} \qquad (6.1)$$

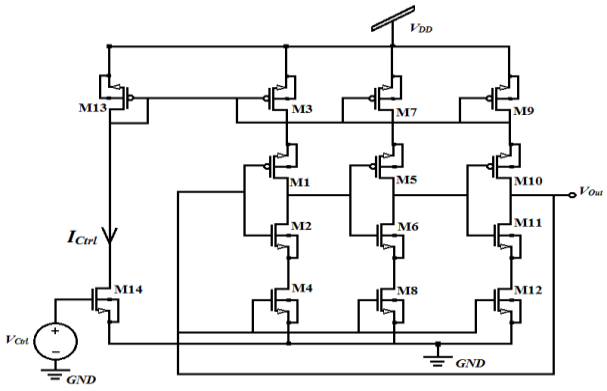

Fig.11 Three stage current starved ring VCO

The conventional MOSFETs are replaced by the DG-MOSFET equivalents, which make up the single stage of the proposed DG-MOSFET based current starved ring VCO as shown in Fig. 11 and Fig. 12 respectively.

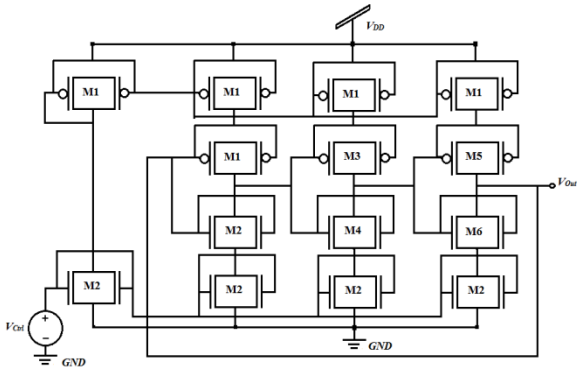

Fig.12. The DG MOSFET based three stage current starved ring VCO

7. SIMULATION RESULTS:

Table I summarizes the variation of oscillation frequency and power consumption with respect to control voltage at different supply voltages at 45 CMOS technology. It is than concluded that with using recent technology, the tuning range in current starved VCO using DG MOSFET is found out to be 16 GHz to 22 GHz compared to MOSFET which is only 3 GHz to 5 GHz. Further the Table II includes the comparison of simulation results of three stage current starved ring VCO and DG based ring VCO at 45 CMOS technology at different supply voltages. Also it depicts almost linear relation between control voltage and frequency of oscillation and endow with a wide tuning range from 16 GHz to 22 GHz at 0.4 V to 1.8 V control voltages with power consumption of 0.09 mW to 2.02 mW. The phase noise performance of DG MOSFET based VCO is also better than MOSFET based VCO for low frequency domain.

TABLE I. SIMULATION RESULTS OF PROPOSED THREE STAGES DG CURRENT STARVED RING VC AT 45 NM CMOS TECHNOLOGY WITH SUPPLY VOLTAGE 1.8 V.

Control voltage (V)	Frequency of oscillation (GHz)	Power consumption (mW)
0.4	16.22	0.059
0.6	17.23	0.378
0.8	18.67	0.889
1.0	19.09	0.401
1.2	20.87	0.846
1.4	21.06	1.222
1.6	21.62	1.488
1.8	22.04	2.021

TABLE II. SIMULATION RESULTS OF THREE STAGE CURRENT STARVED RING VCO AND DG BASED RING VCO AT 45NM CMOS TECHNOLOGY AT DIFFERENT SUPPLY VOLTAGES

Control Voltage (V)	Frequency (GHz) at 45 nm CMOS Technology					
	Supply Voltage 1V		Supply Voltage 2V		Supply Voltage 3V	
	Existing	Proposed	Existing	Proposed	Existing	Proposed
0.4	0.1703	16.42	0.3831	16.77	0.6289	19.56
0.6	0.8474	16.93	1.2520	17.26	1.6066	19.89
0.8	1.1549	17.04	2.1985	18.08	2.0516	20.45
1.0	1.2267	18.93	2.7355	20.54	2.8716	22.03

8. CONCLUSIONS

Being the basic blocks of integrated circuits, implementation of basic inverter and current starved based ring oscillators as delay elements is discussed. The implementation of nanoscale DG MOSFET based implementation of current starved ring VCO are incorporated here with the comparison of the simulated performance at 45 nm CMOS technology. The simulation results show higher oscillation frequency for proposed design that can be achieved by increasing control voltage. Oscillation frequency can also be changed by variation in supply voltages. The proposed designs are very much useful for various applications.

REFERENCES

[1] Shruti Suman, K. G. Sharma and P. K. Ghosh, "Design of PLL Using Improved Performance Ring VCO" - in International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT, held at D. M. I. College of Engineering, Chennai during 3-5 March 2016, ISBN: 978-1-4673-9939-5, pp.-3478-3483, DOI: 10.1109/ICEEOT.2016.7755351

[2] Shruti Suman and B.P. Singh "Design of Temperature Sensor Using Ring Oscillator" in International Journal of Scientific & Engineering Research, Vol. 3, No. 5, May 2012, ISSN 2229-5518.

[3] Shruti Suman, K. G. Sharma, P. K. Ghosh, "250 MHz multiphase delay locked loop for low power applications" in International Journal of Electrical and Computer Engineering, Vol. 7, No. 6, , 2017, pp. 3323-3321

[4] Shruti Suman and Prof B.P. Singh "Ring Oscillator based CMOS Temperature Sensor Design" in International Journal of Scientific & Technology Research, Vol. 1, No.4, May 2012, ISSN 2277-8616.

[5] B. Razavi, Design of Analog CMOS Integrated Circuits, Tata McGraw- Hill, Third edition, (2001).

[6] Adel S. Sedra and Kenneth C. Smith, "Microelectronics Circuits," Oxford University Press, fourth edition, 1997.

[7] Shruti Suman, K. G. Sharma, P. K. Ghosh, "Analysis of Phase Noise and Jitter in Ring Oscillators", in "Innovative Systems Design and Engineering, International Institute for Science, Technology and Education, Vol. 8, No. 2, 2017, pp. 1- 9.

[8] Shruti Suman, K. G. Sharma, P. K. Ghosh, Performance Analysis of Voltage Controlled Ring Oscillators, – in "International Congress on Information and Communication Technology (ICICT)", Advances in Intelligent System., Computing (AISC), Vol. 439, Chapter 4, ISSN 978-981-10-0754-5, Udaipur, 9 – 10 October 2015, pp.-29-38.

[9] Shruti Suman, Monika Bhardwaj, Prof. B. P. Singh "An Improved Performance Ring Oscillator Design," International Conference on Advanced Computing & Communication Technologies, 7-8 January 2012 Rohtak, India, ISBN: 978-0-7695-4640-7, 2012, pp. 236-239.

[10] M. Tiebout, Low Power VCO Design in CMOS, Advanced Microelectronics, Springer Berlin Heidelberg New York, 2011.

[11] Vaishali, Shruti Suman, K. G. Sharma, P. K. Ghosh , "Design of Ring Oscillator based VCO with Improved Performance"-in Innovative Systems Design and Engineering, Vol.5, No.2, 2014, pp. 31-41, ISSN 2222-1727 (Paper), ISSN 2222-2871 (Online), DOI: 10.1109/ACCT.2015.127.

[12] M. Reyboz, O. Rozeau, T. Poiroux and P. Martin, "Asymmetrical Double Gate (ADG) MOSFETs Compact Modeling," cea-leti, Research Institute, France, 2005.

[13] P. Freitas and H. Lapuyade, "Analog Design Considerations for Independently Driven Double Gate MOSFETs and their Application in a Low-Voltage OTA," 14th IEEE International Conference on Electronics, Circuits and Systems, 2007.

[14] M. V. R. Reddy, D. K. Sharma, M. B. Patil, & Rao, "Power-area Evaluation of Various Double-Gate RF Mixer Topologies," IEEE Electronic Devices Lett. Vol. 26, 2005, pp. 664.

[15] Datta, A.; Goel, A.; Cakici, R.T.; Mahmoodi, H.; Lekshmanan, D. & Roy, K.; Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices IEEE Trans. CAD of Integrated Circuits and Systems, vol.26, no.11, Nov. 2007, pp.1957-1966.

[16] Shruti Suman, K. G. Sharma and P. K. Ghosh, "Analysis and Design of Current Starved Ring VCO" - in International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT) , held at D. M. I. College of Engineering, Chennai during 3-5 March 2016, ISBN: 978-1-4673-9939-5,pp.-3222-3227, DOI: 10.1109/ICEEOT.2016.7755299.

[17] Bhawika Kinger, Shruti Suman, , K. G. Sharma, P. K. Ghosh, "Design of Improved Performance Voltage Controlled Ring Oscillator" – in 5th IEEE International Conference on Advanced Computing & Communication Technologies, Rohtak, (India), during February 21-22, 2015, pp. 441-445. ISBN 978-1-4799-8487-9, DOI 10.1109/ACCT.2015.127

[18] Bhavana Goyal, Shruti Suman, P. K. Ghosh , "Design and Analysis of Improved Ring VCO Based on Differential Pair Configuration" - in International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), held in D. M. I. College of Engineering, Chennai during 3 – 5 March 2016,ISBN: 978-1-4673-9939-5,
DOI: 10.1109/ICEEOT.2016.7755348

[19] Yuan taur and Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, second edition, 2001

[20] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 2nd ed., Piscataway, NJ: Wiley Inderscience & IEEE Press, pp. 551–607, 2005S. Kang, and Y. Leblebici, CMOS Digital Integrated Circuits Analysis and Design, New York: International Edition, McGraw-Hill, pp. 218–231, 2003