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Reduction of power dissipation in sequential circuits

B. I. Neelgar, Prabhu. G. Benakop*
G.M.R. Institute of Technology, Rajam-532127, Andhra Pradesh, India
**Aurora Engineering College, Bhongir-508116 Andhra Pradesh, India*
basneel@rediffmail.com pgbenakop@rediffmail.com*

Abstract: In this paper, an attempt is made to reduce the power consumption of a synchronous digital system by minimizing the total power consumed by the clock signals. This paper presents a state assignment technique called priority encoding which uses multi-code assignment plus clock gating to reduce power dissipation in sequential circuits. The basic idea is to assign multiple codes to states so as to enable more effective clock gating in the sequential circuit. Experimental results demonstrate that the priority encoding technique can result in sizable power saving.

Keywords: priority encoding, multi code state assignment, clock gating.

Introduction

Modern digital systems are designed with a target clock period (or clock frequency), which determines the rate of data processing. A clock network distributes the clock signal from the clock generator, or source, to the clock inputs or sinks of the synchronizing components, or modules. The clock distribution network consumes large percentage (20%-50%) of the power consumed by these systems. Therefore, in low-power synchronous systems, it is feasible to minimize the total power consumed by the clock tree subject to performance constraints on the clock signal, such as the operating frequency and maximum clock skew. The power consumed by Complementary Metal Oxide Semiconductor (CMOS) circuits consists of two components: Dynamic power dissipation and Static power dissipation. The dynamic power consumed by a module clocked at a frequency f is given by $P= C_L V_{dd}^2 f$, where Vdd is the supply voltage and C_L is the total load capacitance on the circuit. If a circuit switches 'a' times per clock cycle, then its power consumption is given by $P = a\ C_L V_{dd}^2 f$, where 'a' is called the *circuit activity.* To minimize the power consumed by a CMOS synchronous system, it is required to minimize its total activity.

During the low-power design of the combinational circuits, it has been found that blocking the redundant signals and shutting off the redundant parts of the circuit is an effective method to lower the energy dissipation (Roy & Prasad, 1993). If some part of the circuit has no effect on the circuit functionality during some time period, then this part is functionally redundant in that period. If the part is made inactive (by cutting off the power supply), then power can be saved. This technique of exploiting redundancy can be applied to combinational logic part of a finite state machine. A sequential circuit is however different from a combinational one in a number of important aspects:

(i) A sequential circuit has flip-flops, which store state signals.

(ii) A sequential circuit receives a special signal called clock, which is used to synchronously trigger the flip-flops.

(iii) States are assigned by encoding the state variables. The three restraining techniques with respect to each of these aspects are:

1. Traditional flip-flops are single-edge triggered flip-flips (SETFF), which are sensitive to either rising or falling edge of the clock. So half of the clock transitions do not have any impact on the circuit and thereby create redundant behaviors, which in turn results in wasted power dissipation in the flip-flops. For this reason, a double-edge triggered flip-flop (DETFF) can be used, which utilizes both transition edges of the clock, and thereby achieves power saving (Macii *et al.*, 1998).
2. The function of the clock is to force all flip-flips to synchronously change their state (from present state to next state). During this switching process, if the next state of a certain flip-flop is the same as its present state, then this flip-flip will be in a holding mode. The clock's triggering action for this flip-flop becomes redundant and can be masked. Therefore, clock gating technique can be used to lower the power dissipation (Unger, 1981; Benini & Micheli, 1995).
3. During state assignment, k state variables are used to express 2^k different states. However, if the number of functional states *l* is not equal to 2^k , i. e., $l < 2^k$, then there will exist $(2^k - l)$ redundant states. These redundant states may be used in reducing the complexity of the combinational circuit, but reliability of the circuit may be adversely affected.

This paper proposes a priority encoding

technique to eliminate any unused state code. The result is that some states do not require binary assignment of all state variables. When the system is in such a state, the unused state variables become redundant. Because the corresponding flip-flop outputs are not used, these flip-flops can be isolated from the clock to reduce their power dissipation.

Priority encoding by using redundant states

In combinational circuit design, the existence of redundant states is helpful in generating a large prime implicant during Boolean function minimization. If the implicant contains 2^m minterms, a maximum of m variables may be eliminated from the product form. If k state variables are used to express '*l* different states (*l* <= 2^k) there will be (2^k - *l*) redundant states. These redundant states may be utilized to make some states multi-coded e.g., two-coded, four-coded, etc. These state assignments give rise to large implicants during combinational circuit optimization, thus reducing the complexity of the combination circuit implementation.

An example of sequential circuit with a lot of redundant states is the 4-bit, 4-stat counter, where each state corresponds to a state variable. Take the four-state (S1, S2, S3, S4) counter as an example Fig.1(a) shows the state assignment Karnaugh map and the state assignment table of the four states corresponding to state variables (S1,S2, S3 , S4).

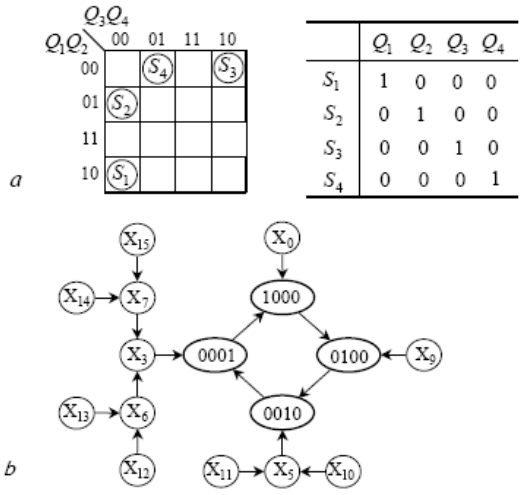

Fig. 1. Design of a 4 bit 4 state Ring Counter
(a) K-map and Truth table
(b) Complete state diagram of the self-corrective design

Notice that each state is encoded by a state variable minterm. The result is a set of twelve (12 = 2^4 - 4) redundant states, which are depicted by empty rooms in Fig 1(a). Although these redundant states can be used to simplify the excitation functions (**D1=Q4, D2=Q1, D3=Q2, D4=Q3),** the problem is that the design will not be self-corrective. It is required to change D1 function to **D1=Q1'Q2'Q3'** to meet this requirement. The complete state diagram of the revised circuit is shown in Fig. 1(b). One can easily verify that if the circuit enters one of the invalid states, it will return to the valid working cycle in a period not more than three clock cycles. These twelve redundant states can be used to realize the multi-code state assignment, as shown in Fig. 2(a).

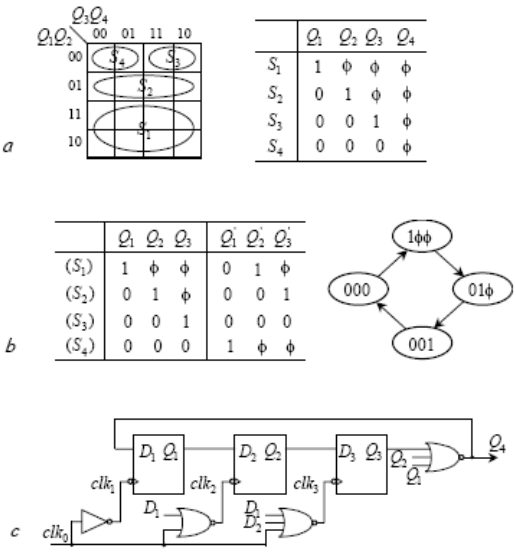

Fig. 2 Design of a one-zero-hot ring counter

(a) Karnaugh-Map and tabular description of state assignment

(b) State table and state diagram

(c) Gated-clock design

Note that encodings for **(S1 , S2 , S3 , S4)** are **Q1, Q1'Q2, Q1'Q2'Q3 and Q1'Q2'Q3'**, hence state variable Q4 is immaterial and can be omitted. Because state S4 is encoded by three zero state variables, the ring counter has evolved from a **one-hot type to a one- zero-hot type** (Prosser & Wu, 1988). Because D flip-flops, are used Qi' = Di, hence the next state equations and the excitation functions of the three flip-flops can be derived based on the state table shown in Fig. 2(b):

D1 = Q1 + Q2 + Q3 , D2 = Q1 , D3 = Q2

These equations may be used to realize a ring counter with correct functionality, but without any clock gating. The clock-gating functions are derived as discussed next.

In Fig. 2(b) S1 is four-coded and S2 is two-coded whereas S3 and S4 are uni-coded. It can be seen that Q1 has the highest priority, which means that when Q1 =1, Q2 and Q3 are don't cares. Similarly, Q2 has the second highest priority because when Q1 =0 and Q2=1, then Q3 is don't care. Therefore, in the corresponding circuit, Q1 =1 can be used to restrain the switching of Q2 and Q3, whereas Q2 =1 can be used to restrain the switching of Q3. The restraining functions can be realized by a clock-gating technique, as shown in Fig.2(c). The signal for gating the clock signal to the second flip-flop must be D1, and not Q1. The reason is that when the clock to the second flip-flop arrives, D1 =1 will force Q1 =1, which will subsequently block the clock to the second and third flip-flop immediately. Similarly, D1 =1 and D2 =1 is used to mask the clock to the third flip-flop as opposed to using Q1 and Q2. If delays of the two NOR gates that produce the gated clock signals clk2 and clk3 are the same as that of the inverter which produces clk1, then the three flip-flops will all work synchronously. Notice that the omitted fourth flip-flop is replaced by the NOR gate that produces Q2. The circuit of Fig. 2(c) has been simulated by Micro-wind. Fig. 3 shows waveforms of the clock and the output signals. The three derived clocks clk1, clk2, and clk3 are quasi-synchronous. The output waveforms show the circuit functionality is correct.

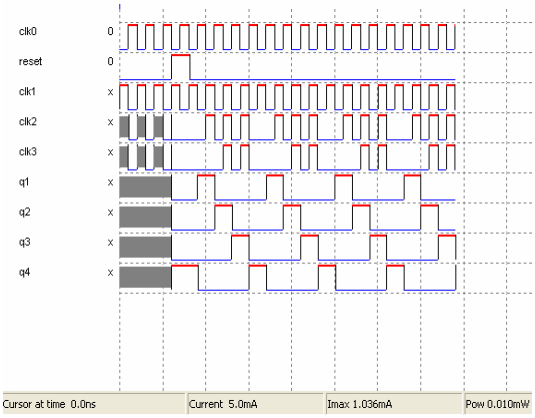

Fig. 3. Simulation of one -zero hot counter

The state assignment table in Fig.1 (a) shows that the four flip-flops receive 16 triggering actions from the clock in one cycle. However, the state assignment table in Fig. 2(b) shows that the three flip-flops receive only 9 triggering actions from the clock in one cycle. Consequently, the maximum power saving due to reduction of one flip-flop and clock gating is (16-9)/16 = 43%. Finally, it should be pointed out that the design of Fig. 2(c) not only simplifies the circuit realization and saves energy dissipation, but also improves the circuit reliability because it eliminates the unused states. The complete state diagram in Fig. 2(b) shows this advantage.

Multi-code state assignment with clock gating

The uni-code state assignment corresponds to a minterm of the state variable space. In contrast, the multi-code state assignment contains 2^m minterms of the state variable space, thereby eliminating $2^m - 1$ redundant states. In general, the set of redundant states can be decomposed into groups of $2^i - 1$ states and determines the corresponding multi-code state assignments. In the previous section, there were 12 redundant states when using four state variables (Q1, Q2 , Q3 , Q4). The non-redundant state assignment in Fig. 2(a) was obtained according to the grouping 7+3+1+1=12. If we used three state variables (Q1, Q2, Q3) instead, then the number of redundant states would be reduced to 4. Since 4 = 3+1, the non-redundant state assignment in Fig. 2(b) would be achieved. Obviously, the inclusion of redundant states increases the complexity of the state assignment procedure. One popular sequential circuit is discussed next.

BCD Counter

In this counter, the counting states (0, 1, 9) are encoded with the conventional 8421 BCD encoding, as shown on the leftmost column of Table 1. Notice that there are 6 redundant states: (1010, 1011, 1100, 1101, 1110, 1111).

From the above table, the excitation functions for the four flip-flops are derived as:

Table 1: Two encodings of a decimal up-counter

	8421 BCD encoding				Priority-encoding			
digit	*D*	*C*	*B*	*A*	*D*	*C*	*B*	*A*
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	ϕ	ϕ	0
9	1	0	0	1	1	ϕ	ϕ	1

$$
\begin{aligned}
D_D &= CBA + D\overline{A}, \\
D_C &= C\overline{B} + C\overline{A} + \overline{C}BA, \\
D_B &= \overline{D} \cdot \overline{B}A + B\overline{A}, \\
D_A &= \overline{A}.
\end{aligned}
\qquad (1)
$$

Since 6 = 3+3, two states among the ten digits can be four-coded. Analyzing the original 8421BCD state encoding table, states 8 and 9 can be four-coded, as shown on the right side of Table 1. This new scheme maintains the characteristics of the original circuit. When D =1, the state variables C and B become don't cares, therefore the priority of D is higher than C and B. In the circuit realization, when the input of flip-flop D is 1, this input can be used to isolate the clock that triggers flip-flops C and B so as to reduce the corresponding energy dissipation. The new excitation functions for the four flip-flops are:

$$\begin{aligned} D_D &= \overline{D}CBA + D\overline{A}, \\ D_C &= \overline{D}C + \overline{D}BA, \\ D_B &= \overline{D} \cdot \overline{B}A + B\overline{A}, \\ D_A &= \overline{A}. \end{aligned} \qquad (2)$$

Comparison between eqn.1 and eqn.2 shows that D_B and D_A are the same in both sets. However, in the latter design, a literal $\overline{D}$ is added to D_D and the form of D_C is simplified. The result is that the combinational circuit part is simpler and the power dissipation is lower. As for the energy dissipation of flip-flops, the occurrence probability of each state in any cycle is 10%. From the right part of Table 1, flip-flops C and B are don't cares in states 8 and 9. During a complete 0-9 count, 20% of power dissipation is saved for flip-flops B or C. For the same counting cycle, the power dissipation reduces in all four flip-flops by 10%.

Conclusions

State assignment of sequential circuits influences the complexity of their combinational circuit realization, to which designers attach a lot of importance. The state assignment also influences the switching behavior of the state variables, and hence the power dissipation in these circuits. This paper proposes a priority-based state assignment technique that exploits the redundant state codes to mask the clock to some of the flip-flops. Priority encoding thus not only eliminates the redundant state codes, but also improves the finite machine reliability. Two practical design examples were presented to show that this technique is feasible and can significantly reduce the energy dissipation.

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